

CMOS IMAGER WITH IMPROVED COLOR RESPONSE

FIELD OF THE INVENTION

[0001] The present invention relates to improved semiconductor imaging devices and, in particular, to a CMOS imager employing a storage capacitor for storing accumulated pixel signals.

BACKGROUND OF THE INVENTION

[0002] CMOS imagers have been increasingly used as low cost imaging devices. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits is beneficial in many digital imaging applications such as, for example, cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices, surveillance systems, auto focus systems and star trackers, among many others.

[0003] In a conventional (4T) CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge at a storage node; (3) transfer of charge from the node to an output transistor accompanied by charge amplification; (4) resetting the storage node to a known state before accumulation of image charge and selective output of reset and pixel image signals. A transfer transistor may also be used to transfer charge from a photo conversion element to the output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate.

[0004] Exemplary CMOS imaging circuits as well as detailed descriptions of the functions of various CMOS elements of an imaging circuit are described, for example, in U.S. Patent No. 6,204,524 to Rhodes, U.S. Patent No. 6,310,366 to Rhodes et al., and U.S. Patent No. 6,326,652 to Rhodes, which disclose a CMOS imager having a storage capacitor connected to the light sensitive node to improve collected storage charge, a pixel

sensor cell formed in a retrograde well in a semiconductor substrate, and self-aligned contact, respectively, the disclosures being incorporated herein by reference.

[0005] CMOS imagers typically suffer from poor signal-to-noise ratios and poor dynamic range as a result of the inability to fully store and utilize the electric charge collected by the photosensitive area. Consequently, storage capacitors have been proposed for use in connection with the light sensitive node of a CMOS pixel sensor cells to improve collected charge storage. For example, U.S. Patent No. 6,204,524 to Rhodes describes in detail the formation of planar and trench storage capacitors electrically connected in parallel with the light sensitive node of a CMOS pixel sensor cell.

[0006] Storage capacitors may also provide useful results when electrically connected to other light sensitive and/or electrical elements of the pixel sensor cell, such as transistor gates or floating diffusion regions, for example, to affect the operation and characteristics of such various light sensitive and/or electrical elements. Capacitors connected to such various light sensitive and/or electrical elements of the pixel sensor cell help amplify the signal of an imager transistor, increase the storage capacitance of a photosite, or provide a low noise decoupling capacitor.

[0007] Example of such storage capacitors are described in co-pending U.S. patent application Serial No. 10/303,897, filed November 26, 2002 by Howard E. Rhodes and Jeff McKee, entitled "CMOS IMAGER PIXEL DESIGNS," the disclosure of which is incorporated herein by reference. The storage capacitors are electrically connected to various light sensitive and/or electrical elements of a pixel sensor cell of a CMOS imager, to affect the operation and characteristics of such various light sensitive and/or electrical elements, add charge storage capability to the pixel sensor cell, independently set charge amplification, and improve the lag and scalability of pixel cells. According to one embodiment, the storage capacitor is formed electrically connected to a floating diffusion region of a pixel sensor cell and to an AC ground. The charge storage capacitor may be formed entirely overlying the field oxide region isolating a pixel sensor cell, or entirely overlying the active area of the imager, or partially over the field oxide area and partially over the active area. According to another embodiment, a charge storage capacitor is

formed electrically connected to and in parallel with a gate of a CMOS imager transistor, for example a charge transfer transistor, to tailor the voltage pulses to the transfer gate and the charge transfer characteristics of the transistor. In yet another embodiment, a plurality of storage capacitors are formed over a field oxide region isolating a pixel sensor cell, and further connected to various light sensitive or electrical elements of the imager. For example, one storage capacitor may be connected to a floating diffusion region and another storage capacitor may be connected to a charge collection region. Other embodiments provide a capacitor at one or more other connection locations of a pixel sensor cell, which can be formed entirely over a field oxide area, entirely over an active pixel area, or over a portion of a field oxide area and an active pixel area.

[0008] While the use of storage capacitors at various locations within a pixel improves pixel operation, those capacitors have the same capacitance value for each pixel color and are not optimized for the photon to charge conversion characteristics of each color pixel.

SUMMARY OF THE INVENTION

[0009] The present invention provides CMOS imagers having storage capacitors of selected capacitance connected to various light sensitive and/or electrical elements of a pixel sensor cell of a CMOS imager. The size of each capacitor is optimized based on the color to be detected by the pixel to which it is connected.

[00010] Also provided are methods of forming the pixels of CMOS imagers containing charge storage capacitors in which capacitance values are associated with each of the pixel colors.

[00011] The presence of a capacitor, and the size of any capacitor employed, is determined based on the color of the pixel to which the capacitor is connected. Generally, the capacitors fall within the range of 1-50 femtofarads (10^{-15} farads). In an RGB color pixel arrangement, for example, most preferably, red pixels will utilize the smallest capacitors, about 0-20 femtofarads, green pixels will utilize a middle range, about 2-20

femtofarads, and blue pixels will utilize the largest capacitors, about 3-20 femtofarads. The capacitors are sized in relation to the electron production of each colored pixel. Red pixels produce the fewest electrons, and therefore have the smallest, or no, capacitor. Blue pixels produce the most electrons, and therefore have the largest capacitor. Green pixels produce electrons in an amount between red and blue. Sizing the capacitor in relation on electron production allows a greater percentage of each capacitor to be utilized. By employing capacitors sized in relation to the electron production of each color pixel, the sensitivity of each pixel circuit is increased.

[00012] Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[00013] Figure 1 is a schematic diagram of a pixel sensor cell in accordance with a first embodiment of the present invention.

[00014] Figure 2 is a schematic diagram of a pixel sensor cell fabricated in accordance with a second embodiment of the present invention.

[00015] Figure 3 is a schematic diagram of a pixel sensor cell fabricated in accordance with a third embodiment of the present invention.

[00016] Figure 4 is a schematic diagram of a pixel sensor cell fabricated in accordance with a fourth embodiment of the present invention.

[00017] Figure 5 is a schematic diagram of a pixel sensor cell fabricated in accordance with a fifth embodiment of the present invention.

[00018] Figure 6 is a schematic diagram of a pixel sensor cell fabricated in accordance with a sixth embodiment of the present invention.

[00019] Figure 7 is a schematic diagram of a pixel sensor cell fabricated in accordance with a seventh embodiment of the present invention.

[00020] Figure 8 is an illustration of a processing system utilizing the pixel sensor cells of the present invention.

[00021] Figure 9 is an illustration of a Bayer filter used in conjunction with a pixel sensor array of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[00022] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

[00023] The terms “wafer” and “substrate” are to be understood as a semiconductor-based material including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a “wafer” or “substrate” in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, gallium arsenide or other semiconductor material.

[00024] The term “pixel” refers to a picture element unit cell containing a photosensor and transistors for converting light radiation to an electrical signal. For purposes of illustration, a representative pixel is illustrated in the figures and description

herein and, typically, fabrication of all pixels in an imager will proceed simultaneously in a similar fashion.

[00025] Methods of manufacturing the pixels disclosed herein are taught in related U.S. Patent Application Serial No. 10/303,897, filed November 26, 2002, in the names of Howard E. Rhodes and Jeff McKee, and entitled "CMOS IMAGER PIXEL DESIGNS," referred to above.

[00026] Referring now to the drawings, where like elements are designated by like reference numerals, Fig. 1 illustrates a first exemplary embodiment of the invention. A pixel sensor cell 100 is illustrated having a storage capacitor 199 overlying a field oxide region, and electrically connected to a floating diffusion region 130 and to ground. As explained in more detail below, storage capacitor 199 is formed so that it does not block any light sensitive areas of the imager. In addition, storage capacitor 199 is formed overlying the field oxide region 115 entirely, without blocking the floating diffusion region 130. Alternatively, however, the storage capacitor 199 also may be formed entirely over the active pixel area, or only partially over the field oxide area and partially over the active area, as desired.

[00027] It should be noted that, although the invention will be described below largely in connection with use in a four-transistor (4T) pixel cell which is depicted in Fig. 1, the invention also has applicability to a three-transistor (3T) cell as well as other configurations. The 3T cells differs from the 4T cell in the omission of a charge transfer transistor, as described further below.

[00028] Referring to Figure 1, the storage capacitor 199 electrically connected between floating diffusion region 130 and ground. Alternatively, capacitor 199 can be connected between floating diffusion region 130 and a voltage source. The four transistors illustrated in Figure 1 can be identified by their gates, as follows: transfer transistor gate 128, reset transistor gate 132, source follower transistor gate 136 and row select transistor gate 138. In the arrangement shown in Fig. 1, storage capacitor 199 amplifies signals collected by a photo diode 125.

[00029] The size of storage capacitor 199 is determined based on the color to be detected by the pixel. According to an exemplary embodiment of the present invention, the pixels form part of an imaging array based on an additive red-green-blue color space. Alternatively, other color arrangements could be utilized, such as a subtractive cyan-yellow-magenta color space.

[00030] A filter, such as Bayer filter 900 shown in Fig. 9, is arranged over the pixels. The Bayer filter pattern alternates a row of green and red filters with a row of blue and green filters. In Fig. 9, red filters 902 are designated with vertical hatching, green filters 904 are designated with left diagonal hatching, and blue filters 906 are designated with horizontal hatching. The filters provide colored light to each pixel. According to the present invention, pixels designated to detect red light are provided with a storage capacitor 199 having a small size in the range of about 0-20 femtofarads. Pixels designated to detect green light have a medium size in the range of about 2-20 femtofarads. Pixels designated to detect blue light have a large size in the range of about 3-20 femtofarads.

[00031] The structure of a pixel cell 200 of a second embodiment of the present invention is illustrated with reference to Figure 2. It should be understood that similar reference numbers correspond to similar elements as previously described with reference to Figure 1. The structure of Figure 2 differs from the above-described embodiment in that storage capacitor 299 is formed in contact with the photodiode 125 and not with the floating diffusion region 130, as in the previous embodiment. Processing of the second embodiment is similar to the processing used to produce the previous embodiment, except that a metal contact is formed that connects an electrode of the storage capacitor 299 to a doped transfer region of the photodiode, and not to the floating diffusion region 130, as in the above-described embodiment. Again, the storage capacitor 299 may be formed entirely or only partially over the field oxide region 115, as well as entirely or only partially over the active area of the pixel sensor cell. If the storage capacitor 299 is formed entirely over the field oxide region 115, the advantage is that the storage capacitor 299 improves the charge storage capacity of the imager without reducing the size of the photosensitive area.

[00032] Once again, the capacitor 299 is sized in accordance with the color of the pixel in the manner described above with reference to Fig. 1. Thus, capacitor 299, for pixels designated to detect red light, has a small size in the range of 0-20 femtofarads. In pixels designated to detect green light, capacitor 299 has a medium size in the range of about 2-20 femtofarads. In pixels designated to detect blue light, capacitor 299 has a large size in the range of 3-20 femtofarads.

[00033] Figure 3 illustrates yet another embodiment of the present invention according to which two different storage capacitors are connected to two different elements of pixel sensor cell 300. For example, Figure 3 depicts storage capacitor 399a, which is connected to the photodiode 125, and storage capacitor 399b, which is connected to the floating diffusion region 130. Both storage capacitors 399a, 399b of pixel sensor cell 300 (Figure 3) may be formed totally overlying the field oxide region 115, without reducing the photosensitive area of the pixel cell, or only partially over the field oxide region 115. Storage capacitors 399a, 399b of pixel sensor cell 300 also may be formed totally overlying the photosensitive area of the pixel cell, or only partially over the active area.

[00034] Once again, the capacitors 399a, 399b are sized in accordance with the color of the pixel in the manner described above with reference to Fig. 1. Thus, capacitors 399a, 399b for pixels designated to detect red light, have a small size combined in the range of 0-20 femtofarads. In pixels designated to detect green light, capacitor 399a, 399b have a medium size in the range of about 2-20 femtofarads. In pixels designated to detect blue light, capacitor 399a, 399b have a large size in the range of 3-20 femtofarads.

[00035] The processing for the formation of the storage capacitors 399a, 399b of pixel sensor cell 300 of Figure 3 are similar to the processing steps for the embodiment described above, except that two capacitors (and not one capacitor) are formed over the field oxide region. In addition, contact 346 (Figure 3) and contact 347 (Figure 3) connect each of the lower electrodes of the storage capacitors 399a, 399b to the doped transfer region 126 and to the floating diffusion region 130, respectively. Preferably, contacts 346, 347 are formed of a conductive material, such as doped polysilicon, or a metal such as titanium/titanium nitride/tungsten. Photolithographic techniques are used to define the

areas to be etched out to form the holes for the contacts 346, 347 wherein the conductive material is subsequently depositing therein.

[00036] Although Figure 3 illustrates only two storage capacitors 399a, 399b, it must be understood that the present invention is not limited to this embodiment. Accordingly, the invention contemplates the formation of a plurality of such storage capacitors which are formed entirely or only partially over the field oxide region, and which are further connected to various light sensitive and/or electrical elements of the pixel sensor cell. The combined capacitances of the storage capacitors is selected based on the color to be detected by the associated pixel.

[00037] Figures 4-6 illustrate additional embodiments of the present invention, according to which a storage capacitor is connected not to a ground source, as in the previous embodiments, but rather to a gate of one of the four transistors of the 4T cell. For example, Figure 4 illustrates storage capacitor 499 formed entirely or partially over the field oxide region 115, and connected to both the photodiode 125 and to the gate stack 127 of transfer transistor 128. In another exemplary embodiment, Figure 5 depicts storage capacitor 599 formed over the field oxide region 115 and also connected to both the floating diffusion region 130 and to the gate stack 127 of transfer transistor 128. According to yet another exemplary embodiment, storage capacitor 699 of Figure 6 is formed over the field oxide region 115 and is further connected to both the floating diffusion region 130 and to a gate of reset transistor 136.

[00038] Thus, capacitors 499, 599, and 699 for pixels designated to detect red light, each have a small size in the range of 0-20 femtofarads. In pixels designated to detect green light, capacitors 499, 599 and 699 have a medium size in the range of about 2-20 femtofarads. In pixels designated to detect blue light, capacitors 499, 599 and 699 have a large size in the range of 3-20 femtofarads.

[00039] Thus, capacitor 799 for pixels designated to detect red light, have a small size in the range of 0-20 femtofarads. In pixels designated to detect green light, capacitor

799 has a medium size in the range of about 2-20 femtofarads. In pixels designated to detect blue light, capacitor 799 has a large size in the range of 3-20 femtofarads.

[00040] In each of the embodiments depicted in Figures 4-6, the processing steps for the fabrication of the storage capacitors 499, 599, and 699 are similar to the processing steps used to manufacture the other embodiments, except that the upper electrode of each of the storage capacitors 499, 599, and 699 is connected not to a ground potential, as in the first embodiment, but rather to another element of the CMOS imager, for example, a gate of one of the four transistors of the pixel sensor cell, as described above.

[00041] Figure 7 illustrates yet another embodiment of the present invention, according to which a storage capacitor 799 is formed over the field oxide region 115 as part of a three-transistor (3T) cell and not a four-transistor (4T) cell, as previously described with reference to Figure 2, for example. The only difference between the structure of Figure 7 and that of Figure 2 is that the structure of Figure 2 contains an additional fourth transistor, that is transfer transistor 128. Thus, storage capacitor 799 of Figure 7 may be also formed entirely or only partially over the field oxide region 115 and connected to the photodiode 125 and the floating diffusion region 130. The processing steps for the fabrication of the storage capacitor 799 are similar to the processing steps required to manufacture the other embodiments described above, except that the storage capacitor 799 is formed by itself over the field oxide region, and not simultaneously with the transfer gate of the transfer transistor.

[00042] A typical processor system 600, which includes a CMOS image sensor 42 having an array of pixels having the construction described above as shown in Figure 8. The processor system is exemplary of a system having digital circuits which could include a CMOS image sensor. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision, vehicle navigation, video phone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

[00043] A processor system, such as a computer system, for example generally comprises a central processing unit (CPU) 644, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 646 over a bus 652. The CMOS image sensor 642 also communicates with the system over bus 652. The computer system 600 also includes random access memory (RAM) 648, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 654, and a compact disk (CD) ROM drive 656 or a flash memory card 657 which also communicate with CPU 644 over the bus 652. It may also be desirable to integrate the processor 654, CMOS image sensor 642 and memory 648 on a single IC chip.

[00044] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

[00045] It should be noted again that, although the invention has been described with specific reference to CMOS imaging circuits having a photogate and a floating diffusion region, the invention has broader applicability and may be used in any CMOS imaging apparatus. Also, although exemplary capacitor structures have been described and illustrated, many variations in capacitor structures could be made. Similarly, the processes described above are only exemplary of many that could be used to produce the invention. For example, although the invention has been described above with reference to the formation of planar capacitors, the invention also has application to other capacitor structures, such as trench capacitors, for example.

[00046] Accordingly, the above description and accompanying drawings are only illustrative of exemplary embodiments that can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is limited only by the scope of the following claims.

CLAIMS

What is claimed as new and desired to be protected is:

1. An imaging pixel comprising:

a photosensor for converting photo energy into electrical charges;

an output transistor for converting electrical charges produced by said photo sensor into an electrical signal; and

a capacitor for storing said electrical charges, wherein the size of said capacitor is associated with the color response characteristics of said imaging pixel.
2. An imaging pixel as in claim 1, wherein the color of the photosensor is red, and the storage capacity of the capacitor is between about 0 and about 20 femtofarads.
3. An imaging pixel as in claim 1, wherein the color of the photosensor is green, and the storage capacity of the capacitor is between about 2 and about 20 femtofarads.
4. An imaging pixel as in claim 1, wherein the color of the photosensor is blue, and the storage capacity of the capacitor is between about 3 and about 20 femtofarads.
5. An imaging pixel as in claim 1, wherein said storage capacitor is a flat plate capacitor.
6. An imaging pixel as in claim 5, wherein said storage capacitor is a flat plate capacitor including a first electrode, a second electrode and a dielectric layer between said first and second electrodes.

7. An imaging pixel as in claim 6, further comprising a transistor for transferring charge between said photosensor and output transistor.

8. An imaging pixel as in claim 6, wherein said second electrode of said storage capacitor is connected to a gate of said transfer transistor.

9. An imaging pixel as in claim 1, wherein said storage capacitor is connected to said charge collection region by a metal contact.

10. An imager pixel comprising:
a photosensor formed in a substrate;
a charge collection region formed in said substrate for collecting charge from said photosensor;
a charge storage capacitor electrically connected to said charge collector region, a storage capacity of the capacitor being based on the color of the photosensor.

11. An imager pixel according to claim 10, wherein said charge storage capacitor is formed fully over said field oxide region.

12. An imager pixel according to claim 10, wherein said charge storage capacitor is formed fully over said active area.

13. An imager pixel according to claim 10, wherein said charge storage capacitor is formed partially over said field oxide region.

14. An imager pixel according to claim 10, wherein said charge storage capacitor is formed partially over said active area.

15. An imager pixel according to claim 10, wherein said storage capacitor is a flat plate capacitor including a first electrode, a second electrode and an insulating layer between said first and second electrodes.

16. An imager pixel according to claim 15, wherein said transferred charge region is connected to said first electrode by an electrical contact.

17. An imager pixel according to claim 16, wherein said second electrode is further connected to a gate of a transfer transistor.

18. An imager pixel according to claim 10, further comprising a source follower transistor for outputting charge accumulated in said transferred charge region which has been transferred to said transferred charge region, wherein the gate of said source follower transistor is formed adjacent said transferred charge region.

19. An imager pixel according to claim 18, wherein said second electrode is further connected to a gate of said source follower transistor.

20. An imager pixel according to claim 10, wherein said photosensor is used in a CMOS imager.

21. A photosensor for use in an imaging device, said photosensor comprising:

a field oxide region formed in a substrate;

a doped layer of a first conductivity type formed in said substrate and adjacent said field oxide region;

a charge collection region formed in said doped layer;

a first doped region of a second conductivity type formed in said doped layer adjacent said charge collection region; and

a first storage capacitor formed over said substrate adjacent said first doped region and connected to said first doped region to store charge collected in said charge collection region, said storage capacitor being formed at least partially over at least one of said field oxide region and an active area of said photosensor;

a transferred charge region for receiving charge from said charge collection region; and

a second storage capacitor connected to said transferred charge region, a storage capacity of the capacitors being selected based on the color of the photosensor.

22. The photosensor according to claim 21, wherein said second storage capacitor is formed at least partially over at least one of said field oxide region and said active area.
23. The photosensor according to claim 21, wherein said first and second capacitors are formed entirely over said field oxide region.
24. The photosensor according to claim 21, wherein said first and second capacitors are formed entirely over said active area.
25. The photosensor according to claim 21, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

26. The photosensor according to claim 21, further comprising a source follower transistor for outputting charge accumulated in said transferred charge region which has been transferred to said transferred charge region, wherein the gate of said source follower transistor is formed adjacent said transferred charge region.
27. The photosensor according to claim 21, wherein said photosensor is used in a CMOS imager.
28. A CMOS imager system comprising:
- (i) a processor; and
 - (ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:
 - a doped layer of a first conductivity type formed in a substrate and adjacent a field oxide region;
 - a charge collection region formed in said doped layer;
 - a first doped region of a second conductivity type formed in said doped layer adjacent said charge collection region; and
 - a charge storage capacitor formed entirely over said field oxide region, a storage capacity of the capacitor being selected based on the color of the photosensor.
29. The system according to claim 28, further comprising a second doped region of a second conductivity formed in said doped layer adjacent a portion of said charge collection region and opposite said first doped region.

30. The system according to claim 29, further comprising a transfer transistor for transferring charge accumulated in said second doped region to a third doped region of said second conductivity type formed in said doped layer of said first conductivity type, wherein the gate of said transfer transistor is formed adjacent said second doped region.
31. The system according to claim 30, further comprising a source follower transistor for outputting charge accumulated in said third doped region which has been transferred to said third doped region, wherein the gate of said source follower transistor is formed adjacent said third doped region.
32. A method of forming a CMOS imager having improved charge storage comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a first doped region of a second conductivity type in said doped layer, said first doped region being adjacent a field oxide region;

forming a charge storage capacitor overlying entirely over at least one of said field oxide region and an active area of said CMOS imager; and

forming a contact between said first doped region and said charge storage capacitor, a storage capacity of the capacitor being selected based on the color of the photosensor.

33. The method according to claim 32, wherein said charge storage capacitor is formed entirely over said field oxide region.
34. The method according to claim 32, wherein said charge storage capacitor is formed entirely over said active area.

35. The method according to claim 32, wherein said charge storage capacitor is formed by:

forming a first conductive layer over said substrate including said field oxide region;

forming a dielectric layer over said first conductive layer; and

forming a second conductive layer over said dielectric layer.

36. The method according to claim 35, wherein said first electrode is a titanium nitride layer, a doped polysilicon layer or a hemispherical grained polysilicon layer.

37. The method according to claim 35, wherein said second electrode is a platinum metal layer, a tungsten metal layer, a titanium nitride layer or a doped polysilicon layer.

38. The method according to claim 35, further comprising:

forming a second doped region of said second conductivity type in the doped layer spaced from said first doped region to transfer charge from a charge collection area;

forming a third doped region of said second conductivity type in the doped layer spaced from said second doped region wherein said third doped region effectuates the transfer of charge to a readout circuit; and

forming a fourth doped region of said second conductivity type in the doped layer spaced from said third doped region wherein said fourth doped region is a drain for a reset transistor for said CMOS imager.

39. The method according to claim 38, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

40. The method according to claim 38, further comprising forming a photogate over said doped layer between said first and second doped regions.

41. A method of forming a CMOS imager having improved charge storage comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a field oxide region within said semiconductor substrate;

forming a first conductive layer over said field oxide region and said substrate;

forming an insulating layer over said first conductive layer;

forming a second conductive layer over said insulating layer;

patterning said first conductive layer, said insulating layer and said second conductive layer to form a storage capacitor and an electrical element of said CMOS imager, wherein said storage capacitor is formed entirely over and in contact with said field oxide region, a storage capacity of the capacitor being selected based on the color of the photosensor.

42. The method according to claim 41, further comprising:

forming a first doped region of a second conductivity type in said doped layer and adjacent said field oxide region;

forming a second doped region of said second conductivity type in said doped layer spaced from said first doped region;

forming a third doped region of said second conductivity type in said doped layer spaced from said second doped region and adjacent said electrical element; and

forming a fourth doped region of said second conductivity type in said doped layer spaced from said third doped region.

43. The method according to claim 42, wherein the first conductivity type is p-type, and the second conductivity type is n-type.
44. The method according to claim 43, wherein said first doped region, said second doped region, said third doped region and said fourth doped region are doped at a dopant concentration of from about 1×10^{15} ions/cm² to about 1×10^{16} ions/cm².
45. The method according to claim 44, wherein said electrical element is a transfer gate.
46. The method according to claim 45, further comprising forming a reset transistor and a source follower transistor.
47. An imaging sensor comprising:
an array of imaging pixels; and
a multi-color filter disposed over the array, whereby each pixel is developed to detect a color, wherein each pixel includes a photosensor connected to a capacitor, a size of the capacitor being determined by the respective color being detected by the pixel.
48. An imaging sensor as in claim 47, wherein the multi-color filter is a Bayer filter.
49. An imaging sensor as in claim 47, wherein pixels are developed to detect red, and each red pixel has a capacitor sized between about 0 and about 20 femtofarads.

50. An imaging sensor as in claim 47, wherein pixels are developed to detect green, and each green pixel has a capacitor sized between about 2 and about 20 femtofarads.
51. An imaging sensor as in claim 47, wherein pixels are developed to detect blue, and each blue pixel has a capacitor between about 3 and about 20 femtofarads.
52. An imaging sensor as in claim 47, wherein pixels are developed to detect one of cyan, yellow, and magenta.
53. A method of forming an imaging sensor comprising:
providing an array of imaging pixels; and
disposing a multi-color filter over the array, whereby each pixel is developed to detect a color, wherein each pixel includes a photosensor connected to a capacitor, a size of the capacitor being determined by the respective color being detected by the pixel.
54. A method of forming an imaging sensor as in claim 53, wherein the multi-color filter is a Bayer filter.
55. A method of forming an imaging sensor as in claim 53, wherein pixels are developed to detect red, and each red pixel has a capacitor sized between about 0 and about 20 femtofarads.
56. A method of forming an imaging sensor as in claim 53, wherein pixels are developed to detect green, and each green pixel has a capacitor sized between about 2 and about 20 femtofarads.

57. A method of forming an imaging sensor as in claim 53, wherein pixels are developed to detect blue, and each blue pixel has a capacitor between about 3 and about 20 femtofarads.
58. A method of forming an imaging sensor as in claim 53, wherein pixels are developed to detect one of cyan, yellow, and magenta.