

RF POWER AMPLIFIER WITH DISTRIBUTED BIAS CIRCUIT

TECHNICAL FIELD OF THE INVENTION

The present invention relates to power amplifiers, and in particular to an RF power
5 amplifier with a distributed bias circuit.

BACKGROUND OF THE INVENTION

In the field of bipolar radiofrequency (RF) power amplifiers, the biasing of the
amplifying transistor(s) is crucial in determining the class of operation and the linearity of
amplifier response. Various conventional biasing schemes for such amplifiers are known.
10 These biasing schemes must typically balance competing considerations such as linearity,
noise figure, distortion and power consumption.

It is well known that a bipolar transistor is subject to thermal instability and
runaway if it is not properly biased. Thus, in power amplifiers, amplifying transistors are
commonly ballasted for thermal stability by applying degeneration (ballast resistors) in the
15 base and/or emitter DC current paths.

While base ballast resistors provide thermal stability, they can adversely affect
amplifier performance. A base ballast resistor must be relatively large to provide adequate
temperature compensation. As input signal power is increased, the large resistance in the
base DC path reduces the amount of power available at the amplifier output. As a result, a
20 base-ballasted amplifier exhibits non-linear response.

A distributed base bias circuit is described in U.S. Patent No. 5,150,076, entitled
“Emitter-Grounded Amplifier Circuit With Bias Circuit.” This active bias scheme
eliminates some of the disadvantages of base ballast resistors. However, the scheme
described in that patent exhibits undesirable thermal characteristics. Moreover, the
25 device’s sensitivity to supply voltage fluctuations requires a relatively high supply voltage

to be used, making the amplifier less suitable for portable applications such as cellular telephones.

SUMMARY OF THE INVENTION

Therefore, a need has arisen for an RF power amplifier that addresses the
5 disadvantages and deficiencies of the prior art. In particular, a need has arisen for an RF power amplifier with a robust, thermally compensated biasing scheme.

Accordingly, an improved amplifier circuit is disclosed. In one embodiment, the amplifier circuit includes an amplifier transistor that has a base terminal connected to receive an input signal. The amplifier transistor amplifies the input signal to generate an
10 output signal. A reference voltage source generates a reference voltage at a reference voltage output node. A local bias circuit provides a bias voltage to the base terminal of the amplifier transistor. The local bias circuit includes a first transistor that has an emitter terminal coupled to the reference voltage output node, a collector terminal coupled to a supply voltage node, and a base terminal connected to the collector terminal. The local
15 bias circuit also includes a second transistor that has a base terminal coupled to the base terminal of the first transistor, a collector terminal coupled to the supply voltage node, and an emitter terminal coupled to the base terminal of the amplifier transistor.

An advantage of the present invention is that a robust, thermally compensated bias voltage is provided to any number of amplifier cells. Another advantage of the present
20 invention is that the bias circuit is ballasted to prevent thermal runaway in any one of the amplifier cells.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and for further features and advantages, reference is now made to the following description taken in
25 conjunction with the accompanying drawings, in which:

FIGURE 1 is a block diagram of an RF power amplifier;

FIGURE 2 is a schematic diagram in partial block form of an amplifier circuit using a distributed bias arrangement in accordance with the present invention;

FIGURE 3 is a schematic diagram of a reference voltage source for use in the amplifier circuit;

5 FIGURE 4 is a schematic diagram of an alternative reference voltage source for use in the amplifier circuit; and

FIGURE 5 is a schematic diagram of another alternative reference voltage source for use in the amplifier circuit.

DETAILED DESCRIPTION OF THE INVENTION

10 The preferred embodiments of the present invention and their advantages are best understood by referring to FIGURES 1 through 5 of the drawings. Like numerals are used for like and corresponding parts of the various drawings.

Referring to FIGURE 1, a block diagram of an RF power amplifier 10 is shown. RF power amplifier 10 may reside on a single integrated circuit chip, such as a gallium
15 arsenide integrated circuit chip. RF power amplifier 10 receives an RF input signal RF_{IN} and generates an RF output signal RF_{OUT} . RF power amplifier 10 has a first amplifier stage 12 which provides an initial amplification of the RF input signal RF_{IN} . This amplified signal is provided to a second amplifier stage 14. In order to drive the output signal RF_{OUT} with sufficient power, amplifier stage has a plurality of amplifier cells 16
20 connected in parallel.

Referring to FIGURE 2, a schematic diagram in partial block form of an amplifier circuit 18 using a distributed bias arrangement is shown. Amplifier circuit 18 is a multi-cellular amplifier circuit which may be used as the second amplifier stage 14 of RF power amplifier 10.

25 Amplifier circuit 18 includes a reference voltage source 20 which supplies a reference voltage to a set of individually biased amplifier cells 22. As described below, in

one embodiment reference voltage source 20 provides a reference voltage approximately equal to one transistor threshold voltage. While only two amplifier cells 22 are shown in FIGURE 2 for purposes of illustration, it will be understood that amplifier circuit 18 may include any number of amplifier cells 22. Amplifier cells 22 may be identical in structure.

5 Each amplifier cell 22 receives the RF input signal RF_{IN} for amplifier circuit 18. The input signal RF_{IN} is provided to the base of an amplifying transistor 24. The collectors of the amplifying transistors 24 from the various amplifier cells 22 may be connected together to provide an output signal RF_{OUT} .

A local bias circuit 26 receives the reference voltage from reference voltage source
10 20 and generates a bias voltage at the base of amplifying transistor 24. Because the amplifying transistor 24 of each amplifier cell 22 is individually biased, a DC blocking capacitor 28 provides DC isolation at the input of each amplifier cell 22. An optional sense resistor R_{SENSE} may be connected between the base of amplifying transistor 24 and reference voltage source 20. This sense resistor may provide additional control of the
15 amplifier base bias voltage, as will be described below.

Each amplifier cell 22 includes an emitter ballast resistor 30 connected between the emitter of amplifying transistor 24 and ground. Emitter ballast resistor 30 provides thermal stabilization for the amplifier cell 22. As is well known to those of skill in the art, a base ballast resistor (not shown) may be connected between the base of amplifying
20 transistor 24 and local bias circuit 26. This base ballast resistor also provides thermal stabilization, and may be used instead of or in addition to emitter ballast resistor 30. However, as will be described below, due to the ballasting features of local bias circuit 26, a base ballast resistor is unnecessary and emitter ballast resistor 30 may have a very small resistance or may be eliminated entirely.

25 The local bias circuit 26 of each amplifier cell includes a first transistor 32 with an emitter coupled to the output of reference voltage source 20 via a resistor 34. The base

and collector of transistor 32 are connected together, and both are coupled to a supply voltage V_{CC} via a resistor 36. A second transistor 38 has its base connected to the base and collector of transistor 32. The collector of transistor 38 is connected to V_{CC} . The emitter of transistor 38 is coupled to the base of amplifying transistor 24. A base ballast resistor (not shown) may optionally be connected between the emitter of transistor 38 and the base of amplifying transistor 24. Alternatively, the emitter of transistor 38 may be directly connected to the base of amplifying transistor 24, as shown in FIGURE 2.

The operation of local bias circuit 26 is as follows. Transistor 32 is configured as a level shifter. Thus, resistors 34 and 36 determine the voltage at the base of transistor 32. This voltage is provided to the base of transistor 38, which acts as an emitter follower. The voltage at the emitter of transistor 38 is provided as a base bias voltage to amplifying transistor 24.

An increase in temperature of transistor 38 would, if uncompensated, decrease the base-emitter voltage drop of transistor 38, thereby increasing the base bias voltage of amplifying transistor 24. However, transistor 32 is matched to transistor 38 and experiences the same V_{be} decrease as transistor 38. Thus, because transistors 32 and 38 are located in physical (thermal) proximity to each other, the V_{be} decrease of transistor 38 is offset by a decrease in base voltage of transistor 32. In this manner, local bias circuit 26 is automatically thermally compensated to produce the same bias voltage at different temperatures.

A further ballasting effect is provided by resistors 34 and 36. When increased bias current is drawn by amplifying transistor 24, the base current of transistor 38 also increases. This increased base current is drawn from the base and collector of transistor 32, thereby decreasing the current through transistor 32 and resistor 34 without decreasing the current through resistor 36. This current change affects the voltage dividing characteristics of resistors 34 and 36 and transistor 32, causing the voltage at the base of

transistors 32 and 38 to drop. The decreasing base voltage of transistor 38 causes a decrease in the bias voltage provided to amplifying transistor 24, thereby counteracting the increase in current drawn by amplifying transistor 24.

As will be apparent to those skilled in the art, the sizes of resistors 34 and 36
5 determine the amount of ballasting provided by local bias circuit 26. Larger resistors 34 and 36 increase the ballasting effect. However, resistor 34 also limits the previously-described ability of transistor 32 to compensate for a thermally-induced drop in V_{be} for transistor 38. Thus, the size of resistor 34 must be chosen to achieve an appropriate compromise of these two features.

10 Referring to FIGURE 3, a schematic diagram of a reference voltage source 40 for use in amplifier circuit 18 is shown. As described below, reference voltage source 40 is capable of generating a robust, stable reference voltage V_{REF} at the base of a bipolar transistor 41. Since transistor 41 has a grounded emitter, reference voltage V_{REF} is approximately one threshold voltage above ground.

15 The collector of transistor 41 is connected to the supply voltage V_{CC} through two resistors 42 and 44. The emitter of a transistor 46 is connected to a node 43 between resistors 42 and 44. Transistor 46 is connected in a diode configuration in series with a resistor 48, which is in turn connected to V_{CC} . Another transistor 50 has its base connected to the base of transistor 46 in an emitter follower configuration. Transistor 50
20 has its collector connected to V_{CC} and its emitter connected to the base of transistor 41. Transistors 41, 46 and 50 may be, for example, heterojunction bipolar transistors (HBTs).

The operation of reference voltage source 40 is as follows. With no load connected to V_{REF} , reference voltage source 40 establishes steady-state value of V_{REF} at the threshold voltage of transistor 41. When a load draws current from the base of
25 transistor 41, a resulting voltage sag will decrease the current through transistor 41, thereby raising the voltage at node 43. Transistor 46 acts as a level shifter, providing a

voltage to the base of transistor 50 that is one threshold voltage above the voltage at node 43. Thus, a voltage increase at node 43 causes a voltage increase at the base of transistor 50. The increase in base voltage and the decrease in V_{REF} cause transistor 50 to conduct more current, counteracting the voltage sag in V_{REF} .

5 This negative feedback loop provides a great deal of stability for V_{REF} . The responsiveness of the feedback loop is determined primarily by the values of resistors 42 and 44, the beta values of transistors 41 and 50 and the voltage difference between V_{CC} and the collector of transistor 41. For maximum responsiveness, resistor 44 has a small resistance compared to that of resistor 42. In one embodiment, resistor 44 may be omitted
10 entirely ($R = 0$). In this embodiment, optional sense resistor R_{SENSE} shown in FIGURE 2 is not used.

Referring to FIGURE 4, a schematic diagram of an alternative reference voltage source 60 for use in amplifier circuit 18 is shown. Reference voltage source 60 may be used in conjunction with the optional sense resistor R_{SENSE} of amplifier circuit 18
15 (FIGURE 2) to provide further stabilization of the base bias voltage of amplifying transistor 24.

Reference voltage source 60 is similar in structure to reference voltage source 40 described above. Reference voltage source 60 operates in the same manner as reference voltage source 40 described above, except that transistor 62 receives its base voltage from
20 the base of amplifying transistor 24 via sense resistor R_{SENSE} . Thus, the feedback path for reference voltage source 60 includes local bias circuit 26. Since transistor 62 senses the base bias voltage of amplifying transistor 24 rather than reference voltage V_{REF} , imperfect voltage buffering by local bias circuit 26 (for example due to thermal variation) may be compensated for at reference voltage source 60. Reference voltage source 60 therefore
25 provides additional stabilization of the base bias voltage of amplifier circuit 18.

Referring to FIGURE 5, a schematic diagram of another alternative reference voltage source 70 for use in amplifier circuit 18 is shown. Reference voltage source 70 may be used in conjunction with the optional sense resistor R_{SENSE} of amplifier circuit 18 (FIGURE 2) to provide stabilization of the base bias voltage of amplifying transistor 24.

5 Reference voltage source 70 is somewhat similar in design to reference voltage source 60 described above. Reference voltage source 70 operates in the same manner as reference voltage source 60 described above, except that the node 73 between resistors 72 and 74 sets the reference voltage V_{REF} directly, without the use of further level-shifting circuitry. Reference voltage source 70 therefore has a smaller, simpler circuit design than
10 reference voltage source 60. Like reference voltage source 60, reference voltage source 70 receives feedback through local bias circuit 26 and sense resistor R_{SENSE} to provide bias voltage stabilization for amplifier cells 22.

Referring to FIGURE 2, sense resistor R_{SENSE} is connected to the base of only one amplifier transistor 24 of amplifier circuit 18. Thus, thermal variation among the amplifier
15 cells 22 will not be taken into account in reference voltage sources 60 or 70 described above. However, the ballasting effect of local bias circuit 26, which prevents thermal runaway, ensures that the amplifier cells 22 will have approximately the same temperature. Thus, reference voltage sources 60 and 70 provide excellent bias voltage stabilization for all amplifier cells 22.

20 Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

We claim:

1. An amplifier circuit comprising:
an amplifier transistor having a base terminal connected to receive an input signal,
5 the amplifier transistor being operable to amplify the input signal to generate an output signal;
a reference voltage source operable to generate a reference voltage at a reference voltage output node; and
a local bias circuit operable to provide a bias voltage to the base terminal of the
10 amplifier transistor, the local bias circuit having:
a first transistor having an emitter terminal coupled to the reference voltage output node, the first transistor having a collector terminal coupled to a supply voltage node, the first transistor having a base terminal connected to the collector terminal; and
15 a second transistor having a base terminal coupled to the base terminal of the first transistor, the second transistor having a collector terminal coupled to the supply voltage node, the second transistor having an emitter terminal coupled to the base terminal of the amplifier transistor.
2. The amplifier circuit of claim 1, wherein the local bias circuit further
20 comprises a first resistor having a first terminal connected to the supply voltage node, the first resistor having a second terminal connected to the collector terminal of the first transistor.
3. The amplifier circuit of claim 1, wherein the local bias circuit further
comprises a second resistor having a first terminal connected to the reference voltage
25 output node, the second resistor having a second terminal connected to the emitter terminal of the first transistor.

4. The amplifier circuit of claim 1, wherein the amplifier transistor comprises a first amplifier transistor, and wherein the local bias circuit comprises a first local bias circuit, the amplifier circuit further comprising:

5 a second amplifier transistor having a base terminal connected to receive the input signal, the second amplifier transistor being connected in parallel with the first amplifier transistor to generate the output signal; and

a second local bias circuit operable to provide a bias voltage to the base terminal of the second amplifier transistor, the second local bias circuit having:

10 a third transistor having an emitter terminal coupled to the reference voltage output node, the third transistor having a collector terminal coupled to the supply voltage node, the third transistor having a base terminal connected to the collector terminal of the third transistor; and

15 a fourth transistor having a base terminal coupled to the base terminal of the third transistor, the fourth transistor having a collector terminal coupled to the supply voltage node, the fourth transistor having an emitter terminal coupled to the base terminal of the amplifier transistor.

5. The amplifier circuit of claim 1, wherein the reference voltage source comprises:

20 a fifth transistor having a base terminal coupled to the reference voltage output node and an emitter terminal coupled to ground;

a third resistor having a first terminal coupled to the supply voltage node, the third resistor having a second terminal coupled to a collector terminal of the fifth transistor;

25 a sixth transistor having an emitter terminal coupled to the collector terminal of the fifth transistor, the sixth transistor having a collector terminal coupled to the supply voltage node, the sixth transistor having a base terminal connected to the collector terminal of the sixth transistor; and

a seventh transistor having a base terminal coupled to the base terminal of the sixth transistor, the seventh transistor having a collector terminal coupled to the supply voltage node, the seventh transistor having an emitter terminal coupled to the reference voltage output node.

5 6. The amplifier circuit of claim 1, further comprising a sense resistor having a first terminal coupled to the base terminal of the amplifier transistor, wherein the reference voltage source comprises:

a eighth transistor having a base terminal coupled to a second terminal of the sense resistor and an emitter terminal coupled to ground;

10 a fourth resistor having a first terminal coupled to the supply voltage node, the fourth resistor having a second terminal coupled to a collector terminal of the eighth transistor;

a ninth transistor having an emitter terminal coupled to the collector terminal of the eighth transistor, the ninth transistor having a collector terminal coupled to the supply voltage node, the ninth transistor having a base terminal connected to the collector terminal of the ninth transistor; and

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a tenth transistor having a base terminal coupled to the base terminal of the ninth transistor, the tenth transistor having a collector terminal coupled to the supply voltage node, the tenth transistor having an emitter terminal coupled to the reference voltage output node.

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7. The amplifier circuit of claim 1, further comprising a sense resistor having a first terminal coupled to the base terminal of the amplifier transistor, wherein the reference voltage source comprises:

an eleventh transistor having a base terminal coupled to a second terminal of the sense resistor, the eleventh transistor having an emitter terminal coupled to ground and a collector terminal coupled to the reference voltage output node;

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a fifth resistor having a first terminal coupled to the supply voltage node, the fourth resistor having a second terminal coupled to the reference voltage output node.

8. The amplifier circuit of claim 1, wherein the reference voltage source further comprises a sixth resistor connected between the reference voltage output node and
5 the collector terminal of the eleventh transistor.

9. A bias voltage generating circuit comprising:

a reference voltage source operable to generate a reference voltage at a reference voltage output node; and

a local bias circuit operable to generate a bias voltage at a bias node, the local bias
10 circuit having:

a first transistor having an emitter terminal coupled to the reference voltage output node, the first transistor having a collector terminal coupled to a supply voltage node, the first transistor having a base terminal connected to the collector terminal of the first transistor; and

15 a second transistor having a base terminal coupled to the base terminal of the first transistor, the second transistor having a collector terminal coupled to the supply voltage node, the second transistor having an emitter terminal coupled to the bias node.

10. The bias voltage generating circuit of claim 9, wherein the local bias circuit
20 comprises a first local bias circuit, the distributed bias voltage generating circuit further comprising a second local bias circuit operable to provide a second bias voltage to a second bias node, the second local bias circuit having:

a third transistor having an emitter terminal coupled to the reference voltage output node, the third transistor having a collector terminal coupled to the supply voltage node,
25 the third transistor having a base terminal connected to the collector terminal of the third transistor; and

a fourth transistor having a base terminal coupled to the base terminal of the third transistor, the fourth transistor having a collector terminal coupled to the supply voltage node, the fourth transistor having an emitter terminal coupled to the second bias node.