

ABSTRACT

A memory device, includes a first memory cell, and a second memory cell adjacent to the first memory cell; and a sequencer configured to, when data is read from the first memory cell:

5 perform a first read operation on the second memory cell;
perform a second read operation on the first memory cell;
perform a third read operation on the first memory cell by
applying a voltage different from that applied in the second
read operation to a gate of the second memory cell; and generate

10 first data stored in the first memory cell and second data for
correcting the first data, based on results of the first to third
read operations.