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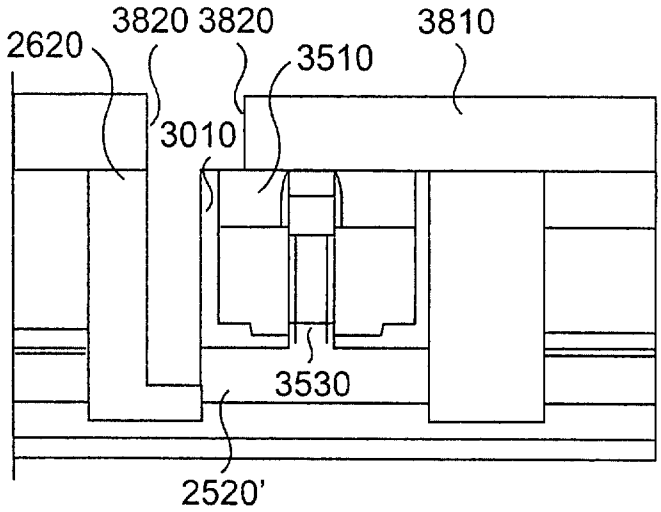
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(54) Title: VERTICAL DUAL GATE FIELD EFFECT TRANSISTOR



(57) Abstract: A vertical transistor particularly suitable for high density integration includes potentially independent gate structures (3230) o opposite sides of a semiconductor pillar (2910) formed by etching in a trench. The gate structure is surrounded by insulting material (2620) which is selectively etchable to isolation material surrounding the transistor. A contact (3820) is made to the lower end of the pillar by selectively etching the isolation material selective to the insulating material. The upper end of the pillar is covered by a cap (2730) and sidewalls of selectively etchable materials so that gate and source connection openings (3720, 3620) can also be made by selective etching with good registration tolerance.

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