MULTI-CHIP CHIP-SCALE INTEGRATED CIRCUIT PACKAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention:

This invention relates to integrated circuit (IC) packaging technology, and more particularly, to a multi-chip chip-scale IC package that can pack two chips therein and with its overall size being only slightly larger than the size of the chips enclosed in it.

2. Description of Related Art:

The fabrication of integrated circuit (IC) products includes three stages: (1) preparing a semiconductor wafer; (2) forming circuit components, such as metal-oxide semiconductor transistors and multi-level interconnects, on the wafer; and (3) packaging the fabricated chips. The primary goal of the packaging technology is aimed at making the overall size of the resulting IC package as small as possible. Conventional packaging techniques that can achieve this goal include, for example, the Chip Scale Package (CSP) and the Multi-Chip Module (MCM) technologies. In the submicron level of fabrication at 0.18 μm or below, the size the IC package is a primary concern to provide high integration. To increase integration, an IC package now typically packs two or more chips, rather than just one chip, therein. Such an IC package is customarily referred to as a multi-chip IC package. A multi-chip IC package can either pack a processor chip and a memory chip (such as a DRAM chip or a flash memory chip) together therein, or a logic chip and a memory chip together therein. The use of multi-chip IC

packaging technology not only helps reduce manufacturing cost, but also helps reduce the signal transmission path between the chips and the external circuitry to allow an increased performance of the chips without additional particular assembling process. The multi-chip IC packaging technology may also be applied to a multi-chip system with variable functions and operation frequencies, for example,

1. A system comprises memory chips, microprocessors, resistors, capacitors, and inductors.

2. A system comprises memory chips (DRAM), logic circuit chips, and memory chips (Flash memory),

3. A system comprises analog chips, logic circuit chips, memory chips (including DRAM, SRAM, Flash memory), resistor, capacitor, and inductor.

FIG. 1 is a schematic, cross-sectional diagram of a conventional IC package that is packaged by the MCM technology. This kind of IC package is customarily referred to as a multi-chip IC package. As shown, this IC package is constructed on a substrate 10 which is a multi-level PCB. A plurality of chips 12 is mounted on the substrate 10 by means of insulating glue 14. A wire bonding technique is used to electrically connect the chips 12 via a plurality of bonding wires 16 to a plurality of connecting points (not shown) on the substrate 10. Alternatively, a flip-chip or controlled collapse chip connection technique (C4) can be used to electrically connect the chips 12 to the substrate 10 by means of conductive bumps (not shown). After the chips 12 are mounted in position on the substrate 10, a resin compound 18 is formed to hermetically enclose the chips 12. After this, a plurality of tin balls 20 are arranged by using the Ball Grid Array

(BGA) technology on the bottom side of the substrate 10. These tin balls 20 are used to bond and electrically connect the resulting IC package to a circuit board (not shown).

One drawback to the multi-chip IC package of FIG. 1, however, is that its overall size is considerably large due to the fact that the chips 12 are arranged in a side-by-side manner in the same plane. Moreover, the signal transmission path is quite lengthy between the chips 12 and the external circuitry that is connected via the tin balls 20. The use of the C4 technology, although capable of package size reduction, would nevertheless make the testing difficult to carry out due to the reason that the Known Good Die (KGD) technology should be additionally used. A low yield and a high cost are thus resulted. The use of the KGD technology would considerably increase the packaging cost.

A solution to reduce the size of a multi-chip IC package is disclosed in U.S. Patent No. 5,331,235, which arranges the chips in a face-to-face manner that allows the overall package size to be considerably reduced. The disclosed package structure is here schematically illustrated in FIG. 2. As shown, this face-to-face type of multi-chip IC package is designed to pack two chips 30, 32 therein, which are arranged in a face-to-face manner by using the Tape Automatic Bonding (TAB) technology. The Inner Lead Bonding (ILB) process for the two chips 30, 32 is carried out by the use of conductive bumps 34, 36 to bond and electrically connect the bonding pads (not shown) on the chips 30, 32 to corresponding points on a film carrier 38; while the Outer Lead Bonding (OLB) process is carried out by connecting the film carrier 38 to a leadframe 40. Furthermore, a tin ball 42 is arranged between the two chips 30, 32 to interconnect the two chips 30, 32. Finally, a resin compound 44 is formed to hermetically enclose the whole

of the two chips 30, 32, the whole of the film carrier 38, and part of the leadframe 40. This completes the packaging of the chips 30, 32 into an IC package.

One drawback to the foregoing multi-chip IC package of FIG. 2, however, is that the use of the TAB technology would considerably lengthen the signal transmission path between the chips 30, 32 and the external circuitry (not shown). Moreover, the use of the resin compound 44 to enclose the chips 30, 32 would cause the overall size of the resulting IC package to be considerably large, making the IC package less compact and less effective in heat dissipation.

SUMMARY OF THE INVENTION

The present invention to provides a multi-chip chip-scale IC package, whose size is only slightly larger than the chips that are enclosed therein.

The signal transmission path between the enclosed chips and the external circuitry is reduced as compared to the prior art. In addition, an increased heat-dissipating efficiency as compared to the prior art.

Moreover, the multi-chip chip-scale IC package provided in the invention can be tested directly during the packaging process without having to use the KGD technology as in the case of the prior art.

A multi-chip chip-scale IC package is provided. By the invention, two chips are mounted in a face-to-face manner on a film carrier by using the flip-chip or controlled collapse chip connection technique in which conductive bumps are used to bond and electrically connect the two chips to the corresponding conductive wires on the insulating film. Furthermore, an insulating compound is formed from an insulating material

filled between the two chips in such a manner as to cover the component surfaces of the two chip, while uncovering the backs of the same. This arrangement allows the signal transmission path between the chips and the external circuitry to be shorter than the prior art, thus increasing the performance of the chips.

Moreover, the multi-chip chip-scale IC package of the invention can be mounted on a circuit board to constitute an IC board that allows a higher heat-dissipating efficiency by coupling the back of one chip to a printed circuit line on the circuit board and the back of the other chip to a heat-dissipating device. Furthermore, the insulating film can be optionally formed with a plurality of securing openings which are filled with the insulating material when forming the insulating compound to help secure the insulating compound more tightly to the film carrier. Thus, an improved packaging quality and an enhanced reliability are obtained.

BRIEF DESCRIPTION OF DRAWINGS

The invention can be more fully understood by reading the following detailed description of the preferred embodiments, with reference made to the accompanying drawings, wherein:

FIG. 1 is a schematic, cross-sectional diagram of a conventional Multi-Chip Module IC package;

FIG. 2 is a schematic, cross-sectional diagram of a conventional face-to-face type of multi-chip IC package;

FIG. 3 is a schematic, cross-sectional diagram of the multi-chip chip-scale IC package of the invention;

FIGs. 4A-4D are schematic diagrams respectively showing the various kinds of film carriers that can be utilized in the multi-chip chip-scale IC package of the invention;

FIG. 5 is a schematic, cross-sectional diagram of the IC package of the invention when utilizing the type of film carrier shown in FIG. 4D; and

FIG. 6 is a schematic, cross-sectional diagram showing the mounting of the multi-chip chip-scale IC package of the invention on a circuit board.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A multi-chip IC packaging process typically includes three stages: (1) selecting a suitable carrier; (2) electrically connecting the chips to the selected carrier; and (3) performing a compound molding process to form an insulating compound to enclose the chips. In the first stage, the carrier can be either a leadframe, a film carrier, or a printed circuit board (PCB). In the case of using the TAB technology, it is preferable to use a film carrier. In the second stage, the technique used can be the wire-bonding technique, or TAB technique, or flip-chip or controlled collapse chip connection (C4) technique. In the third stage, resin or ceramic is used to form the insulating compound to hermetically enclose the chips in the IC package.

FIG. 3 is a schematic, cross-sectional diagram of the multi-chip chip-scale IC package of the invention. In this preferred embodiment, the multi-chip, chip-scale IC package is used to pack two chips 50, 52 therein, whose overall size is only slightly larger than the chips 50, 52 packed therein. The chips 50, 52 are substantially equal in size and can be any kinds of integrated circuits, such as DRAM (dynamic random-

access memory) chips, ROM (read-only memory) chips, logic circuit chips, and analog circuit chips. In accordance with the invention, a film carrier 58, which is composed of an insulating film 54 and a plurality of conductive wires 56, is used to mount the chips 50, 52.

The first chip 50 has a component surface 60 on which various circuit components (not shown) are formed; and the second chip 52 has a component surface 62 on which various circuit components (not shown) are formed. The two chips 50, 52 are arranged in a face-to-face manner, with the component surface 60 of the first chip 50 facing the component surface 62 of the second chip 52. A plurality of first conductive bumps 64 are provided on the component surface 60 of the first chip 50, each being bonded and electrically connected to one of the bonding pads (not shown) on the component surface 60 of the first chip 50; and similarly, a plurality of second conductive bumps 66 are provided on the component surface 62 of the second chip 52, each being bonded and electrically connected to one of the bonding pads (not shown) on the component surface 62 of the second chip 52. The component surface 60 of the first chip 50 and the component surface 62 of the second chip 52 are arranged, faceface-to-face, on opposite sides of the film carrier 58, with the bonding pads (not shown) of the two chips 50, 52 being electrically connected via the first and second conductive bumps 64, 66 to the conductive wires 56 on the film carrier 58.

In the compound molding process, an insulating material, such as epoxy, fills the void space between the two chips 50, 52 to thereby form an insulating compound 68. It is a characteristic feature of the invention that the insulating compound 68 is formed in such a manner as to enclose only the conductive bumps 64, 66 and the component sur-

faces 60, 62 of the two chips 50, 52, but uncovering the back 70 of the first chip 50 and the back 72 of the second chip 52. This completes the assembly of the multi-chip chip-scale IC package. As illustrated in FIG. 3, the resulting IC package is quite small in height, making the overall package size very compact. Moreover, the uncovered backs 70, 72 of the chips 50, 52 can facilitate the heat-dissipation from the chips 50, 52.

By the invention, the signal transmission path between the chips 50, 52 and the external circuitry (not shown) include only the conductive wires 56 and the conductive bumps 64, 66, which is considerably shorter than the prior art. The subsequent process to bend the conductive wires 56 and the mounting of the completed IC package on a circuit board (not shown) through Surface Mount Technology (SMT) are all conventional techniques, so description thereof will not be further detailed.

Various types of film carriers can be used to implement the film carrier 58 in the IC package of the invention shown in FIG. 3, which are respectively depicted in FIGs. 4A-4D.

Referring to FIG. 4A, the first example of the film carrier 58 is a long-lead, cantilever-type of film carrier, which is composed of an insulating film 54 on which a plurality of conductive wires 56, such as copper wires, are arranged. To facilitate automatic packaging, the insulating film 54 is further formed with two rows of guide holes 80 on the edges thereof. The conductive wires 56 each have the outer lead thereof attached to the insulating film 54.

Referring to FIG. 4B, the second example of the film carrier 58 differs from the first example of FIG. 4A only in that a free-floating ring 82 is provided to support the

inner-lead portions of the conductive wires 56. The provision of this free-floating ring 82 can help hold the conductive wires 56 more securely in position.

Referring to FIG. 4C, the third example of the film carrier 58 differs from the previous two examples of FIGs. 4A and 4B only in that a corner-supported ring 84 is provided to support the inner-lead portions of the conductive wires 56. This corner-supported ring 84 differs from the free-floating ring 82 shown in FIG. 4B in that the corner-supported ring 84 is linked to the insulating film 54 while the free-floating ring 82 shown in FIG. 4B is not. The provision of the corner-supported ring 84 can help hold the conductive wires 56 more securely in position.

Referring to FIG. 4D, the fourth example of the film carrier 58 is designed in accordance with the invention specifically for the purpose of strengthening the fixture of the insulating compound 68 to the film carrier 58. The fourth example of the film carrier 58 is substantially identical in structure to the third example shown in FIG. 4C except that a plurality of securing openings 86 are formed in the corner-supported ring 84. These securing openings 86 can be any shape, such as a cross, a circle, or a square. In the embodiment of FIG. 4D, for example, the securing openings 86 are shaped like a cross.

FIG. 5 is a schematic, cross-sectional diagram of the IC package of the invention when utilizing the fourth example of film carrier 58 shown in FIG. 4D. In FIG. 4D, the area enclosed by the dashed box indicated by the reference numeral 88 is the area that is to be enclosed by the insulating compound 68. When the insulating material fills this area 88 to form the insulating compound 68, it also fills into the securing openings 86 in the corner-supported ring 84, thereby allowing the resulting insulating compound 68 to

be highly secured to the film carrier 58. The secured compound 68 further allows the chips 50, 52 enclosed therein to be highly secured in position.

FIG. 6 is a schematic, cross-sectional diagram showing the mounting of the multi-chip chip-scale IC package of the invention on a circuit board 100 to constitute an IC board. The circuit board 100 is composed of a substrate 102 and a plurality of printed circuit lines 104, 106 on the substrate 102. The substrate 102 can be, for example, a multi-level PCB substrate. In accordance with the invention, the multi-chip chip-scale IC package is mounted on the circuit board 100 by connecting the conductive wires 56 on the film carrier 58 to the printed circuit line 104 on the circuit board 100 through, for example, the Surface Mount Technology (SMT). Moreover, the back 72 of the second chip 52 is arranged in such a manner as to come into contact with the printed circuit line 106 which is connected to a grounded line (not shown), thereby providing the IC package with a heat-dissipating path via the back 72 of the second chip 52 to the ground. In addition, a heat-dissipating device 108 can be mounted on the back 70 of the first chip 50 to provide another heat-dissipating path. Therefore, the heat-dissipation efficiency of the multi-chip chip-scale IC package of the invention is considerably better than the prior art.

Another benefit of the invention is that, since the invention is based on a film carrier, it can be tested directly during the packaging process without having to use the KGD technology as in the case of the prior art. Therefore, the manufacturing cost for the multi-chip chip-scale IC package of the invention can be reduced.

In conclusion, the multi-chip chip-scale IC package of the invention has the following advantages over the prior art.

First, the invention allows the overall size of the multi-chip chip-scale IC package to be only slightly larger than the size of the chips enclosed therein, thus allowing the IC package to be made very compact.

Second, the invention allows the signal transmission path between the chips and the external circuitry to be shorter than in the prior art, thus increasing the performance of the chips.

Third, the invention allows a higher heat-dissipating efficiency by exposing the backs of the chips in the IC package and being arranged in such a manner that the back of one chip is coupled to a printed circuit line on the circuit board, while the back of the other chip is coupled to a heat-dissipating device.

Fourth, the invention allows the testing of the resulting IC package to be carried out during the packaging process without having to use the KGD technology. The manufacturing cost of the multi-chip chip-scale IC package of the invention is therefore reduced as compared to the prior art.

The invention has been described using exemplary preferred embodiments. However, it is to be understood that the scope of the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements. The scope of the claims, therefore, should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

CLAIMS



What is claimed is:

1. A multi-chip, chip-scale IC package, which comprises:

a film carrier which is composed of an insulating film and a plurality of conductive wires mounted on the insulating film;

a first chip which is electrically connected by means of a plurality of first conductive bumps to corresponding conductive wires on the insulating film;

a second chip which is electrically connected by means of a plurality of second conductive bumps to corresponding conductive wires on the insulating film; wherein the second chip is arranged in a face-to-face manner with the first chip, on opposite sides of the insulating film; and

an insulating compound formed from an insulating material between the first and second chips in such a manner as to cover the component surfaces of the first and second chips while uncovering the backs of the same.

2. The multi-chip chip-scale IC package of claim 1, wherein the film carrier is of the type having a free-floating ring for supporting the inner-lead portions of the conductive wires.

3. The multi-chip chip-scale IC package of claim 1, wherein the film carrier is of the type having a corner-supported ring for supporting the inner-lead portions of the conductive wires.

4. The multi-chip chip-scale IC package of claim 3, wherein the insulating film is formed with at least one secured opening which is filled with the insulating material

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when forming the insulating compound to help secure the insulating compound to the film carrier.

5. The multi-chip chip-scale IC package of claim 1, wherein, when the multi-chip chip-scale IC package is mounted on a circuit board, the back of the second chip comes into contact with a printed circuit line on the circuit board.

6. The multi-chip, chip-scale IC package of claim 5, wherein the back of the first chip is mounted with a heat-dissipating device.

7. An IC board, which comprises:

a substrate;

a plurality of printed circuit lines formed over the substrate;

a multi-chip, chip-scale IC package mounted on the substrate, the multi-chip, chip-scale IC package including:

a film carrier which is composed of an insulating film and a plurality of conductive wires mounted on the insulating film, the conductive wires being electrically connected to corresponding ones of the printed circuit lines on the substrate;

a first chip which is electrically connected by means of a plurality of first conductive bumps to corresponding conductive wires on the insulating film;

a second chip which is electrically connected by means of a plurality of second conductive bumps to corresponding conductive wires on the insulating film, wherein the second chip is arranged in a face-to-face manner with the first chip on opposite sides of the insulating film; and



an insulating compound formed from an insulating material between the first and second chips in such a manner as to cover the component surfaces of the first and second chips while uncovering the backs of the same.

8. The IC board of claim 7, wherein the film carrier is of the type having a free-floating ring for supporting the inner-lead portions of the conductive wires.

9. The IC board of claim 7, wherein the film carrier is of the type having a corner-supported ring for supporting the inner-lead portions of the conductive wires.

10. The IC board of claim 9, wherein the insulating film is formed with at least one securing opening which is filled with the insulating material when forming the insulating compound to help secure the insulating compound to the film carrier.

11. The IC board of claim 7, wherein, when the multi-chip chip-scale IC package is mounted on a circuit board, the back of the second chip comes into contact with a printed circuit line on the circuit board.

12. The IC board of claim 11, wherein the back of the first chip is mounted with a heat-dissipating device.

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