

SEMICONDUCTOR WAFER CARRIER

BACKGROUND OF THE INVENTIONField of the Invention

The present invention relates to a carrier used for the transportation of semiconductor wafers from one processing station to another.

Discussion of the Related Art

Figs. 1A and 1B show a top view and a front view of a conventional wafer carrier.

In Fig. 1B, the carrier is seen on the side of an opening through which the wafers are inserted. The carrier includes a base 12 from which two vertical walls 13 extend on both sides. Walls 13 comprise horizontal grooves 15 with a trapezoidal section. Each groove 15 of one of walls 13 is in the same plane as a groove 15 of the other wall 13, so that the two grooves form a single groove for receiving a wafer.

As can be seen in Fig. 1A, walls 13 include a straight portion A on the side of the insertion opening and a curved portion B at the back, which follows the shape of the wafers and stops them.

The carrier is generally provided with a handle 17 forming integral with the upper surface of the carrier, arranged close to the insertion opening.

These carriers are used to carry batches of wafers from one processing station to another. At each station, the wafers are loaded and unloaded one by one by means of a handling robot provided with fingers which have to slide between the wafers. For the robot to be able to properly handle the wafers, it is necessary that the wafer positions vary little with respect to corresponding reference positions. The accuracy of the wafer positioning depends on grooves 15.

Fig. 2 shows an enlarged view of a groove 15. As mentioned previously, this groove 15 conventionally has a trapezoidal section, the narrowest side of the trapezoid forming the

9905387-8

30 OCT 1999

bottom of the groove. This shape enables an easy handling of the wafers with no clamping risk. The upper wall and the lower wall of the groove are slanted symmetrically with respect to the horizontal direction.

Fig. 2 also shows a same wafer 20 such as it is normally arranged at the level of straight portion A of the groove and at the level of curved portion B (see Fig. 1A). These two positions are designated by A and B, respectively.

In position B, the edge of the wafer is generally in contact with the groove bottom, this being due to the fact that, during transportation, the carriers are arranged with their insertion opening facing upwards and that these carriers are then handled with care when they are placed vertically, to avoid ejecting the wafers.

In position A, given the clearance that is provided at this level between the wafers and the groove bottoms, the edge of the wafer is distant from the groove bottom and thus is in a lower position than the rear edge of the wafer, due to the slanting of the lower groove wall. Thus, wafers 20 are slanted forward, which reduces the operation range of the handling robots and increases risks of wafer damage.

Conscious of this problem, carrier manufacturers have devised several solutions to ensure that wafers 20 are maintained more horizontally. FLUOROWARE has provided wafers in which the groove walls, still slanted, comprise a horizontal portion in the vicinity of the groove bottom.

This solution however has the disadvantage of widening the groove bottom, which decreases the axial positioning accuracy of the wafers when placed vertically. This inaccuracy is incompatible with an operation of wafer transfer to special carriers comprising, in the same volume, twice as many wafers. Indeed, this transfer operation is performed by lifting the wafers by means of a comb with a pitch which is double that of the wafers. If the wafers are axially mispositioned, they could be caught in wrong grooves of the comb.

EMPAK has devised to form, in the bottom of the grooves at the curved portion B, humps on the slanted walls. The humps aim at pushing the rear edges of the wafers substantially to the position of the edges in straight portion A of the grooves.

It is however difficult to form these humps with a sufficient accuracy and to ensure that the rear edges of the wafers are always pushed by the same distance, which causes wafer slanting dispersions.

Summary of the invention

An object of the present invention is to provide a wafer carrier ensuring an excellent wafer horizontality.

Another object of the present invention is to provide such a wafer carrier ensuring also an excellent axial positioning of the wafers when said wafers are vertically arranged.

To achieve these objects, the present invention provides a semiconductor wafer carrier comprising several parallel grooves for receiving the wafers by lateral insertion, the groove walls being configured so that the grooves narrow towards their bottom. The lower wall of each groove, on which the corresponding wafer rests when the carrier is arranged with the wafers parallel to the ground, is substantially horizontal, the upper wall being slanted.

According to an embodiment of the present invention, the lower walls of the grooves are vertically positioned so that the wafers have the same vertical position as in a conventional carrier, the grooves of which have two slanted walls.

According to an embodiment of the present invention, the groove bottoms are V-shaped.

According to an embodiment of the present invention, the lower walls of the grooves are slanted by approximately 1° with respect to the horizontal direction.

According to an embodiment of the present invention, the upper walls of the grooves are slanted by approximately 10° with respect to the horizontal direction.

According to an embodiment of the present invention, the V-shaped groove bottoms have an angle of substantially 135° .

The foregoing objects, features and advantages of the present invention, will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

Brief Description of the Drawings

Figs. 1A and 1B, previously described, show a top view and a front view of a conventional wafer carrier;

Fig. 2, previously described, shows an enlarged view of a groove of the carrier of Figs. 1A and 1B; and

Fig. 3 shows an embodiment of a groove of a carrier according to the present invention.

Detailed Description

In Fig. 3, a groove 15' of a wafer carrier according to the present invention includes asymmetrical walls. According to an aspect of the present invention, the lower wall is substantially horizontal, preferably very slightly slanted downwards from the groove bottom, for example, by approximately 1° . The upper wall of the groove is slanted to ensure a sufficient opening of the groove, necessary to facilitate wafer insertion. This upper wall is slanted upward from the groove bottom, by approximately 10° , for example.

Due to the fact that the lower wall is practically horizontal, the edge of a wafer 20 is practically at the same height, be it at the bottom of a groove or distant from the bottom. Wafer 20 thus remains horizontal.

It is desirable to be able to use a carrier according to the present invention to replace conventional carriers without having to modify the setting of the handling robots. It is also desirable to be able to indifferently use carriers according to the present invention and conventional carriers in a same installation. For this purpose, wafers 20 must, in a carrier according to the present invention, be at the same height as in a conventional carrier having grooves of the type in Fig. 2. In

other words, wafer 20 shown in Fig. 3, the edge of which is distant from the groove bottom, has to be at position A of Fig. 2. The corresponding position of the groove of Fig. 2 is shown in dotted lines in Fig. 3. The lower wall of groove 15' is at a height such that the edge of wafer 20 is at the intersection of the lower wall of groove 15', in full line, and of the lower wall of the groove shown in dotted line.

According to the groove opening and to the slanting chosen for its upper wall, the groove bottom can be relatively large. To nevertheless ensure a good axial positioning of the wafers when they are vertically positioned, the groove bottom preferably has, as shown, a V-shape. This V for example has an angle of approximately 135° . Thus, when the wafers are vertically arranged, they center by gravity at the bottom of the Vees, as shown for a wafer 22.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:



CLAIMS

1. A semiconductor wafer carrier comprising several parallel grooves (15, 15') for receiving the wafers (20) by lateral insertion, the groove walls being configured so that the grooves narrow towards their bottom, wherein the lower wall of each groove (15'), on which the corresponding wafer rests when the carrier is arranged with the wafers parallel to the ground, is substantially horizontal, the upper wall being slanted, and wherein the groove bottoms are V-shaped.

2. The wafer carrier of claim 1, wherein the lower walls of the grooves are vertically positioned so that the wafers have the same vertical position as in a conventional carrier, the grooves of which have two slanted walls.

3. The wafer carrier of claim 1, wherein the lower walls of the grooves are slanted by approximately 1° with respect to the horizontal direction.

4. The wafer carrier of claim 1, wherein the upper walls of the grooves are slanted by approximately 10° with respect to the horizontal direction.

5. The wafer carrier of claim 1, wherein the V-shaped groove bottoms have an angle of substantially 135° .