

## ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a memory cell array and an address decoder. The memory cell array includes a plurality of memory blocks, each of the plurality of memory blocks includes a plurality of dynamic memory cells coupled to word-lines and bit-lines, each of the plurality of memory blocks are divided into a plurality of row blocks by row block identity bits of a row address, and each of the of row blocks includes a plurality of sub-array blocks arranged in a first direction. The address decoder changes a physical row address of a memory cell that stores or outputs data based on a column address received with a write command or a read command.

FIG. 2