What is claimed is:

1. A semiconductor device comprising:

a gate pattern disposed over a lower structure, and including an intermediate gate pattern and an upper gate pattern over the intermediate gate pattern, wherein the intermediate gate pattern includes a gate electrode region and a gate pad region extending from the gate electrode region; ~~and~~

a vertical channel semiconductor layer having a side surface facing ~~the gate electrode region of~~ the intermediate gate pattern and the upper gate pattern~~,~~; and

a void in the gate pad region,

wherein the gate pad region includes a first pad region having a thickness greater than a thickness of the gate electrode region,

the first pad region includes an upper surface, a lower surface opposing the upper surface, and an outer side surface,

the outer side surface has a lower outer side surface and an upper outer side surface, divided from each other by a boundary portion, ~~and~~

the lower outer side surface extends from the lower surface in a rounded shape,

the lower outer side surface protrudes further in a lateral direction than the upper outer side surface,

the lateral direction is a direction from the gate electrode region toward the gate pad region,

the void is in the first pad region of the gate pad region, and

the void is at a lower level than the boundary portion.

2. The semiconductor device according to claim 1, wherein the lower outer side surface has a convex shape, and

wherein a connection portion of the lower outer side surface and the lower surface

has a rounded shape.

3. The semiconductor device according to claim 2, wherein the upper outer side surface has a convex shape and extends from the upper surface, and a connection portion of the upper outer side surface and the upper surface has a rounded shape, and

the boundary portion of the outer side surface is a concave portion formed by connecting the lower outer side surface having the convex shape and the upper outer side surface having the convex shape.

4. The semiconductor device according to claim 2, wherein at least a portion of the upper outer side surface has a concave shape, and

the boundary portion of the outer side surface is an inflection portion at a connection portion of the lower outer side surface having the convex shape and the portion of the upper outer side surface having the concave shape.

5. The semiconductor device according to claim 2, wherein the upper outer side surface comprises:

a first upper outer side surface extending at an obtuse angle with respect to the upper surface; and

a second upper outer side surface extending from the first upper outer side surface with a slope different than a slope of the first upper outer side surface.

6. The semiconductor device according to any one of claims 1 to 5, wherein the gate pad region further includes a second pad region between the first pad region and the gate electrode region, and

the second pad region includes a portion having a thickness smaller than the thickness of the gate electrode region.

7. The semiconductor device according to any one of claims 1 to 6, wherein a relatively lower portion of the lower outer side surface protrudes further in a lateral direction than a relatively upper portion of the lower outer side surface.

8. The semiconductor device according to any one of claims 1 to 6, wherein ~~the lower outer side surface protrudes further in a lateral direction than the upper outer side surface~~the semiconductor device further comprises:

an upper interlayer insulation layer disposed on the upper gate pattern;

a first capping insulation layer disposed to cover the gate pad region and having an upper surface coplanar with the upper interlayer insulation layer; and

an insulating liner covering the gate pad region and extending between the upper interlayer insulation layer and the first capping insulation layer.

9. A semiconductor device comprising:

a first gate pattern over a lower structure;

a second gate pattern over the first gate pattern; ~~and~~

an intermediate interlayer insulation layer between the first gate pattern and the second gate pattern~~,~~; and

a vertical channel semiconductor layer having a side surface facing the first and second gate patterns,

wherein the first gate pattern includes a gate electrode region overlapping with the second gate pattern, and a gate pad region extending from the gate electrode region,

the gate pad region includes a first pad region having a thickness greater than a thickness of the gate electrode region,

the first pad region includes a lower region and an upper region on the lower region, and

the lower region includes a lower outer side surface having a convex shape, and

wherein the semiconductor device further comprises:

an upper interlayer insulation layer disposed on the second gate pattern;

a first capping insulation layer disposed to cover the gate pad region and having an upper surface coplanar with the upper interlayer insulation layer; and

an insulating liner covering the gate pad region and extending between the upper interlayer insulation layer and the first capping insulation layer.

~~10. The semiconductor device according to claim 9, wherein the first and second gate patterns protrude further than the interlayer insulation layer in a direction parallel to an upper surface of the lower structure.~~

~~11~~10. The semiconductor device according to claim 9 ~~or claim 10~~, wherein the second gate pattern has a lower surface and an outer side surface extending from the lower surface, and a connection portion of the lower surface and the outer side surface has a rounded shape.

~~12~~11. The semiconductor device according to ~~any one of claims 9 to 11~~claim 9 or claim 10, wherein the upper region includes an upper outer side surface, ~~and~~

the first pad region includes a boundary portion, which divides the lower outer side surface of the lower region and the upper outer side surface of the upper region, and

wherein a thickness of the lower region is greater than a thickness of the upper region.

~~13. The semiconductor device according to claim 12, wherein a thickness of the lower region is greater than a thickness of the upper region.~~

~~14~~12. The semiconductor device according to claim ~~12 or claim 13~~11, wherein the upper region includes a first upper region, and a second upper region between the first upper region and the lower region,

the upper outer side surface includes a first upper outer side surface of the first upper region, and a second upper outer side surface of the second upper region, and

the first upper outer side surface and the second upper outer side surface have different shapes.

~~15~~13. The semiconductor device according to ~~any one of claims 12 to 14~~claim 11 or claim 12, wherein the upper region includes a raised side surface opposing the upper outer side surface, and

wherein the raised side surface includes a first raised side surface extending from an upper surface of the upper region and forming an obtuse angle with the upper surface of the upper region, and a second raised side surface extending from the first raised side surface and having a more acute slope than the first raised side surface.

~~16~~14. A semiconductor device comprising:

a lower structure;

gate patterns spaced apart from each other in a direction perpendicular to an upper surface of the lower structure, the gate patterns including intermediate gate patterns, a lower gate pattern in a position lower than a position of the intermediate gate patterns, and an upper gate pattern over the intermediate gate patterns; and

a vertical channel semiconductor layer having a side surface facing the upper gate pattern, the intermediate gate patterns and the lower gate pattern,

wherein each of the intermediate gate patterns includes an intermediate gate electrode region overlapping with a gate pattern from among the gate patterns positioned at a relatively upper portion, and an intermediate gate pad region extending from the

intermediate gate electrode region,

the intermediate gate pad region includes a first intermediate pad region, and a second intermediate pad region between the intermediate gate electrode region and the first intermediate pad region,

the first intermediate pad region has a thickness greater than a thickness of the intermediate gate electrode region and a thickness of the intermediate second pad region,

the first intermediate pad region includes a lower outer side surface, an upper outer side surface, and a boundary portion between the upper outer side surface and the lower outer side surface, ~~and~~

a connection portion of a bottom surface of the first pad region and the lower outer side surface of the first pad region has a rounded shape,

the lower outer side surface of the first pad region protrudes further in a lateral direction than the upper outer side surface of the first pad region,

the lower outer side surface has a convex shape, and

the lateral direction is a direction from the gate electrode region toward the gate pad region.

~~17~~15. The semiconductor device according to claim ~~16~~14,

wherein the intermediate gate patterns include a first gate pattern, a second gate pattern over the first gate pattern, and one or more third gate patterns over the first gate pattern and in a position lower than a position of the second gate pattern,

the intermediate gate pad region of each of the first and second gate patterns extends from the intermediate gate electrode region in a first horizontal direction, and

outer side surfaces of the one or more third gate patterns positioned in the first horizontal direction extend from lower surfaces of the one or more third gate patterns in a rounded shape.

~~18~~16. The semiconductor device according to claim ~~17~~15, wherein relatively lower portions of the outer side surfaces of the one or more third gate patterns protrude further in a lateral direction than relatively upper portions of the outer side surfaces of the one or more third gate patterns.

~~19~~17. The semiconductor device according to ~~any one of claims 16 to 18~~claim 15, wherein the lower gate pattern includes a lower gate electrode region overlapping the intermediate gate patterns, and a lower gate pad region extending the lower gate electrode region in the lateral direction~~the gate patterns further include a lower gate pattern in a position lower than a position of the intermediate gate patterns~~, and

wherein the~~a~~ connection portion of the bottom surface of the first intermediate pad region and the lower outer side surface of the first intermediate pad region has a more rounded shape than a connection portion of a lower surface of the lower gate pad region of the lower gate pattern and an outer side surface of the lower gate pad region of the lower gate pattern.

~~20~~18. The semiconductor device according to claim ~~19~~15, wherein ~~the gate patterns further include an upper gate pattern over the intermediate gate patterns, and~~

a connection portion of a lower surface of the upper gate pattern and an outer side surface of the upper gate pattern has a more rounded shape than the connection portion of the lower surface of the lower gate pad region of the lower gate pattern and the outer side surface of the lower gate pad region of the lower gate pattern.

19. The semiconductor device according to claim 16, further comprising a void in the first pad region,

wherein at least a portion of the void is at a lower level than the boundary portion.

20. The semiconductor device according to claim 16, further comprising contact plugs,

wherein the lower gate pattern includes a lower gate electrode region overlapping the intermediate gate patterns, and a lower gate pad region extending the lower gate electrode region in the lateral direction,

wherein the upper gate pattern includes an upper gate electrode region, and an upper gate pad region extending the upper gate electrode region in the lateral direction,

wherein a thickness of the lower gate pad region is the same as a thickness of the lower gate electrode region,

wherein the thickness of the lower pad region is smaller than the thickness of the first intermediate pad region,

wherein a thickness of the upper gate pad region is substantially the same as a thickness of the upper gate electrode region,

wherein the thickness of the upper pad region is smaller than the thickness of the first intermediate pad region, and

wherein the contact plugs include:

a lower contact plug contacting the lower gate pad region of the lower gate pattern;

intermediate contact plugs contacting the intermediate gate pad regions of the intermediate gate patterns; and

an upper contact plug contacting the upper gate pad region of the upper gate pattern.