Description

Connection for coupling binary control and warning signals into a data processing unit

As a rule, a large number of binary control and warning signals must be processed, for instance, in the automation of technical processes such as, for example, in the case of technical plant, machines, equipment and the like, with the aid of data processing systems, e.g. process computers, stored-program or numeric controls or application-specific integrated circuits (ASICs). In the text which follows, the data processing system will be called processor, to simplify matters but this is not connected with a restriction to conventional microprocessors. The binary control and warning signals, which will be called binary signals to simplify matters in the text which follows, are generated by suitable transducers in the technical process depending on the current state or when special operating conditions occur and must be supplied to the processor. In the processor, this results in a change in its program sequence in the sense of an appropriate intended response to the changed condition conveyed by the respective binary signal.

Such changes in status can be classified in two groups. The first group of status changes involves so-called warning or alarm signals. Due to the urgency, the associated binary signals require fast response of the processor and will be called interrupt-capable binary signals in the text which follows. In the case of microprocessors, such fast responses can be effected by immediate interruptions of the running program with the aid of a so-called interrupt. The second group of status changes involves so-called status signals which indicate the occurrence of a less critical operational change which, in most cases, has been present for a relatively long time. Although the associated binary signals, which will be called status-

capable binary signals in the text which follows, do not require a fast response of the processor, they must still be inserted correctly into the program sequence of the processor within a predetermined period of time.

A problem is seen in the fact that hitherto almost every binary signal and especially the binary signals of the first group which force a fast response of the processor by triggering an interrupt, are supplied to the processor system in the form of a separate signal. If, for example, an application-specific circuit (ASIC) has a very large number of internal interrupt sources, a very large number of connections must be reserved at the output of the ASIC and at the input of the processor system. On the other hand, the manner of supplying a binary signal of the second group, which signals a status change, to the processor is different, as a rule, in comparison with the status-capable binary signals. Thus, different hardware connections are frequently provided for interrupt-capable binary signals and for status-capable binary signals at the processor input. This further increases the circuit complexity.

On pages 237 to 255 in the textbook by Helmut Müller and Lothar Walz with the title "Mikroprozessortechnik" (Microprocessor technology), Vogel Fachbuchverlag Würzburg, 1st edition 1988, a so-called parallel interface chip is described. This has two input or output data registers designated as one port each. The direction of the data is selected via a program in which a large number of operating modes can be preset for the ports. In an operating mode designated as single-bit input/output, every bit of a port can be changed and output or read in by means of a single-bit command. Furthermore, each bit which is switched as input can trigger an interrupt.

The invention, by comparison, is based on the object of specifying a connection which can be used more universally.

The object is achieved by means of the connection contained in Claim 1. Advantageous further developments of the invention are contained in the subclaims.

The connection according to the invention has the advantage that a suitable internal preprocessing in the input modules according to the invention makes it possible to supply binary signals of both groups, i.e. both interrupt-capable binary signals and status-capable binary signals, to a processor in a simple manner.

The invention will be explained in greater detail by means of the figures listed briefly in the text which follows. In the figures,

Figure 1 shows a diagram of the connection according to the invention,

Figure 2 shows a first embodiment for an input module in the connection according to the invention, and

Figure 3 shows a second embodiment for an input module in the connection according to the invention.

In the left-hand area of Figure 1, binary control and warning signals B1...Bn, called binary signals in the text which follows, are supplied externally to the circuit according to the invention. In this arrangement, each binary signal B1...Bn is subjected to preprocessing in a respective input module M1...Mn allocated for this purpose. In Figure 1, only the input module M1 belonging to binary signal B1 is shown for reasons of clarity, whilst the other input modules are symbolized by a general module Mn. After completed preprocessing, the binary signals B1...Bn appear in the form of so-called interrupt signals IR1...IRn and/or status signals ST1...STn, the generation and function of which will be explained in the text which

follows, at the output of the respective input module M1...Mn and are supplied to an input and output interface area of a processor MP shown in the right-hand area of Figure 1.

According to the invention, each input module M1...Mn can be switched over, preferably via a so-called mode bit MB1...MBn in such a manner that the quality of a signal triggering an interrupt of the processor MP, called interrupt-capable binary signal in the text which follows, or the quality of a binary signal informing the processor MP of a status, called status-capable binary signal in the text which follows, can be freely allocated in an application-specific manner to the associated binary signal B1...Bn. In accordance with this allocation, the corresponding binary signal B1...Bn appears in the form of a so-called interrupt signal IR1...IRn or of a so-called status signal ST1...STn at the output of the corresponding input module M1...Mn. The mode bits M1...Mn are first written into a register RMB, preferably via a load signal LMB, by the processor MP. To distribute the bits, each output of the register RMB is connected to the corresponding input at the respective input module M1...Mn for supplying the associated mode bit MB1...MBn. For the further explanation it will be assumed that a mode bit having the significance 0 will switch the corresponding input module over in such a manner that it converts the binary signal Bn at the input into an interrupt signal IRn at the output. On the other hand, a mode bit having the significance 1 will switch the corresponding input module over in such a manner that it converts the binary signal Bn at the input into a status signal STn at the output.

This arrangement has the advantage that the classification as interrupt signal or as status signal can be allocated to a binary signal B1...Bn without any restriction and at any time, i.e. the allocation can be freely parametrized. In practice, the decision which of the binary signals B1...Bn present overall require a fast response of the processor and which do not will often be

taken only late in a development sequence and may also have to be revised. This circumstance is accorded special consideration by the invention in that a binary signal can be excluded from the interrupt processing of the processor or can be supplied to it in an application-specific manner via the "mode bit control".

In the opposite input and output interface area of the processor MP, a first register RIR, which can be switched between the read and store states via a control bit SIR is provided for simultaneously receiving active interrupt signals IR1...IRn. In parallel therewith, there is a second register RST which can also be switched between the read and store states via a control bit RST for simultaneously receiving active status signals ST1...STn. In this arrangement, the number of available interrupt signals IR1...IRn and of the status signals ST1...STn in each case corresponds to the existing number of binary signals B1...Bn and thus determines the bit width of the registers RIR and RST.

The content of the registers is read in at suitable times via the databus DB by the processor MP and is correspondingly processed further. If one or more binary signals B1...Bn occur which are classified as interrupt-capable binary signals, these will trigger a control signal AIR via a logic OR gate IRO which combines all interrupt signals IR1...IRn. This collective signal signals to the processor MP the presence of at least one active interrupt-capable binary signal B1...Bn and of the corresponding subsequent signal IR1...IRn. The processor MP thereupon interrupts its normal program sequence, activates the register RIR via the control bit SIR so that the entire content of the register RIR and thus also the in each case active signals from the group IR1...IRn are supplied to the processor MP via the databus DB. The processor can then trigger actions separately allocated to each of the active interrupt-capable binary signals.

If, on the other hand, one or more binary signals B1...Bn occur which are classified as status-capable binary signals, these are present at the input of register RST. The content of this register will be supplied to the processor MP via the databus DB by the one main programm in the processor, during each normal run of this programm and controlled via a control bit SST acting on the register RST. The processor, in turn, can then trigger actions individually allocated to each of the active status-capable binary signals.

The device according to the invention thus has the advantage, on the one hand, that a number of interrupt signals, which have become active following one another closely in time and have not yet been processed, of different binary signals B1...Bn used as source can be supplied to the processor in a single-interrupt process by reading the register RIR. Due to this temporary buffer function, the loss of interrupt-capable binary signals which disappear again unexpectedly quickly, on the one hand, and, on the other hand, multiple interrupt-related interruptions following one another directly in the program sequence of the processor MP can be avoided. Interrupt signals IR1...IRn which have become active almost simultaneously will not be prioritized and thus do not cause any separate interrupt processes. The multiple triggering, which may occur in direct succession in time, of an interrupt-like interruption of the program of the processor is avoided and thus its loading is reduced. Instead, all interrupt signals which have been detected as almost simultaneously active by reading the content of the register RIR will be processed in succession under software control. On the other hand, less time-critical binary signals no longer produce interrupts in the processor but can be reliably detected via the register RST even if they only occur in short pulses.

If thus the content of the register RIR or of the register RST has been "read" by the processor MP, the latter outputs a reset signal RMI or RMS. As shown in Figure 1, this pair of signals is supplied to each of the input modules M1...Mn. Due to the presetting of each input module by the appropriate mode bit MB1...MBn, however, not all the input modules M1...Mn will be reset in the same manner. Instead, after the register RIR has been read and the associated reset signal RMI has been activated as a result, only those input modules Mn will be reset which have been switched over via the corresponding mode bit MBn in such a manner that an interrupt signal IRn at the output has been allocated to an active binary signal Bn at the input. Correspondingly, after the register RST has been read and the associated reset signal RMS has been activated as a result, only those input modules Mn will be reset which were switched over via the corresponding mode bit MBn in such a manner that a status signal STn at the output has been allocated to an active binary signal Bn at the input.

This arrangement has the special advantage that the processing of the binary signals classified as interrupt signals and as status signals via the mode bits can take place in a manner in which they are decoupled from one another. On the one hand, the group of status signals can be read via the register RST separately in time from the interrupt signals detected via the register RIR. On the other hand, however, the reading of one of the two registers and the associated resetting of associated input modules will not influence the condition of the other input modules. If, for example, active binary signals classified as status signals, i.e. less urgent information, is fetched and processed by reading the register RST, the subsequent resetting of the associated input modules will not influence the condition of the other input modules for interrupt-capable binary signals, and thus the condition of the register RIR. Any interrupt signals IR1...IRn which may be present will thus not be

deleted but can expect immediately fast processing by the processor by way of an interrupt.

Figure 1 also shows a first embodiment of the internal configuration of the identical input modules M1...Mn. This will be explained using input module M1 as an example. The active edge of the corresponding binary signal B1, the rising edge in the example, is first supplied to a resettable storage element. This makes it possible to temporarily store the active state of the triggering binary signal independently of whether this state disappears again in the meantime. The resettable storage element is preferably constructed in the form of a flip flop F1 which is supplied with the binary signal at the clock input. The active signal state of the binary signal B1 which is virtually reproduced at the output Q of flip flop F1 is now supplied to a selection circuit AS1. Depending on the state of mode bit MB1, this forms from this either an active interrupt signal IR1 (e.g. when MB1 = 0) or an active status signal ST1 (e.g. when MB1 = 1), which is then temporarily stored in the manner already described, either in the register RIR for interrupt signals or in the register RST for status signals. After the content of register RIR or RST has been read, a corresponding reset signal RMI or RMS is formed and supplied to a switching element S1 in the input module AS1. This element, in turn, conducts either an active reset signal RMI or RMS to the reset input R of flip flop F1 depending on the state of mode bit MB1. If, for example, the input module MB1 is switched to converting an active binary signal B1 into an interrupt signal IR1 by a mode bit MB1 having the significance, flip flop F1 is reset by an active reset signal RMI triggered by reading the register RIR whilst an active reset signal RMS triggered by reading the register RST has no effect.

Figure 2 shows a first embodiment of an input module M1...Mn in detail. The associated selection circuit AS1 has two logic AND gates U11 and U21 for generating an interrupt signal IR1 or a status signal ST1. One input of the AND gates U11, U21 is in each case supplied with the output signal Q of flip flop F1. The other input of gate U11, in contrast, is supplied with mode bit MB1 inverted via an invertor I1 and the other input of gate U21 is directly supplied with mode bit MB1. The consequence of this is that in the case of a mode bit having significance 0, an active binary signal B1 generates an interrupt signal IR1 via gate U11 whilst in the case of a mode bit having significance 1, an active binary signal B1 generates a status signal ST1 via gate U21. Flip flop F1, which stores every active edge of a binary signal B1...Bn independently of its classification as interrupt-capable or status-capable binary signal via the mode bit ensures, that status-capable binary signals present only for a short time as an exception are also detected and mapped to a status signal ST1...STn.

Figure 3 shows a second especially advantageous embodiment of an input module M1...Mn in detail. The associated selection circuit AS1 has a logic AND gate U11 for generating an interrupt signal IR1 and a logic OR gate O1 for generating a status signal ST1. One input of the two gates U11 and O1 is again supplied in each case with the output signal Q of flip flop F1. On the other hand, only the other input of gate U11 is supplied with the mode bit MB1 inverted via an invertor I1 whilst the other input of gate O1 is directly supplied with binary signal B1 via a line L2.

If, for example, the input module MB1 is switched to converting an active binary signal B1 into a status signal ST1 by a mode bit MB1 having significance 1, the AND gate U11 is blocked via the invertor I1 and the

generation of an interrupt signal is prevented. An active edge of the binary signal B1 then sets the flip flop F1. The output Q of the latter then generates an active status signal ST1 via line L1 and the OR gate O1. If after the register RST has been read and the status change has been detected by the processor MP, a reset signal RMS is generated, flip flop F1 will be reset because of the corresponding position of switch S1. If, however, the originating binary signal B1 is present unchanged, a status signal ST1 will also be generated unchanged via line L2 and OR gate O1. This arrangement has the advantage that thus, as a rule, status-capable binary signals B1 active for relatively long periods of time, i.e. a number of processor cycles, can be observed and especially the time of their inactivation can be detected.

If, on the other hand, the input module MB1 has been switched to converting an active binary signal B1 into an interrupt signal IR1 by mode bit MB1 having significance 0, the AND gate U11 is activated via the invertor I1. An active edge of the binary signal B1 sets flip flop F1. Its output Q then generates an active interrupt signal IR1 via AND gate U11. The fact that in this case an active signal ST1 also appears at the output of the OR gate via lines L1, L2 is initially without significance. Due to the interrupt signal IR1, the sequence of the main program in the processor is interrupted by an interrupt via gate IRO and the collective alarm AIR caused by it, and the content of the associated register RIR is correctly read. As a result, the binary signal or signals B1...Bn used as interrupt source is identified and the appropriate actions are triggered.

After the register RIR has been read the processor continues the interrupted processing of the main program. Furthermore, a reset signal RIS is again generated and flip flop F1 is reset because of the corresponding position of switch S1. If then, however, the originating binary signal B1 is present unchanged contrary

to the usual expectations, the signal ST1 generated via line L2 and OR gate O1 becomes active. This is detected by the processor as a status signal when the main program routinely reads the register RST for status signals in the course of normal processing. The main program is then capable of detecting from the divergence between the classification of the binary signal B1 as interrupt-capable binary signal, on the one hand, and the unchanged activity of this signal in the form of a status signal which has been virtually bridged through despite preceding interrupt processing, that an unusual condition and possibly even a fault condition is present which cannot be eliminated by actions triggered via the interrupt. Furthermore, it is prevented that this faultily invariably active interrupt-capable binary signal B1 continuously triggers interrupts in the processor MP and thus almost stops the normal processing of its main program.

The embodiment shown in Figure 2 thus has the advantage that the capability of the circuit, triggered by a signal interrupt signal, of processing a multiplicity of different interrupt-capable binary signals, which have become active in close succession in time, by the processor in a single-interrupt routine virtually in parallel, is not impaired. The resetting of the affected input modules caused by the read-out of the register RIR thus deletes all interrupt signals IR1...IRn which have been hitherto active. Even if one of the binary signals requesting an interrupt should still remain active, no new interrupt request is triggered via the OR gate IRO and the control signal AIR. The "disturbed" binary signal is thus taken out of the interrupt processing virtually automatically in spite of corresponding presetting via the mode bit, and passed over into the level of status signal processing. The interrupt routine in the processor system can then respond again to new interrupt signals IRn of undisturbed binary signals Bn which have become active.

The connection according to the invention is characterized, on the one hand, by a simple uncomplicated hardware configuration, especially of the input modules AS1...ASn. On the other hand, by means of the mode bit control these modules can be used universally both for interrupt-capable binary signals requiring a fast response and for status-capable binary signals requiring to be processed with less time priority. Finally, the modules can be developed further in a further embodiment so that interrupt-capable binary signals present permanently due to a fault are also detected and do not cause any blocking of the connection.

Patent Claims

1. Device for coupling binary signals (B1...Bn) used as control and warning signals into a processor (MP), each binary signal (B1...Bn) being supplied to a separately allocated input module (MB1...MBn) which

a) have both in each case an output (IR1...IRn) for outputting a binary signal (B1...Bn) classified as interrupt-capable and in each case an output (ST1...STn) for outputting a binary signal (B1...Bn) classified as status-capable, and which

b) can be switched over in an application-specific manner via the processor (MP) in such a manner that, when an active state of the corresponding binary signal (B1...Bn) occurs, these modules generate at the appropriate output an interrupt signal (IR1...IRn) interrupting the normal program sequence of the processor (MP) or a status signal (ST1...STn) which can be detected by the processor (MP) during a normal program sequence.

2. Device according to one of the preceding claims, wherein both a register (RIR) for interrupt signals (IR1...IRn) and a register (RST) for status signals (ST1...STn) is preferably present for temporary storage in the processor (MP).

3. Device according to claim 2, wherein, when an interrupt signal (IRn) occurs, the normal program sequence of the processor (MP) is interrupted, the content of the register for interrupt signals (IR1...IRn) is read and a first reset signal (RMI) is generated by the processor (MP) for those input modules (MB1...MBn) which were switched over for generating interrupt signals (IR1...IRn).

4. Device according to claim 2, wherein, in the normal sequence of the program of the processor (MP), the content of the register for status signals (ST1...STn) is read and a second reset signal (RMS) is generated by the processor (MP) for those input modules (MB1...MBn) which were switched over for generating status signals (ST1...STn).

5. Device according to one of the preceding claims, wherein the interrupt signals (IR1...IRn) of the input modules (MB1...MBn) are combined into an interrupt requesting signal (AIR) for the processor (MP) via a preferably logic OR gate (IRO).

6. Device according to one of claims 2 to 5, wherein the width of the registers for interrupt and status signals (RIR, RST) corresponds to the number of binary signals (B1...Bn).

7. Device according to one of the preceding claims, wherein each input module (MB1...MBn) has both an output for an interrupt signal (IR1...IRn) and an output for a status signal (ST1...STn).

8. Device according to one of the preceding claims, wherein each input module (MB1...MBn) has a resettable storage element (F1...Fn), especially a flip flop, for the active edge of the associated binary signal (B1...Bn).

9. Device according to claim 8, wherein the resettable storage element (F1...Fn) is followed by a selection circuit (AS1...ASn) which can be switched over by the processor (MP).

10. Device according to claim 9, wherein the selection circuits (AS1...ASn) in the input modules (MB1...MBn) are switched over by one mode bit (MB1...MBn) each, and the mode bits (MB1...MBn) are stored by the processor (MP) in a register for mode bits (RMB) and are supplied separately to the input modules (MB1...MBn).

11. Device according to claims 9 and 10, wherein the selection circuits (AS1...ASn) in the input modules (MB1...MBn) have

a) in each case an AND gate (U11...U1n) for generating an interrupt signal (IR1...IRn), one input of the gate being connected to the output of the resettable storage element (F1...Fn) and the mode bit (MB1...MBn) being applied to the other input of the gate, and

b) in each case an OR gate (O1...On) for generating a status signal (ST1...STn), one input of the gate being connected to the output of the resettable storage element (F1...Fn) and the binary signal (B1...Bn) being applied to the other input of the gate.