

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate including a first region and a second region;

a lower layer structure on the substrate, the lower layer structure having a first thickness on the first region and a second thickness on the second region, the second thickness being greater than the first thickness, the lower layer structure including an electrode layer at a top and an insulating layer under the electrode layer;

an etch stop layer on the lower layer structure;

an upper layer structure on the etch stop layer, a top surface of the upper layer structure being substantially a same level on the first and second regions, the etch stop layer having an etch selectivity with respect to both the upper layer structure and the lower layer structure; and

a first contact plug filling a first opening, the upper layer structure and the etch stop layer including the first opening defined therethrough on the first region, the first contact plug being in connection with the electrode layer of the lower layer structure; and

a second contact plug filling a second opening, the upper layer structure and the etch stop layer including the second opening defined therethrough on the second region, a bottom surface of the first contact plug having a first distance from a bottom surface of the etch stop layer and a bottom surface of the second contact plug having a second distance from the bottom surface of the etch stop layer, the first distance being different from the second distance;

wherein each of the first and second contact plugs includes an extended portion extending in a first direction perpendicular to a top surface of the substrate and a contacted portion protruding horizontally from the extended portion and disposed in the etch stop layer.

2. The semiconductor device of claim 1, wherein the second distance extends farther

into the electrode layer of the lower layer structure from the bottom surface of the etch stop layer than the first distance.

3. The semiconductor device of claim 1, wherein the etch stop layer includes a material having the etch selectivity of about 1000:1 or more with respect to both the upper layer structure and the lower layer structure.

4. The semiconductor device of claim 1, wherein the etch stop layer is an amorphous boron layer containing about 90 to 100 atomic percent of boron.

5. The semiconductor device of claim 1, wherein the first contact plug has a first sidewall portion facing the etch stop layer, the second contact plug has a second sidewall portion facing the etch stop layer, and the first sidewall portion has an inclined shape and the second sidewall portion has a rounded shape.

6. The semiconductor device of claim 1, wherein the upper layer structure includes at least one of a single insulation layer, a plurality of insulation layers, or a stack of conductive patterns and insulation layers.

7. A semiconductor device comprising:
a substrate including a first region and a second region;
a lower layer structure on the substrate, the lower layer structure having a first thickness

on the first region and a second thickness on the second region, the second thickness being greater than the first thickness, the lower layer structure including an electrode layer at a top and an insulating layer under the electrode layer;

an amorphous boron layer on the lower layer structure, ;

an upper layer structure on the amorphous boron layer, a top surface of the upper layer structure being substantially a same level on the first and second regions, the amorphous boron layer having an etch selectivity with respect to both the upper layer structure and the lower layer structure;

a first contact plug filling a first opening, the upper layer structure and the amorphous boron layer including the first opening defined therethrough on the first region, the first contact plug being in connection with the electrode layer of the lower layer structure; and

a second contact plug filling a second opening, the upper layer structure and the amorphous boron layer including the second opening defined therethrough on the second region, the second contact plug being in connection with the electrode layer of the lower layer structure;

wherein each of the first and second contact plugs includes an extended portion extending in a first direction perpendicular to a top surface of the substrate and a contacted portion protruding horizontally from the extended portion and disposed in the etch stop layer.

8. The semiconductor device of claim 7, wherein the amorphous boron layer includes about 90 to 100 atomic percent of boron.

9. The semiconductor device of claim 8, wherein the amorphous boron layer has an etch selectivity of about 1000:1 or more with respect to both the lower layer structure and the upper layer structure.

10. The semiconductor device of claim 7, wherein a bottom surface of the first contact plug and a bottom surface of the second contact plug are at first and second distances, respectively, from a bottom surface of the amorphous boron layer, and the first and second distances are different from each other.

11. The semiconductor device of claim 10, wherein the second distance extends farther into the electrode layer of the lower layer structure from the bottom surface of the amorphous boron layer than the first distance.

12. The semiconductor device of claim 7, wherein the first contact plug has a first sidewall portion facing the amorphous boron layer, the second contact plug has a second sidewall portion facing the amorphous boron layer, and the first sidewall portion has an inclined shape and the second sidewall portion has a rounded shape.

13. The semiconductor device of claim 7, wherein at least one of the lower layer structure or the upper layer structure includes at least one of a single insulation layer, a plurality of insulation layers, or a stack of conductive patterns and insulation layers.

14. A three dimensional (3D) semiconductor memory device comprising:
a substrate including a cell array region and a connection region;
a stack structure on the substrate, the stack structure being an alternating structure of

conductive layers and insulating layers, the stack structure having a stepped shape in the connection region, the stepped shape including a plurality of steps, the plurality of steps including at least a first step and a second step, the second step being lower than the first step, the first step and the second step each including a conductive layer at a top and an insulating layer under the conductive layer;

an etch stop layer on the stack structure;

a layer structure on the etch stop layer, a top surface of the layer structure being substantially a same level on the cell array region and the connection region, the etch stop layer having an etch selectivity with respect to both the layer structure and the stack structure;

a first contact plug filling a first opening, the layer structure and the etch stop layer including the first opening defined therethrough and reaching the conductive layer of the first step; and

a second contact plug filling a second opening, the layer structure and the etch stop layer including defined therethrough and reaching the conductive layer of the second step, a bottom surface of the first contact plug being farther into the conductive layer of the layer structure from a bottom surface of the etch stop layer than a bottom surface of the second contact plug;

wherein each of the first and second contact plugs includes an extended portion extending in a first direction perpendicular to a top surface of the substrate and a contacted portion protruding horizontally from the extended portion and disposed in the etch stop layer.

15. The semiconductor memory device of claim 14, wherein the etch selectivity of the etch stop layer with respect to both the layer structure and the stack structure is about 1000: 1 or more.

16. The semiconductor memory device of claim 14, wherein the etch stop layer is an amorphous boron layer.

17. The semiconductor memory device of claim 16, wherein the amorphous boron layer includes about 90 to 100 atomic percent of boron.

18. The semiconductor memory device of claim 16, wherein the amorphous boron layer has an etching selectivity of about 1000:1 or more with respect to both the layer structure and the stack structure.

19. The semiconductor memory device of claim 14, wherein the first contact plug has a first sidewall portion facing the etch stop layer, the second contact plug has a second sidewall portion facing the etch stop layer, and the first sidewall portion has an inclined shape, and the second sidewall portion has a rounded shape.

20. The semiconductor memory device of claim 14, wherein the layer structure includes at least one of a single insulation layer, a plurality of insulation layers, or a stack of conductive patterns and insulation layers.

21. A method of manufacturing a semiconductor device, the method comprising:
providing a substrate including a cell array region and a connection region;

forming a stack structure on a substrate such that the stack structure has a stepped shape in the connection region, the stack structure being an alternating structure of conductive layers and insulating layers, the stepped shape including a plurality of steps, the plurality of steps including at least an upper step and a lower step, the upper step and the lower step each including a conductive layer at a top and an insulating layer under the conductive layer;

forming an etch stop layer on the stack structure;

forming a layer structure on the etch stop layer such that a top surface of the layer structure is substantially a same level on the cell array region and the connection region, the etch stop layer having an etch selectivity with respect to both the layer structure and the stack structure;

forming a first opening through the layer structure and the etch stop layer on the upper step such that a bottom surface of the first opening has a first distance from a bottom surface of the etch stop layer;

forming a second opening through the layer structure and the etch stop layer on the lower step such that a bottom surface of the second opening has a second distance from the bottom surface of the etch stop layer and the first distance is farther into the conductive layer of the stack structure from the bottom surface of the etch stop layer than the second distance;

removing the etch stop layer remaining in the first and second openings;

filling a first contact plug in the first opening and filling a second contact plug in the second opening to form an intermediate structure; and

providing the semiconductor device employing the intermediate structure;

wherein each of the first and second contact plugs includes an extended portion extending in a first direction perpendicular to a top surface of the substrate and a contacted portion protruding horizontally from the extended portion and disposed in the etch stop layer.

22. The method of claim 21, wherein the forming an etch stop layer includes forming

an amorphous boron layer containing about 90 to 100 atomic percent of boron.

23. The method of claim 21, wherein the filling a first contact plug includes forming the first contact plug, which has a first sidewall portion facing the etch stop layer, the filling a second contact plug includes forming a second sidewall portion facing the etch stop layer, the first sidewall portion has an inclined shape, and the second sidewall portion has a rounded shape.