

A Method Of Performing Model-Based Scanner Tuning

Technical Field

[01] The technical field of the present invention relates generally to a method and program product for performing model-based scanner tuning and optimization so as to allow for optimization of performance of multiple lithography systems.

Background

[02] Lithographic apparatus can be used, for example, in the manufacture of integrated circuits (ICs). In such a case, the mask may contain a circuit pattern corresponding to an individual layer of the IC, and this pattern can be imaged onto a target portion (*e.g.* comprising one or more dies) on a substrate (silicon wafer) that has been coated with a layer of radiation-sensitive material (resist). In general, a single wafer will contain a whole network of adjacent target portions that are successively irradiated via the projection system, one at a time. In one type of lithographic projection apparatus, each target portion is irradiated by exposing the entire mask pattern onto the target portion in one go; such an apparatus is commonly referred to as a wafer stepper. In an alternative apparatus, commonly referred to as a step-and-scan apparatus, each target portion is irradiated by progressively scanning the mask pattern under the projection beam in a given reference direction (the "scanning" direction) while synchronously scanning the substrate table parallel or anti-parallel to this direction. Since, in general, the projection system will have a

magnification factor M (generally < 1), the speed V at which the substrate table is scanned will be a factor M times that at which the mask table is scanned. More information with regard to lithographic devices as described herein can be gleaned, for example, from US 6,046,792, incorporated herein by reference.

[03] In a manufacturing process using a lithographic projection apparatus, a mask pattern is imaged onto a substrate that is at least partially covered by a layer of radiation-sensitive material (resist). Prior to this imaging step, the substrate may undergo various procedures, such as priming, resist coating and a soft bake. After exposure, the substrate may be subjected to other procedures, such as a post-exposure bake (PEB), development, a hard bake and measurement/inspection of the imaged features. This array of procedures is used as a basis to pattern an individual layer of a device, *e.g.*, an IC. Such a patterned layer may then undergo various processes such as etching, ion-implantation (doping), metallization, oxidation, chemo-mechanical polishing, etc., all intended to finish off an individual layer. If several layers are required, then the whole procedure, or a variant thereof, will have to be repeated for each new layer. Eventually, an array of devices will be present on the substrate (wafer). These devices are then separated from one another by a technique such as dicing or sawing, whence the individual devices can be mounted on a carrier, connected to pins, etc.

[04] For the sake of simplicity, the projection system may hereinafter be referred to as the "lens"; however, this term should be broadly interpreted as encompassing various types of projection systems, including refractive optics, reflective optics, and catadioptric systems, for example. The radiation system may also include components operating according to any of these design types for directing, shaping or controlling the projection beam of radiation, and

such components may also be referred to below, collectively or singularly, as a “lens”. Further, the lithographic apparatus may be of a type having two or more substrate tables (and/or two or more mask tables). In such “multiple stage” devices the additional tables may be used in parallel, or preparatory steps may be carried out on one or more tables while one or more other tables are being used for exposures. Twin stage lithographic apparatus are described, for example, in US 5,969,441, incorporated herein by reference.

[05] The photolithographic masks referred to above comprise geometric patterns corresponding to the circuit components to be integrated onto a silicon wafer. The patterns used to create such masks are generated utilizing CAD (computer-aided design) programs, this process often being referred to as EDA (electronic design automation). Most CAD programs follow a set of predetermined design rules in order to create functional masks. These rules are set by processing and design limitations. For example, design rules define the space tolerance between circuit devices (such as gates, capacitors, etc.) or interconnect lines, so as to ensure that the circuit devices or lines do not interact with one another in an undesirable way. The design rule limitations are typically referred to as "critical dimensions" (CD). A critical dimension of a circuit can be defined as the smallest width of a line or hole or the smallest space between two lines or two holes. Thus, the CD determines the overall size and density of the designed circuit. Of course, one of the goals in integrated circuit fabrication is to faithfully reproduce the original circuit design on the wafer (via the mask).

[06] Another goal is to be able to utilize the same “process” for imaging a given pattern with different lithography systems (e.g., scanners) without having to expend considerable amounts of time and resources determining the necessary settings of each lithography system

to achieve optimal/acceptable imaging performance. As is known, designers/engineers spend a considerable amount of time and money determining the optimal settings of a lithography system (e.g., scanner), which include numerical aperture (NA), σ_{in} , σ_{out} , etc., when initially setting up a given process to work with a particular scanner so that the resulting image satisfies the design requirements. Indeed, this is often a trial and error process wherein the scanner settings are selected and the desired pattern is imaged and then measured to determine if the resulting image is within specified tolerances. If not, the scanner settings are adjusted and the pattern is imaged once again and measured. This process is repeated until the resulting image is within the specified tolerances.

[07] However, as each scanner, even identical model types, exhibit different optical proximity effects (OPEs) when imaging a pattern, the actual pattern imaged on the substrate differs from scanner to scanner due to the different OPEs. For example, different OPEs associated with given scanners can introduce significant CD variations through pitch. As such, it is not feasible to simply utilize a new scanner at the nominal settings to image a given pattern, as the resulting image can vary considerably from the desired target. Thus, if it is desirable to utilize a different scanner to print a given pattern, the engineers must optimize or tune the new scanner, so that the resulting image satisfies the design requirements. Currently, this is typically accomplished by a trial and error process, which as noted above, is both expensive and time consuming.

[08] As such, there is a need for a method for optimizing a process for imaging a given pattern that allows the process to be utilized with different lithography systems that does not require a trial and error process to be performed to optimize the process and scanner settings

for each individual scanner. In other words, there is a need for a method for optimizing the imaging performance of multiple scanners with respect to a given target mask that does not require a trial and error optimization process.

Summary

[09] Accordingly, the present invention relates to a method for tuning lithography systems so as to allow different lithography systems to image a given target pattern utilizing a known process that does not require a trial and error process to be performed to optimize the process and lithography system settings for each individual lithography system.

[10] More specifically, the present invention relates to a model-based tuning method for tuning a first lithography system utilizing a reference lithography system, each of which has tunable parameters for controlling imaging performance. The method includes the steps of defining a test pattern and an imaging model; imaging the test pattern utilizing the reference lithography system and measuring the imaging results; imaging the test pattern utilizing the first lithography system and measuring the imaging results; calibrating the imaging model utilizing the imaging results corresponding to the reference lithography system, where the calibrated imaging model has a first set of parameter values; tuning the calibrated imaging model utilizing the imaging results corresponding to the first lithography system, where the tuned calibrated model has a second set of parameter values; and adjusting the parameters of the first lithography system based on a difference between the first set of parameter values and the second set of parameter values.

[11] The present invention also relates to a method of tuning a lithography system utilizing an imaging model, where both the lithography system and the imaging model each have

tunable parameters for controlling imaging performance. The method includes the steps of defining a test pattern; imaging the test pattern utilizing the lithography system and measuring the imaging results, where the lithography system has a first set of parameter values; tuning the imaging model utilizing the imaging results corresponding to the lithography system, the tuned imaging model having a second set of parameter values; adjusting the first set of parameters of the lithography system based on a difference between the first set of parameter values and the second set of parameter values.

[12] In another embodiment, the present invention relates to a method of tuning a lithography system utilizing a target pattern, where the lithography system has tunable parameters for controlling imaging performance. The method includes the steps of defining a test pattern and an imaging model; imaging the target pattern utilizing the first lithography system and measuring imaging results, simulating the imaging of the target pattern utilizing the imaging model and determining simulated imaging results, the imaging model having a first set of parameter values; determining target wafer data based on the simulated imaging results and a difference between the imaging results and the target pattern, and tuning the imaging model utilizing the target wafer data; where the tuned imaging model has a second set of parameter values; adjusting the tunable parameters of the lithography system based on a difference between the first set of parameter values and the second set of parameter values.

[13] The present invention provides significant advantages over prior art methods. Most importantly, the present invention provides a systematic and cost effective model-based tuning method for the optimization of imaging performance and OPE matching between different lithography systems, including scanners, which are being utilized to image the same

target pattern. As a result, the method readily allows performance matching between different scanners of the same model as well as for performance matching between different model scanners.

[14] Additional advantages of the present invention will become apparent to those skilled in the art from the following detailed description of exemplary embodiments of the present invention.

[15] Although specific reference may be made in this text to the use of the invention in the manufacture of ICs, it should be explicitly understood that the invention has many other possible applications. For example, it may be employed in the manufacture of integrated optical systems, guidance and detection patterns for magnetic domain memories, liquid-crystal display panels, thin-film magnetic heads, etc. The skilled artisan will appreciate that, in the context of such alternative applications, any use of the terms "reticle", "wafer" or "die" in this text should be considered as being replaced by the more general terms "mask", "substrate" and "target portion", respectively.

[16] In the present document, the terms "radiation" and "beam" are used to encompass all types of electromagnetic radiation, including ultraviolet radiation (*e.g.* with a wavelength of 365, 248, 193, 157 or 126 nm) and EUV (extreme ultra-violet radiation, *e.g.* having a wavelength in the range 5-20 nm).

[17] The term mask as employed in this text may be broadly interpreted as referring to generic patterning means that can be used to endow an incoming radiation beam with a patterned cross-section, corresponding to a pattern that is to be created in a target portion of the substrate; the term "light valve" can also be used in this context. Besides the classic mask

(transmissive or reflective; binary, phase-shifting, hybrid, etc.), examples of other such patterning means include:

- a programmable mirror array. An example of such a device is a matrix-addressable surface having a viscoelastic control layer and a reflective surface. The basic principle behind such an apparatus is that (for example) addressed areas of the reflective surface reflect incident light as diffracted light, whereas unaddressed areas reflect incident light as undiffracted light. Using an appropriate filter, the said undiffracted light can be filtered out of the reflected beam, leaving only the diffracted light behind; in this manner, the beam becomes patterned according to the addressing pattern of the matrix-addressable surface. The required matrix addressing can be performed using suitable electronic means. More information on such mirror arrays can be gleaned, for example, from United States Patents US 5,296,891 and US 5,523,193, which are incorporated herein by reference.

- a programmable LCD array. An example of such a construction is given in United States Patent US 5,229,872, which is incorporated herein by reference.

[18] The invention itself, together with further objects and advantages, can be better understood by reference to the following detailed description and the accompanying schematic drawings.

Brief Description of the Drawings

[19] Fig. 1 is an exemplary flowchart illustrating the method of the present invention.

[20] Fig. 2 illustrates a graphical representation of the process set forth in Fig. 1.

[21] Fig. 3 is a first graphical representation of the space spanned by the tunable and non-tunable parameters of the imaging model illustrating the example where the tunable parameters have an orthogonal affect on the non-tunable parameters.

[22] Fig. 4 is a second graphical representation of the space spanned by the tunable and non-tunable parameters of the imaging model illustrating the example where the tunable parameters do not have an orthogonal affect on the non-tunable parameters.

[23] Fig. 5 is a block diagram graphically illustrating the components involved in the model-based scanner tuning process of the present invention.

[24] Fig. 6 illustrates a graphical representation of another example of the first embodiment of the present invention.

[25] Fig. 7 illustrates a graphical representation of a second embodiment the method of the present invention.

[26] Fig. 8 illustrates a graphical representation of a third embodiment the method of the present invention.

[27] Fig. 9 is a block diagram that illustrates a computer system which can assist in the implementation of the model-based tuning process of the present invention.

[28] Fig. 10 schematically depicts a lithographic projection apparatus suitable for use with the method of the present invention.

Description

[29] Fig. 1 is an exemplary flowchart illustrating the model-based scanner tuning method of the present invention. As explained in detailed below, the method of the present invention allows for simultaneous optimization of imaging performance and OPE matching between

different lithography systems, including scanners, which are being utilized to image the same target pattern.

[30] Referring to Fig. 1, the first step (Step 10) in the process is to define the test pattern that is to be utilized to calibrate the model for a reference scanner. A suitable test pattern (also referred to as model calibration gauge patterns) may be utilized. The test pattern utilized should sufficiently represent the features to be imaged so that a robust model capable of accurately predicting imaging performance of the lithography system may be generated. Such test patterns can be readily generated/selected by those of skill in the art once the target pattern or application is determined. It is noted that it is also possible to utilize the target pattern to be imaged as the test pattern in the calibration process.

[31] Once the test pattern is defined, in the next step (Step 20) each scanner to be tuned (including the reference scanner) images the test pattern and the imaging results are measured. When imaging the test pattern, the parameters, P , of each scanner is set at a predefined nominal value, which is chosen during the process design. Preferably, the same nominal value for each parameter is utilized for each scanner during the imaging of the test pattern. Next, the resulting features in each of the imaged wafers are measured so as to obtain wafer data indicative of the imaging performance of the given scanner. For the purposes of facilitating the following explanation, the measured wafer data (WD) is designated WD_1, WD_2 ... WD_n, where WD_1 corresponds to the wafer data/imaging result of the first scanner, WD_2 corresponds to the wafer data/imaging result of the second scanner and so on up to the nth scanner. It is noted the measurement of the wafer data may be made, for example, by performing various CD measurements or measuring the entire

contour of the imaged feature which can be performed utilizing SEM. Typically, the necessary measurements of the wafer data will be defined by the model being utilized to represent the imaging process, plus the design rules defining the relevant pattern space.

[32] Once the wafer data is measured, the next step (Step 30) is to calibrate the model utilizing the wafer data associated with the reference scanner. The model parameters associated with the reference scanner are designated MP_R, and include tunable and non-tunable parameters. As is known, during the calibration process (which is an iterative process), the non-tunable parameters are fixed and the tunable parameters are adjusted until the image generated by the model (i.e., the simulated result) matches the actual imaging result produced by the reference scanner. Thus, the model parameters MP_R are adjusted (i.e., calibrated) such that the imaging results produced by the model equal the actual wafer data associated with the reference scanner WD_R within some predefined error criteria or the best match possible. It is noted that any suitable model for simulating the imaging performance of a scanner may be utilized in this process, for example, the Tachyon FEM (focus-exposure-model) or LithoCruiserTM offered by ASML. It is further noted that any one of the scanners to be tuned and the associated wafer data, WD_1 ...WD-n, may be utilized to calibrate the model. As another alternative, it is possible to average the wafer data for each of the scanners (WD_1 WD-n) for each necessary measurement to be input into the model, and utilize these average values as the reference wafer data utilized to calibrate the model parameters MP_R.

[33] In the next step (Step 40), for each scanner to be tuned, the model calibrated in the previous step having parameters MP_R is tuned in accordance with the wafer data WD_i

associated with the given scanner (i.e., scanner i). More specifically, utilizing model parameters MP_R as a start point, the non-tunable parameters of MP_R remain fixed and the variable or tunable parameters in MP_R are tuned so that the model for the given scanner, MP_Ri, produces an imaging result which is the same as the actual wafer data WD_i associated with the given scanner (i) within some predefined error criteria or the best match possible. This step is a standard calibration step, which is an iterative process in which the variable model parameters in MP_Ri are adjusted until the output of the imaging model corresponds to the desired image (WD_i). Step 40 is performed for each scanner to be tuned.

[34] Once the model MP_R is tuned for each of the scanners, thereby creating “n” models MP_R1 MP_Rn (where n is the number of scanners), in Step 50, each of the scanners is tuned from the nominal parameter values that were utilized to generate the initial wafer data WD_1 WD_n utilizing the parameter values of the reference model MP_R and the adjusted model parameters MP_Ri. More specifically, the parameters Pi of each scanner are tuned in accordance with the following equation:

[35]
$$P_i = P_i (\text{nominal}) + MP_R - MP_Ri,$$

[36] where Pi (nominal) corresponds to the nominal parameters utilized to generate the initial wafer data WD_i; MP_R corresponds to parameters of the calibrated model for the reference scanner, and MP_Ri corresponds to parameters of the calibrated model for the scanner(i). The resulting parameters, Pi, are then utilized to tune the corresponding scanner(i).

[37] It is noted that in the foregoing process, only like parameters are subtracted from one another when executing the foregoing equation. For example, assuming the tunable

parameters are $(T_1, T_2 \dots T_m)$, and their values for the reference model are $(T_{1r}, T_{2r} \dots T_{mr})$, and for scanner(i) are $(T_{1i}, T_{2i} \dots T_{mi})$, the nominal values, P_i , of these parameters are tuned by a delta equal to $(T_{1r}-T_{1i}, T_{2r}-T_{2i} \dots T_{mr}-T_{mi})$. By performing the foregoing operation it is possible to reduce/minimize the difference between the models such that the two scanners perform in the substantially same manner. Thus, the foregoing process provides a systematic process which allows for the matching of similar scanners (same type and model of machines) as well as for the matching the imaging performance of different scanners (i.e., different models and/or manufacturer). It is noted that the tunable parameters typically include, but are not limited to focus, dose illumination sigma, stage tilt, etc. The fixed parameters include, for example, but are not limited to, resist parameters and etch parameters.

[38] Fig. 2 illustrates a graphical representation of the foregoing process. As shown in Fig. 2, the process effectively computes the difference between two virtual scanners (MP_R and MP_{Ri}) and then utilizes this computed difference to tune the actual scanners. Figs. 3 and 4 are graphical representations of the space spanned by the tunable and non-tunable parameters. Fig. 3 illustrates the example where the tunable parameters have an orthogonal effect on the non-tunable parameters, and Fig. 4 illustrates an example where the tunable parameters do not have an orthogonal effect on the non-tunable parameters. As shown, any residual errors are orthogonal to the space spanned by the tunable parameters. In the case where the effects from tunable and non-tunable parameters are not orthogonal, it is possible to compensate to some degree the differences caused by the non-tunable parameters, through tuning the value of the tunable parameters.

[39] Fig. 5 is a block diagram graphically illustrating the components involved in the model-based scanner tuning process of the present invention. As shown, the components include a tuning target and a scanner to be tuned. As is clear from the foregoing, while there is always at least one scanner to be tuned, it is possible that there would be multiple scanners to be tuned. The scanner to be tuned is always a physical scanner (i.e., an actual device). However, as explained in further detailed below, the tuning target may be either a real scanner or a virtual scanner or contour. As detailed above, the tuning amount is the difference between the virtual scanner (i.e., model) of the scanner to be tuned and the virtual scanner (i.e., model) of the tuning target. In the model-based tuning process disclosed herein, the model (i.e., virtual scanner) provides the link between the tuning target and the scanner to be tuned.

[40] As noted, it is possible to utilize at least three different tuning targets in the foregoing process. The three possibilities are a physical scanner, a virtual scanner and a desired wafer contour. Examples of the use of the three different tuning targets are described below. The first option is to utilize a physical scanner as the tuning target. A physical scanner was utilized in the example detailed above. Utilizing a physical scanner as the tuning target provides for OPE matching between scanners. In addition, it allows for matching between like scanner units (e.g., SN1 SNn), where SN represents the same scanner model. It also allows for matching between different scanner types from the same manufacturer, as well as for matching between scanners from different manufacturers.

[41] When performing model-based scanner tuning between different scanner devices, the same process as set forth above in Fig. 1 is utilized. As an example, assuming the to be tuned

scanner is scanner A and the tuning target is scanner R, the first step is to print test patterns utilizing nominal scanner parameters, P , on both scanner A and scanner R so as to generate wafer data WD_A and WD_R . Then, the imaging model being utilized is calibrated for scanner R such that the results of the model accurately correspond to WD_R within some predefined criteria. Next, the non-tunable parameters in the model MP_R are fixed and utilized in the model and the tunable parameters are adjusted such that the results of the model (now referred to as MP_RA) associated with scanner A correspond to WD_A within some predefined error criteria. Then, in the final step, the parameters of scanner A, referred to as PA , are tuned from the nominal parameters, P , utilized to produce WD_A to “ $P + MP_R - MP_RA$ ”. Fig. 6 provides a graphical representation of this process.

[42] As an alternative to the foregoing, it is also possible to calibrate the model for scanner A such that the results of the model accurately correspond to WD_A with some predefined error criteria, and then fix the non-tunable parameters in the model MP_A and utilize these parameters in model MP_AR . The tunable parameters of MP_AR are then adjusted such that the results of the model MP_AR associated with scanner R correspond to WD_R within some predefined error criteria. Then, in the final step, the parameters of scanner A, referred to as PA , are tuned from the nominal parameters, P , utilized to produce WD_A to “ $P + MP_AR - MP_A$ ”. In yet another variation, it is also possible to utilize an average of the two foregoing processes when determining the amount to tune scanner A. These processes can also be utilized when tuning scanners from different manufacturers.

[43] Next, an example is provided of utilizing a virtual scanner (i.e., model) as the tuning target. The first step in the process is to obtain a known model, referred to as MP_K .

Preferably, the model MP_K is calibrated for the given process being utilized and produces results which are within some predefined error criteria. The next step is to print test patterns with the current scanner C (i.e., the scanner to be tuned) and measure the resulting wafer data, thereby generating data WD_C. Next, all of the non-tunable parameters in model MP_K are fixed and the tunable parameters of model MP_K are adjusted so that the results of the model, now referred to as MP_KC, correspond to WD_C within some predefined error criteria. Then, in the final step of the process, the settings of scanner C are tuned from the current settings “PC”, which were utilized to initially produce WD_C, to “PC + MP_K – MP_KC”. This process can be useful for correction of drift (e.g., laser drift) within the scanner, and well as correction of drift in other lithography processes (e.g., resist process, etch process, etc.) The process is also useful for optimizing a given scanner for a given OPC process, where the OPC process is effectively incorporated into the model to which the scanner will be tuned. It is noted that it is possible to utilize an FEM model in the foregoing process as the reference model. Further, the model may consider both in focus and defocus conditions. A graphical representation of this process is illustrated in Fig. 7.

[44] As noted above, it is also possible to utilize a wafer contour as the tuning target. This process is useful for optimizing a scanner for a specific device mask to optimize CDU (critical dimension uniformity), as well as for optimizing a scanner for a known mask error. The first step in the process is to image/print a specific device mask and measure the data, which is referred to as WD_M. The mask is imaged utilizing the scanner to be tuned, where the parameters of the scanner are initially set to nominal values “PC”. It is noted that the target or desired wafer data, which obtains optimal CDU is referred to as WD_T. In the next

step, utilizing a given model (as with the examples above, any suitable simulation model may be utilized) which is referred to as MP_C, the target pattern is processed by the model MP_C and produces simulated wafer data WD_C. Next, the tuning of the model MP_C necessary to obtain the desired simulated imaging result, which is referred to as WD_CT, is determined by the equation:

$$WD_{CT} = WD_C + (WD_T - WD_M)$$

[45] Thereafter, all of the non-tunable parameters in model MP_C are fixed and the tunable parameters are tuned so that the model, which is now referred to as MP_CT, produces a simulated imaging result which corresponds to WD_CT. In the final step, the scanner to be tuned is tuned from the nominal settings of “PC” to PC + MP_CT – MP_C”. Fig. 8 illustrates a graphical representation of the foregoing process.

[46] It is noted that the foregoing process can be useful for optimizing CDU across the chip after the mask is made for a number of critical patterns. It is also noted that in the foregoing process, a limitation on the tuning may be necessary to prevent excessive tuning for the limited device patterns considered in the CDU. For example, a test pattern may be mixed in order to anchor the tuning process.

[47] This third category of scanner tuning also allows for scanner optimization for a given mask error. More specifically, the process entails obtaining a current model with a known mask error, referred to as MP_M. It is noted that in the given example, MP_M is essentially the FEM with a known non-tunable parameter (mask error) changed by a known amount. Then, utilizing the model MP_M, without the mask error, simulate the test pattern (i.e., wafer contour) so as to obtain simulated wafer data with mask error, WD_T. Next, all non-tunable

parameters in model MP_M are fixed, and the tunable parameters are adjusted such that the model, now referred to as MP_MT, produces a simulated imaging result based on the test pattern which corresponds to WD_T. In the final step, the scanner to be tuned is tuned from the nominal settings of “PC” to $PC + MP_MT - MP_M$. This process allows the scanner to be tuned to image a mask with a known systematic error.

[48] As noted above, the model-based scanner tuning provides numerous advantages over prior art methods. Most importantly, the present invention provides a systematic and cost effective method for the optimization of imaging performance and OPE matching between different lithography systems, including scanners, which are being utilized to image the same target pattern. As a result, the present invention readily allows performance matching between different scanners of the same model as well as for performance matching between different model scanners.

[49] The methods of the present invention also allow scanners to be tuned to a known model or a known wafer contour (i.e., target pattern). These processes allow for, among other things, lithography process drift corrections, scanner optimization for a given OPC process, scanner optimization for a specific device mask in order to optimize CDU and scanner optimization for a known mask error.

[50] It is further noted that model separability is an important aspect of the model based tuning/matching/optimization process of the present invention. In other words, the total lithography behavior can be described accurately by adjusting only the tunable parameters. Brion’s focus-exposure-model “FEM” achieves separability across focus-exposure process window variation. Further, FEM can also achieve model separability with respect to many

other tunable parameters, such as, but not limited to, NA, illumination, etc., within a reasonable range of parameter change. If the tuning amount is too large such that it goes beyond the model separability range, the tuning can be achieved through two or more steps.

[51] It is also noted that if desired, the effect of the tuning on the pattern can be analyzed using an OPC verification tool such as Tachyon's LMC (Lithographic Manufacturability Check), since the model can quantitatively analyze the impact of the changes to the model (i.e., tuning) on the full chip patterns. The procedure for performing this check is as follows. First, use LMC to simulate full chip on-wafer contour using the models before and after tuning. Next, compare the difference between the two contours to analyze the differences between the two.

[52] With non-tunable parameters allowed to vary, it is also possible to quantitatively analyze the residual error's effect on the full chip pattern. The residual error is the difference between the after-tuning and tuning target. This can be accomplished by fitting the model for the wafer data, and allowing both tunable and non-tunable parameters to vary, i.e., fitting a full model based on the wafer data, and then using LMC to simulate full chip on-wafer contour using models which: (1) only allow tunable parameters to vary (i.e., the model coming out of the tuning procedure), and (2) allow both tunable and non-tunable parameters to vary (i.e., the model coming out of the above additional step). Once this is done, a comparison is made to identify the differences between the two contours. The difference between the contours is the residual error after tuning. If there are contour differences that are too large to be acceptable, the normal scanner tuning based on existing tunable

parameters is unable to achieve the tuning goal. Additional actions may be taken to enable more parameters to be tunable, or scanner changes may be required.

[53] Alternatives to the foregoing processes are also possible. As one example, when wafer data is available for both current scanner condition and tuning target condition, e.g., in the case of matching between two physical scanners without a prior model, an alternative embodiment is to perform joint calibration on the wafer data utilizing both current scanner condition and target scanner condition. This entails performing a joint model calibration process which allows non-tunable parameters to vary in the calibration process but forces them to be the same in both the current scanner condition and the target scanner condition, and which allows the tunable parameters to independently vary under both conditions. After the joint calibration, the difference between the tunable parameters of both conditions is the optimal tuning amount.

[54] Fig. 9 is a block diagram that illustrates a computer system 100 which can assist in the model-based scanner tuning method disclosed herein. Computer system 100 includes a bus 102 or other communication mechanism for communicating information, and a processor 104 coupled with bus 102 for processing information. Computer system 100 also includes a main memory 106, such as a random access memory (RAM) or other dynamic storage device, coupled to bus 102 for storing information and instructions to be executed by processor 104. Main memory 106 also may be used for storing temporary variables or other intermediate information during execution of instructions to be executed by processor 104. Computer system 100 further includes a read only memory (ROM) 108 or other static storage device coupled to bus 102 for storing static information and instructions for processor 104.

A storage device 110, such as a magnetic disk or optical disk, is provided and coupled to bus 102 for storing information and instructions.

[55] Computer system 100 may be coupled via bus 102 to a display 112, such as a cathode ray tube (CRT) or flat panel or touch panel display for displaying information to a computer user. An input device 114, including alphanumeric and other keys, is coupled to bus 102 for communicating information and command selections to processor 104. Another type of user input device is cursor control 116, such as a mouse, a trackball, or cursor direction keys for communicating direction information and command selections to processor 104 and for controlling cursor movement on display 112. This input device typically has two degrees of freedom in two axes, a first axis (e.g., x) and a second axis (e.g., y), that allows the device to specify positions in a plane. A touch panel (screen) display may also be used as an input device.

[56] According to one embodiment of the invention, portions of the scanner tuning process, for example, simulation operations, may be performed by computer system 100 in response to processor 104 executing one or more sequences of one or more instructions contained in main memory 106. Such instructions may be read into main memory 106 from another computer-readable medium, such as storage device 110. Execution of the sequences of instructions contained in main memory 106 causes processor 104 to perform the process steps described herein. One or more processors in a multi-processing arrangement may also be employed to execute the sequences of instructions contained in main memory 106. In alternative embodiments, hard-wired circuitry may be used in place of or in combination with

software instructions to implement the invention. Thus, embodiments of the invention are not limited to any specific combination of hardware circuitry and software.

[57] The term “computer-readable medium” as used herein refers to any medium that participates in providing instructions to processor 104 for execution. Such a medium may take many forms, including but not limited to, non-volatile media, volatile media, and transmission media. Non-volatile media include, for example, optical or magnetic disks, such as storage device 110. Volatile media include dynamic memory, such as main memory 106. Transmission media include coaxial cables, copper wire and fiber optics, including the wires that comprise bus 102. Transmission media can also take the form of acoustic or light waves, such as those generated during radio frequency (RF) and infrared (IR) data communications. Common forms of computer-readable media include, for example, a floppy disk, a flexible disk, hard disk, magnetic tape, any other magnetic medium, a CD-ROM, DVD, any other optical medium, punch cards, paper tape, any other physical medium with patterns of holes, a RAM, a PROM, and EPROM, a FLASH-EPROM, any other memory chip or cartridge, a carrier wave as described hereinafter, or any other medium from which a computer can read.

[58] Various forms of computer readable media may be involved in carrying one or more sequences of one or more instructions to processor 104 for execution. For example, the instructions may initially be borne on a magnetic disk of a remote computer. The remote computer can load the instructions into its dynamic memory and send the instructions over a telephone line using a modem. A modem local to computer system 100 can receive the data on the telephone line and use an infrared transmitter to convert the data to an infrared signal.

An infrared detector coupled to bus 102 can receive the data carried in the infrared signal and place the data on bus 102. Bus 102 carries the data to main memory 106, from which processor 104 retrieves and executes the instructions. The instructions received by main memory 106 may optionally be stored on storage device 110 either before or after execution by processor 104.

[59] Computer system 100 also preferably includes a communication interface 118 coupled to bus 102. Communication interface 118 provides a two-way data communication coupling to a network link 120 that is connected to a local network 122. For example, communication interface 118 may be an integrated services digital network (ISDN) card or a modem to provide a data communication connection to a corresponding type of telephone line. As another example, communication interface 118 may be a local area network (LAN) card to provide a data communication connection to a compatible LAN. Wireless links may also be implemented. In any such implementation, communication interface 118 sends and receives electrical, electromagnetic or optical signals that carry digital data streams representing various types of information.

[60] Network link 120 typically provides data communication through one or more networks to other data devices. For example, network link 120 may provide a connection through local network 122 to a host computer 124 or to data equipment operated by an Internet Service Provider (ISP) 126. ISP 126 in turn provides data communication services through the worldwide packet data communication network, now commonly referred to as the "Internet" 128. Local network 122 and Internet 128 both use electrical, electromagnetic or optical signals that carry digital data streams. The signals through the various networks

and the signals on network link 120 and through communication interface 118, which carry the digital data to and from computer system 100, are exemplary forms of carrier waves transporting the information.

[61] Computer system 100 can send messages and receive data, including program code, through the network(s), network link 120, and communication interface 118. In the Internet example, a server 130 might transmit a requested code for an application program through Internet 128, ISP 126, local network 122 and communication interface 118. In accordance with the invention, one such downloaded application provides for the illumination optimization of the embodiment, for example. The received code may be executed by processor 104 as it is received, and/or stored in storage device 110, or other non-volatile storage for later execution. In this manner, computer system 100 may obtain application code in the form of a carrier wave.

[62] Fig. 10 schematically depicts an exemplary lithographic projection apparatus that could be tuned utilizing the process of present invention. The apparatus comprises:

- a radiation system Ex, IL, for supplying a projection beam PB of radiation. In this particular case, the radiation system also comprises a radiation source LA;
- a first object table (mask table) MT provided with a mask holder for holding a mask MA (*e.g.*, a reticle), and connected to first positioning means for accurately positioning the mask with respect to item PL;
- a second object table (substrate table) WT provided with a substrate holder for holding a substrate W (*e.g.*, a resist-coated silicon wafer), and connected to second positioning means for accurately positioning the substrate with respect to item PL;

- a projection system (“lens”) PL (*e.g.*, a refractive, catoptric or catadioptric optical system) for imaging an irradiated portion of the mask MA onto a target portion C (*e.g.*, comprising one or more dies) of the substrate W.

[63] As depicted herein, the apparatus is of a transmissive type (*i.e.*, has a transmissive mask). However, in general, it may also be of a reflective type, for example (with a reflective mask). Alternatively, the apparatus may employ another kind of patterning means as an alternative to the use of a mask; examples include a programmable mirror array or LCD matrix.

[64] The source LA (*e.g.*, a mercury lamp or excimer laser) produces a beam of radiation. This beam is fed into an illumination system (illuminator) IL, either directly or after having traversed conditioning means, such as a beam expander Ex, for example. The illuminator IL may comprise adjusting means AM for setting the outer and/or inner radial extent (commonly referred to as σ -outer and σ -inner, respectively) of the intensity distribution in the beam. In addition, it will generally comprise various other components, such as an integrator IN and a condenser CO. In this way, the beam PB impinging on the mask MA has a desired uniformity and intensity distribution in its cross-section.

[65] It should be noted with regard to Fig. 10 that the source LA may be within the housing of the lithographic projection apparatus (as is often the case when the source LA is a mercury lamp, for example), but that it may also be remote from the lithographic projection apparatus, the radiation beam that it produces being led into the apparatus (*e.g.*, with the aid of suitable directing mirrors); this latter scenario is often the case when the source LA is an

excimer laser (*e.g.*, based on KrF, ArF or F₂ lasing). The current invention encompasses at least both of these scenarios.

[66] The beam PB subsequently intercepts the mask MA, which is held on a mask table MT. Having traversed the mask MA, the beam PB passes through the lens PL, which focuses the beam PB onto a target portion C of the substrate W. With the aid of the second positioning means (and interferometric measuring means IF), the substrate table WT can be moved accurately, *e.g.* so as to position different target portions C in the path of the beam PB. Similarly, the first positioning means can be used to accurately position the mask MA with respect to the path of the beam PB, *e.g.*, after mechanical retrieval of the mask MA from a mask library, or during a scan. In general, movement of the object tables MT, WT will be realized with the aid of a long-stroke module (coarse positioning) and a short-stroke module (fine positioning), which are not explicitly depicted in Fig. 10. However, in the case of a wafer stepper (as opposed to a step-and-scan tool) the mask table MT may just be connected to a short stroke actuator, or may be fixed.

[67] The depicted tool can be used in two different modes:

- In step mode, the mask table MT is kept essentially stationary, and an entire mask image is projected in one go (*i.e.*, a single “flash”) onto a target portion C. The substrate table WT is then shifted in the x and/or y directions so that a different target portion C can be irradiated by the beam PB;

- In scan mode, essentially the same scenario applies, except that a given target portion C is not exposed in a single “flash”. Instead, the mask table MT is movable in a given direction (the so-called “scan direction”, *e.g.*, the y direction) with a speed v , so that

the projection beam PB is caused to scan over a mask image; concurrently, the substrate table WT is simultaneously moved in the same or opposite direction at a speed $V = Mv$, in which M is the magnification of the lens PL (typically, $M = 1/4$ or $1/5$). In this manner, a relatively large target portion C can be exposed, without having to compromise on resolution.

[68] The concepts disclosed herein may simulate or mathematically model any generic imaging system for imaging sub wavelength features, and may be especially useful with emerging imaging technologies capable of producing wavelengths of an increasingly smaller size. Emerging technologies already in use include EUV (extreme ultra violet) lithography that is capable of producing a 193nm wavelength with the use of a ArF laser, and even a 157nm wavelength with the use of a Fluorine laser. Moreover, EUV lithography is capable of producing wavelengths within a range of 20-5nm by using a synchrotron or by hitting a material (either solid or a plasma) with high energy electrons in order to produce photons within this range. Because most materials are absorptive within this range, illumination may be produced by reflective mirrors with a multi-stack of Molybdenum and Silicon. The multi-stack mirror has a 40 layer pairs of Molybdenum and Silicon where the thickness of each layer is a quarter wavelength. Even smaller wavelengths may be produced with X-ray lithography. Typically, a synchrotron is used to produce an X-ray wavelength. Since most material is absorptive at x-ray wavelengths, a thin piece of absorbing material defines where features would print (positive resist) or not print (negative resist).

[69] While the concepts disclosed herein may be used for imaging on a substrate such as a silicon wafer, it shall be understood that the disclosed concepts may be used with any type of

lithographic imaging systems, *e.g.*, those used for imaging on substrates other than silicon wafers.

[70] Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

CLAIMS

1. A method of tuning a lithography system utilizing an imaging model, said lithography system and said imaging model each having tunable parameters for controlling imaging performance, said method comprising the steps of:
 - defining a test pattern;
 - imaging a test pattern utilizing said lithography system and measuring the imaging results, said lithography system having a first set of parameter values;
 - tuning said imaging model utilizing said imaging results corresponding to said lithography system, said tuned imaging model having a second set of parameter values;
 - adjusting said first set of parameters of said lithography system based on a difference between said first set of parameter values and said second set of parameter values.
2. A method of tuning a lithography system according to claim 1, wherein said lithography system comprises a scanner.
3. A method of tuning a lithography system according to claim 1, wherein said imaging model further comprises fixed parameters.
4. A method of tuning a lithography system according to claim 1, wherein said tunable parameters of said lithography system correspond to said tunable parameters of said imaging model.

5. A method of tuning a lithography system according to claim 1, wherein said tunable parameters of said lithography system are set at a nominal value when imaging said test pattern