Semiconductor device and manufacturing method thereof

ABSTRACT OF THE DISCLOSURE

It is an object of the present invention to provide an SGT manufacturing method capable of obtaining a structure for reducing resistances of a source and a drain, a structure for reducing a parasitic capacitance, a desired gate length, desired configurations of the source and drain, and a desired diameter of a columnar semiconductor. In order to achieve the object, the present invention provides a method of manufacturing a semiconductor device, which comprises the steps of: forming a first columnar semiconductor layer on a substrate, and forming a first flat semiconductor layer in an upper portion of the substrate lying under the first columnar semiconductor layer; forming a first semiconductor layer of a second conductive type in a lower portion of the first columnar semiconductor layer and an entirety or an upper portion of the first flat semiconductor layer; forming a first insulating film around a lower sidewall of the first columnar silicon layer and above the first flat semiconductor layer; forming a gate insulating film and a gate electrode around the first columnar silicon layer; forming a sidewall-shaped second insulating film to surround an upper sidewall of the first columnar silicon layer while contacting an upper surface of the gate electrode and to surround a sidewall of the gate electrode; forming a second semiconductor layer of the second conductive type in an upper portion of the first columnar silicon layer, and forming a semiconductor layer of a first conductive type between the first semiconductor layer of the second conductive type and the second semiconductor layer of the second conductive type; and forming a metal-semiconductor compound on each of an upper surface of the first semiconductor layer of the second conductive type and an upper surface of the second semiconductor layer of the second conductive type, wherein the first insulating film has a thickness larger than that of the gate insulating film formed around the first columnar silicon layer.

Figures 41(a) & 41(b)