

SPECIFICATION

Distributed control digital switching system

5 This invention relates generally to distributed control digital communication systems.

In modern telephone switching systems, it is required for data representative of the status, of the subscriber lines and trunks served by such a system, together with the required actions in response to various lines' and trunks' status conditions to be stored. Representative data is path set-up through the network, subscriber class of service, trunk class of call, directory number (DN) to equipment number (EN) translations, EN-to-DN translations, etc. In known centralised control systems, this data is available in a common memory, which is duplicated for security and reliability purposes and is accessible by common control computers for serial operations upon the extracted data. Known multiprocessing common control systems need more than one processor to access the common memory to obtain data at the same time, resulting in interference problems and an effective loss of throughput, which increases as the number of processors increases.

Decentralisation of control and distributed data processing has evolved in the light of the problems inherent in a centrally controlled system. One known switching system wherein stored-program controllers are distributed throughout the system is described in U.S. Patent No. 3,974,343. Another prior art progressively-controlled distributed-control switching system is described in U.S. Patent No. 3,860,761.

Prior art systems have concentrated upon obtaining a high efficiency for processing, with multiprocessing to give increased processing capability; however, undesirable interaction may occur between software packages wherein the modification or addition of features could interfere with the current working of other features in an unpredictable manner. A major reason for the problems of prior art common control architectures, whether or not multiple processors are used, is that stored program control processing functions are shared in time between a plurality of tasks which randomly occur on demand of the originating and terminating traffic, which does not provide for an efficient operation of the stored software packages.

50 An object of the invention is to provide an improved processor-controlled system in which some at least of the disadvantages of known systems are minimised or avoided.

According to the present invention there is provided a distributed control digital communication system including a number of terminal units for interfacing a number of PCM communication terminals each associated with one of a number of subscribers' lines to one or more common communication paths, wherein:

(a) each of said PCM terminals is adapted to convey digitized speech in frames with each said frame containing a number of channels usable for the conveyance of said digitized speech;

65 (b) in-channel path selection control signals

derived by respective ones of a group of processors each of which provides processing functions for a group of said PCM terminals are multiplexed with the digitized speech so that the same physical paths are used to convey digitized speech and said in-channel path selection control signals;

(c) a digital switching network is coupled to a number of paths such as said common communication paths for bit asynchronously interconnecting the PCM terminals through paths set up through the switching network in response to said path selection control signals; and

(d) means is provided at each of said terminal units for selectively multiplexing said digitized speech and said in-channel path selection control signals on the appropriate one of the common communication paths such that the path selection control signals precede the digitized speech in channels designated by said path selection control signals on the said common communication path.

In a preferred embodiment, a switching network architecture is provided wherein not only are multi-channel digitised PCM speech samples or data between one terminal and another carried by the network, but the same channels also convey the path selection and other control signals for the distributed control, which are carried on the same transmission paths through the network. Every terminal, whether carrying data from a line or trunk or other data source is serviced by a terminal unit having all of the facilities and control logic to communicate with other terminals via other terminal units, and to establish, maintain and terminate paths through the switching network to other terminal units. All inter-processor communication occurs via the switching network. A group switch having switching elements providing both time and space switching is provided which is modularly expandable without disruption of service or rearrangement of existing interconnections to provide a growth from approximately 120 to 128,000 or more terminals, to accommodate increasing traffic load while acting as an effectively non-blocking network. A failed switch element is easily and automatically identified, isolated and bypassed by traffic.

In such a system a group switch is provided in which multiport single-sided switching elements are arrangeable in any inlet/outlet configuration, e.g. as 8X8 switches containing space and time switching in an "ST" configuration. Path selection in the network of switching elements is performed by control commands carried by the speech channels. Further, there are reflection switching facilities, so that a path set up, for example, in a stage two switch, when no stage three is yet provided, will be reflected back via the speech path to form a folded network, while the outlets of the stage two switch remain available for future connection for network expansion. The expansion to a third stage would then require connection of the available outlets of stage two to the inlets of the future stage three switch.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which.

130 Figure 1 is a block diagram of a distributed control

system embodying the invention;

Figure 2 shows the modular expandability of the switching network of Figure 1;

Figure 3 is a simplified block diagram of a multi-port switching element used in the network of Figure 1;

Figure 4 shows one plane of a switching network of Figure 1;

Figures 5A, 5B, 5C and 5D illustrate the expansion of the switching network;

Figure 6 is a block diagram of a line terminal subunit;

Figure 7 is a block diagram of a trunk terminal subunit;

Figure 8 is a simplified illustration of the TDM bus of the multiport switching element used in the present system;

Figure 9 is a block diagram of the logic of one port of the element of Figure 8;

Figures 10(a), 10(b), 10(c), 10(d) and 10(e) illustrate channel word formats used in the present system;

Figures 11(a), 11(b), 11(c) and 11(d) illustrate additional channel word formats used in the present system;

Figure 12 illustrates a typical connection between terminals through the switching network of Figure 1;

Figures 13(a), 13(b), 13(c), 13(d), 13(e), 13(f), 13(g) and 13(h) are timing diagrams illustrative of the operation of the switching elements of the present system;

Figures 14(a), 14(b), 14(c), 14(d) and 14(e) are more detailed timing diagrams illustrative of the operation of the switching elements of the present system;

Figure 15 illustrates the TDM bus lines of a switching element of the present system.

Features of the systems described herein which are not claimed herein are claimed separately in application No. 7906265 (No. 2 016 867) from which the present application was divided, and in No.

7924308 (No. 2 021 901) also divided from application No. 7906265 (No. 2 016 867). Further features of these systems are also claimed in our applications No. 7906324 (No. 2 016 865), No. 7936366 (No. 2 029 671), and No. 7906266 (No. 2 010 866).

Figure 1 is a system block diagram of a distributed-control digital switching system with a group switch 10 via which connections between terminal units are switched to provide transmission paths for coupling data between terminals serviced by the terminal units.

As the term is used herein, a terminal unit is a subsystem for servicing a group of terminals which terminate on one first stage switch in every plane of the group switch. Each terminal unit includes eight access switches through which data from the terminals is coupled to and from the group switch 10.

As the term is used herein, a terminal subunit is a subsystem of a terminal unit for servicing a group of terminals which terminate on one security pair of access switches. Each terminal unit contains four security pairs of access switches. The PCM data at each terminal is derived, for example, from telephone line circuits such as described in detail in our copending application No. 6797/78.

Terminal units 12, 14 and 16 are shown as exam-

ples; however up to 128 or more terminal units may be switched by the group switch 10. Each terminal unit can interface, for example, 1920 subscriber line terminals or 480 trunks to four terminal subunits, with terminal subunits 18, 20, 22 and 24 illustrated for terminal unit 12. Thirty-two channel PCM multiplexed digital lines having multiplexed thereon thirty bidirectional subscriber lines are coupled to the terminal units.

Each terminal unit such as unit 12 is coupled to group switch 10 by multiplexed transmission links, each comprising two unidirectional transmission paths. Each terminal subunit 18, 20, 22 and 24 of terminal unit 12 is coupled to each plane of the group switch 10 by two such links. Thus for terminal subunit 18, links 26 and 28 couple subunit 18 to plane 0 of group switch 10 and links 30 and 32 couple subunit 18 to plane 3 of group switch 10. Similarly, subunit 18 is coupled to planes 1 and 2 of the group switch 10 by similar links. Subunits 20, 22 and 24 are also coupled to every plane of the group switch in a similar manner.

Each transmission link 26, 28, 30 and 32 shown for terminal subunit 18 is bidirectional as it includes a pair of unidirectional transmission paths, each path being dedicated to one direction of data flow. Each unidirectional path carries thirty-two channels of digital information time division multiplexed (TDM) thereon in bit-serial format. Each frame of TDM format has thirty-two channels with each channel having 16-bits of information, and the bit transmission rate is 4.096 Mb/s. This transmission rate is clocked throughout the system, so the system may be characterised as rate synchronous.

Since, as will be explained, the system is phase-asynchronous, there is no required phase relationship as to which data bits in a frame are received by different switching elements or by the different ports in a single switching element. This rate synchronous and phase asynchronous system is implemented in the group switch and in the access switches by multi-port switching elements. When digital speech samples are transmitted anywhere within the system to or from a particular terminal, the digital speech samples must be time multiplexed into the correct channels on the transmission links between switching elements used to connect the terminals. Time slot interchange is provided by each switching element, since the channels used to interconnect the terminals may vary.

Time slot interchange, i.e., the transposition of data on one channel to another channel is well known. As will be seen, a unique multiport switching mechanism, which may comprise a 16-port switching element usable as a thirty-two channel time switch and a sixteen port space switch in typically less than a single frame time for all inputs thereto, is provided. The speech samples may comprise up to 14-bits of the 16-bit channel word with the two remaining bits used as protocol bits (to identify the data type in the other 14-bits of the channel word). Thus the 16-port switching element can be used to switch, for example, 14-bit linear PCM samples, 13-bit linear PCM samples; 8-bit companded PCM samples; 8-bit data bytes, etc.

Two groups of processors are included within each terminal subunit, such as subunit 18, and the first group of processors, e.g. A0, A1, . . . A7, are each dedicated to a separate group of terminals, called a terminal cluster, and perform a specific group of processing functions, e.g. path set-up through the group switch 10 and the provision of an interface to the terminals within the cluster. High traffic clusters, such as trunk lines may include up to thirty terminals whereas low traffic clusters, such as subscriber lines may contain up to sixty terminals. Each terminal subunit may interface with up to four high traffic clusters; hence it contains four A-type processors, whereas a low traffic subunit may interface with eight low traffic clusters and thus has eight A-type processors. Each A-processor may include for example, an Intel Corp. Model 8085 microprocessor interface and associated RAM and ROM memory.

Thus, each terminal unit may contain up to 1920 low traffic terminals (for subscriber lines) or 480 high traffic trunk terminals. Each terminal cluster, such as cluster 36 in subunit 18 includes one A-processor and its associated cluster terminal interface. This interface is coupled by a pair of bidirectional links 38 and 40 respectively to each of two access switches 42 and 44 within terminal subunit 18. The access switching elements, such as elements 42 and 44 of subunit 18 are of the same switching element configuration as are the elements of the group switch 10. Elements 42 and 44 each provide access for subunit 18 to one of a pair of a second group of processors, such as processors B₀ and B₁ in terminal subunit 18. Other pairs of B-type processors are included within subunits 20, 22 and 24, but for purpose of description, only the B-processors of subunit 18 are illustrated.

These second processors, the B-processors, are dedicated to a second group of processing functions, such as call control (the processing of call related data, such as signalling analysis, translations, etc.) for the terminals interfaced by terminal subunit 18

and may also be implemented by Intel Corp. microprocessor Model No. 8085 or its equivalent. A security pair of processors is constituted by the inclusion of identical processing functions in B-processors 46 and 48 and the access switches 42 and 44 for terminal subunit 18, therefore allowing each terminal cluster such as A₀ to select either half of the security pair, i.e., either B-processor 46 via access switch 42 or B-processor 48 via access switch 44 in the event of a failure of one half of the security pair, thereby providing an alternate path.

Figure 2 shows the group switching matrix 10 having four independent planes of switching capability, plane 0 at 100, plane 1 at 102, plane 2 at 104 and plane 3 at 106 as shown. Two or more planes are provided to meet the traffic and service integrity requirements of the particular system. In preferred embodiments, two, three or four planes of switching may be provided, which will service 120,000 or more terminals, i.e., subscriber lines or trunks each having its own line circuit.

Each switching plane may contain up to three stages of switching elements in a preferred architecture. Access switching which selects a particular plane for a connection may be located within the individual terminal unit 12, rather than in the group switch 10. The particular plane of switching elements is selected for a connection by the access switching stage in the terminal unit. Thus, access switching element 42 in subunit 18 can select, for example, plane 0, 100 via link 26 and plane 3, 106 via link 30.

Group switch 10 is modularly expandable either by increasing the number of planes to increase data traffic handling performance, or by increasing the number of stages of switching elements or the number of switching elements per stage to increase the number of terminals served by the group switch. The number of stages per plane of the group switch 10 for typical application requirements is modularly expandable as follows:

STAGE	LINKS PER PLANE	LOCAL APPLICATION		TANDEM APPLICATION
		LINES	TERMINALS	TRUNKS
1 ONLY	8	1,000	1,120	240
1 and 2	64	10,000	11,500	3,500
1, 2 and 3	1,024	>100,000	>120,000	>60,000

Referring now to Figure 3, a fundamental switching element as used in the present system from which all switching stages are configured may be a multiport single-sided switch 300 described as a 16-port switching element. Note that the number of ports could be greater or less than sixteen, which is an example only. A single-sided switch may be defined as a switching element having a plurality of ports of bidirectional transmission capability in which data received at any port may be switched to and transmitted by any port (either the same or other port of the switching element). Operationally, all data transfer from port to port within element 300

occurs via a bit-parallel bus 302, which enables space switching which may be defined as the provision of a transmission path between any two ports within the switching element.

Each port 0 to 15 of switching element 300 includes its own receive control logic Rx304 and its own transmit control logic Tx306 illustrated by way of example, for port number 7. Data is transferred to and from any port such as port 7 from switching elements of like configuration with which the element 300 is linked in bit-serial format via the receive control input line 308 and transmit control output line 310, respectively, at the 4.096 Mb/s system clock

rate, with 512 serial bits constituting a frame, subdivided into thirty-two channels of 16-bits each.

Data transmitted serially from the sixteen ports is both rate and phase synchronous, *i.e.*, the transmit control logic 306 and the equivalent transmit control logic for the other 15 ports of the switching element 300 all transmit at the same 4.096 Mb/s clock rate, and at any instant are transmitting the same bit position of a frame. On the other hand, reception of bit serial data at the receive control logic 304 of port 7 and at all other ports of the switching element 300 is rate synchronous only, *i.e.*, there is no necessary relationship with respect to which bit in a frame that any two ports may be receiving at any instant. Thus reception is phase asynchronous. Receive control logic 304 and transmit control logic 306 each include a control logic portion and a random access memory, described below with reference to Figure 9.

Figure 4 shows one plane 0, 100, of group switch 10. As described with reference to Figure 3, the switching elements such as 108, 110, 112, from which the group switch plane is constructed are 16-port single-sided switching elements 300. It is only by definition *i.e.*, position in the switching network, that switch ports are designated as inlets or outlets. In the three stage group switch plane 100, we have ports 0 to 7 of switching elements 108 and 110 in stages 1 and 2 designated as inlets and ports 8 to 15 as outlets, thus appearing as two-sided, wherein in stage 3, all switching elements such as switching elements 112 are single-sided, *i.e.*, all ports are designed as inlets.

In general, considering any group switch stage, if at some time additional stages are needed to modularly effect network growth, then the stage is equipped as a two-sided stage with the outlets reserved for growth. However, if at any stage the size of the network allows greater than half the maximum required terminals to be connected, then the stage is equipped as a single-sided stage, to allow continual modular expansion up to the maximum required network size without requiring a re-arrangement of the linking between stages.

The modular expansion of the element 300 to a switching plane 100 is illustrated by Figures 5A to 5D. Figure 5A shows a group switch plane of a group switch 10 for an application of one terminal unit having, for example, about 1000 subscriber lines. Thus port 0 may be coupled to line 26 of terminal subunit 18 while ports 1 to 7 are coupled to other access switches in terminal unit 12. Ports 8 to 15 are reserved for network growth.

Figure 5B is an example of the next stage of growth of the plane 100, for two terminal units. Thus, two first stage switching elements are provided per plane of the group switch with each plane having second stage switching elements, *e.g.* 0, 1, 2 and 3 to interconnect the two first stage switching elements. The outlets on the second stage are reserved for subsequent network growth, and this network (one plane of which is shown) serves about 2000 subscriber lines.

Figure 5C illustrates an example of the growth of a switching plane 100 to accommodate eight terminal units. The stage 1 and stage 2 elements are now

shown as fully interconnected and only the stage 2 outlets are available for further growth. Thus to interconnect additional groups of up to eight terminal units, a third stage of switching per plane must be added, as shown in Figure 5D, which shows sixteen terminal units coupled to the expanded group switch plane. Typically, the switching capability of the network of Figure 5C is about 10,000 lines and that of the network of Figure 5D is about 20,000 lines.

The unconnected ports in Figure 5B, 5C and 5D are available for expansion, and each plane of the network, *e.g.* Figure 5D is expanded by connection of these ports up to, for example, the network of Figure 4, which can switch in excess of 100,000 subscriber lines.

Figure 6 shows a line terminal subunit 18 which includes up to eight terminal clusters 36, each including sixty subscriber lines, a terminal interface and an A-microprocessor, three of which clusters are shown at 36, 37 and 39. The subunit 18 access switches 180 and 181 serve eight terminal clusters, only three of which are shown for simplicity of description. Each interface, such as interface 190, is associated with for example, sixty subscriber lines from sixty line circuits, and with an A-processor 198 dedicated to certain processing functions, such as path set-up through the switching network, or terminal control, for lines coupled to the interface 190. Each terminal interface 190 has one bidirectional link such as link 199 to a port of each of the access switches such as switches 180 and 181. Each access switch such as switch 180, which comprises the 16-port element described with reference to Figure 3, provides switched access either to the planes of the group switch 10, *e.g.*, via outlet ports 8, 10, 12, 14 or to a B-processor 183 via for example an outlet such as outlet port 9, this B-processor performing other processing functions such as call control. Unused outlet ports of the access switch, such as ports 11, 13 and 15, are shown as SPARE and are available for equipping other devices such as alarms, monitors, diagnostics controllers, etc.

Figure 7 shows a trunk terminal subunit such as subunit 18, functionally identical to the line terminal subunit described with reference to Figure 6; however it serves a lesser number of high traffic inputs. To account for the increased traffic intensity of trunk groups compared with line terminals, the trunk terminal subunit has up to four terminal interfaces each associated with, for example, thirty trunk terminals. Thus inlets 4 to 7 on each access switch 180 and 181 are unused in this configuration, and terminal clusters 60 and 61 of four such clusters are shown, each including a terminal interface 62 and 63 respectively and an A-processor and memory 64 and 65 respectively.

The B-processor and associated memory 66 and 67 coupled to access switch 180 and B-processor and associated memory 68 and 69 coupled to access switch 181 are of the same configuration as described with reference to Figure 6, and may for example be Intel Corp. 8085 Model microprocessors.

Referring now to Figure 8, the sixteen port switching element 300 described with reference to Figure 3 will be further described. Each port, such as port 15,

consists of a receive control logic 304, a transmit control logic 306, and input and output unidirectional transmission paths 308 and 310 respectively, and has access to a parallel time division multiplexed bus 302 within switching element 300.

In a preferred arrangement, connections are set up through the element 300 on a unidirectional (simplex) basis. A simplex connection between an input channel of a port (one of 32) to an output channel of any port (one of 512) is established by an inchannel command referred to as a SELECT command. This SELECT command is in the single 16-bit word in the input channel requesting the connection. A number of different types of connections are possible through a switching element and these are differentiated by information in the SELECT command. Typical select commands are "any port, any channel", a command received by the receive control logic of the port, and initiates a connection to any free channel in any outlet of any port. "Port N, Any channel", is another SELECT command which initiates a connection to any free channel in a particular port N, e.g., port 8. "Port N, Channel M", is another SELECT command which initiates a connection to a specified channel M such as Channel 5 in a specified port N, such as port 8. Other specialised SELECT commands such as "connect to one of any odd (or even) numbered ports" and specialised channel 16 commands and maintenance commands in channel 0 are within the capacity of the switch module (one port thereof being comprised of one module), as described in greater detail with reference to Figure 9.

The receive control logic 304 for each port synchronises to the incoming data from other switching elements. The channel number (0-31) of the incoming channel is used to fetch destination port and channel addresses from port and channel address storage RAM's. During the multiplexed module access to bus 302 in the channel the receive logic 308 sends the received channel word along with its destination port and channel addresses to the TDM bus 302 of switching element 300. During every bus cycle (the time during which data is transferred from the receive control logic 308 to the transmit control logic 306), every transmit logic at every port looks for its port address on the TDM bus 302. If the port number on the bus 302 corresponds to the unique address of a particular port, the data (channel words) on the bus 302 is written into the data RAM of the recognising port at an address corresponding to the address read out of the channel RAM to the receive control logic port. This accomplishes a one-word data transfer from a receive control logic through the TDM bus 302 to the transmit control logic of a port.

Referring also to Figure 9, the port transmit and receive control logic for a typical port 300 operates as follows: data at 4.096 Mb/s on line 308 is coupled into input sync circuit 400, which provides bit and word synchronisation to the information on line 308. The output of sync circuit 400 is a 16-bit channel word and its channel number (representing the channel position within the frame), is coupled to a first-in-first-out buffer register stack 402 which synchronises data on line 403 to the bus 302 timing, which is needed since data on line 308 is asynchron-

ous to the bus 302 timing. The FIFO buffer 402 output is a 16-bit channel word and its 5-bit channel number. Information contained within the 16-bit channel word indicates the nature of the information in that word. This information is contained within protocol bits of the channel word and together with information in the receive control RAM 404 specifies the action to be taken by the receive control circuit 406 for this channel in this frame.

Five types of actions, SPATA, SELECT, INTERROGATE, ESCAPE or IDLE/CLEAR are possible. If the protocol is SPATA (speech and data words), the channel word is sent to bus 302 unmodified and the channel address fetches destination port and channel addresses from the channel RAM 408 and the port RAM 410 and couples them to the bus 302 during the port's receive logic bus access time slot. If a select command is "any port, any channel" the first free port select circuit 412 selects a transmit logic with an idle channel to do a "first free channel select". During the receive logic TDM bus 302 access time a "first free channel select" is done into the selected port's selected transmit logic which returns a "free channel" number from its first free channel search circuit 414. A NACK receive circuit 416 examines the contents of channel-16 for path set-up failure indications from succeeding stages of the switching network that have been set up through the transmit logic 306 of the module. NACK search logic 418 examines the receive control RAM 404 for channels that are NACK'ed (not acknowledged) and causes the channel numbers of NACK'ed channels to be outpulsed from the transmit logic 306 in channel-16.

Transmit logic 306 examines the state of the port address lines of the bus 302 with its module identification code at decode port logic. If the correct port address is decoded at decoder 420, and the select line of bus 302 is inactive, then the contents of the SPATA lines of the bus 302 will be written into data RAM 422 at an address given by the state of the channel address lines of the bus 302.

If the select line of bus 302 is active and a first free channel search is requested by receive control such as 406 (for any channel selection) then no data RAM 422 write operation occurs, but a free channel number is returned to the requesting receive logic such as 304 from the first free channel search circuit 414.

The data RAM 422 is a time slot interchanger and is read from sequentially under the control of a counter in the transmit/bus timing circuit 428. Words read out of data RAM 422 are loaded into a parallel-input-serial-output register 430 which couples the serial bit stream to transmit line 310 at 4.096 Mb/s. The word loaded into output register 430 may be modified in channel 0 or 16. In channel 0, alarms on line 432 are inserted (for error checking) and the NACK channel information is inserted in channel-16, when required, by logic 434. The transmit control RAM 426 contains the status of each outgoing channel. The transmit control logic 424 co-ordinates the read and write operations to the data RAM 422 and transmit control RAM 426, free channel search 414, and output register 430 loading.

The establishment of connections through the network between terminals will now be described.

As aforementioned, the 16-port switching elements provide both time and space switching functions for all transmission paths. Information arriving on the incoming path at any port for any channel can be transferred by the 16-port switching element to the outgoing path of any port, giving space switching, and any channel on that path, giving time switching. All speech and data (SPATA) transmission through the network is the result of individual ports in the multi-port switching elements implementing transformation of input channel (one out of 512) to output channel (one out of 512), as predetermined by path set-up procedures, with thirty-two channel words per frame on any give transmission path. Figure 10 illustrates one example of channel word format applicable to all of channels 1 to 15 and 17 to 31, which channels are SPATA channels. The channel word formats for channel 0 (maintenance and synchronisation) and channel 16 (special purpose control, NACK, etc.) are shown in Figure 11.

The SPATA channels can be used for both digital speech and interprocessor data transmission. When speech is transmitted, 14-bits per channel word are available for the encoded PCM sample and 2-bits are available for network protocol selection. When used for path set up control, 13 bits/channel word are available for the data and 3-bits for protocol selection. The channel word format enables switching throughout the network, which involves connection through a plurality of the 16-port switching elements. These connections are unidirectional. For bidirectional connection, two unidirectional connections are required.

Figure 10 shows examples of channel word formats for all channels except channels 0 and 16, and Figure 11 shows examples of word formats for channel 16. Figures 10(a) to 10(d) illustrate data field formats for SELECT, INTERROGATE, ESCAPE, SPATA and IDLE/CLEAR respectively. Figures 11(a) to 11(d) illustrate SELECT, ESCAPE, HOLD and IDLE/CLEAR for channel 16. The channel words in channel 0 also contain the frame synchronisation bit pattern (6-bits) between adjoining 16-port switching elements.

SELECT command sets up a connection through a switching element.

INTERROGATE command is used after the path is set up to determine which port was chosen in the switching element for that path.

ESCAPE command is used once a path has been set up to transfer information between two terminal clusters and to distinguish such information from digitised speech samples.

SPATA format is used to transfer speech or data information between any two terminals.

IDLE/CLEAR command format indicates that the channel is clear.

For channel 16, the SELECT, ESCAPE and IDLE/CLEAR commands are similar to those described with reference to Figure 10, except that as there is no SPATA mode, the INTERROGATE command is not needed, and since channel 16 carries the NACK channel, the types of SELECTS are restricted.

The HOLD command maintains a channel 16 connection once it has been set up by SELECT commands. Channel 0 is reserved for maintenance and diagnostics of the network.

Figure 12 illustrates a terminal subunit 18, which contains its portion of the access switching stage, access switches 42 and 44, as described with reference to Figure 1, and the group switch 10, which contains three stages of switching. Individual planes in the group switch and individual switching elements within each stage are not shown, for simplicity of description.

A connection through the switching network is set up from one terminal interface, such as 690 to another terminal interface such as 190, or from a B-processor such as 183 to another processor such as A-processor 198 associated with terminal interface 190 by a series of SELECT commands, i.e., channel word formats which are inserted into the PCM framed bit stream between the originating terminal interface (or processor) and the access switch in successive frames in the channel allocated to the connection. One SELECT command is required for each path connection through each stage of switching.

A connection through the switching network is made by a sequential series of connections through individual switching stages. The connection proceeds as an orderly progression from lower numbered stages to higher numbered stages by "inlet to outlet" connections across switching elements until a predetermined "reflection stage" is reached. Reflection is the connection between inlet ports in the switching element and enables connection to be made without penetrating the switching network more than is required to complete the desired connection. For a detailed description of the concept of reflection in a switching network, reference is made to our copending application No. 1786/78.

Across the switching elements in the reflection stage an "inlet to inlet" connection is made, followed by an orderly progression from higher numbered stages to lower numbered stages by "outlet to inlet" connections across switching elements.

The predetermination of the "reflection stage" is made with respect to a unique network address of the required terminal interface such as 190. These rules are generalised as follows:

(i) If the terminating terminal interface is in the same terminal subunit, reflection is made to occur at the access switch.

(ii) If the terminating terminal interface is in the same terminal unit, reflection is made to occur at stage 1.

(iii) If the terminating terminal interface is in the same group of terminal units, reflection is made to occur at stage 2.

(iv) For all other cases, reflection is made to occur at stage 3.

We refer again to Figures 1 and 4, which illustrate a unique feature of the network architecture, in which a terminal unit, such as unit 12 with 8 bidirectional transmission links to each group switch plane such as the illustrated plane 0 of Figure 4, has these links terminating on one switching element in each

plane. This element can be seen to have a unique address when viewed from the centre (i.e. third stage) of the group switch 10. Thus, for example, see Figure 4, the switching element 108 when viewed from any switching element in the third stage is accessible via inlet 0 from stage 3 followed by inlet 0 from stage 2. This constructs the address of the terminal unit, i.e., it has the address TU (0,0). Furthermore, a terminal subunit is uniquely addressed within a terminal unit with respect to the second stage inlets, i.e., see Figure 1, terminal subunit 18 can be seen as TSU () of TU (0,0) as it is uniquely addressed from inlets 0 and 4 of first stage switch (0,0). Similarly, each terminal interface in each terminal cluster is uniquely addressed via its inlet address on the access switch. Thus, the address of a terminal interface, such as interface 190 of Figure 12 as seen by any other terminal interface such as 690 in terminal unit 16, for example, is independent of which switching element in stage three is the "reflection point".

This allows the path set up controlling A-processor, 698, to launch the following sequence of SELECT commands into the network in order to set up a connection to the terminal interface 190 whose network address is, for example, (a, b, c, d).

(i) FRAME 1. SELECT, ANY EVEN PORT, ANY CHANNEL: This sets a SPATA connection through the access switch to a group switch plane.

(ii) FRAME 2. SELECT, ANY PORT, ANY CHANNEL: This sets a connection through stage 1 of the chosen plane.

(iii) FRAME 3. SELECT, ANY PORT, ANY CHANNEL: This sets a connection through stage 2 of the chosen plane.

(iv) FRAME 4. SELECT PORT (a) ANY CHANNEL: This reflects the connection through stage 3 to stage 2.

(v) FRAME 5. SELECT PORT (b) ANY CHANNEL: This sets a connection back through stage 2.

(vi) FRAME 6. SELECT PORT (c) ANY CHANNEL: This sets a connection back through stage 1.

(vii) FRAME 7. SELECT PORT (d) ANY CHANNEL: This sets a connection back through the access switch to terminal interface (a, b, c, d).

This network permits switching forward to any reflection point in the stage determined as the reflection stage and then back through the network with a constant address independent of the reflection switching element in that stage.

The sequence of SELECT's can be used by any terminal interface to set up a connection to TI (a, b, c, d) and the "first free channel" selection mechanism described above ensures minimum transmission delay on the selected path. Where reflection is possible at an earlier switching stage as decided from the above rules given, a subset of the above sequence can be used. Thus, see Figure 12, the B-processor, 183, which is in the same terminal subunit 18 as terminal interface 190, need launch only the subset of the above sequence formed by FRAME 1. SELECT PORT (d) ANY CHANNEL.

The processing functions performed by the A and B processors are dependent upon the particular computer programs used; however, examples of

processing functions are: *terminal control*, which provides the features for each class of service for subscriber or trunk lines; *signalling control*, which generates signals to call terminals under control of the terminal control processing, and decodes and interprets sequences of signals and digits which are coupled as telephone events to the terminal control processor for action; *switching control*, which sets up, maintains, and tears down paths through the network as directed by the terminal control and signalling control functions; *data base control*, which performs all operation on the physical data base and allows all other processes to operate independently of a particular organisation the data base; and *hardware control*, which comprehends processes for the control of the hardware actually interfacing subscriber lines or trunks, and for the terminal units and switching elements. An example of the distribution of processing functions is the allocation of hardware control for up to 60 line terminals or 30 trunk terminals at each A microprocessor, with the other functions performed by the B microprocessor for some other number of terminals. Of course, switch control could alternatively be performed by the A-microprocessor.

Referring now to Figure 13, timing diagrams illustrative of the operation of a switching element 300 are shown.

Figure 13(a) shows the current bus 302 time slot number and channel number, with 16 time slots constituting one channel; with the time slot numbers being written in hexadecimal notation, and with channels 0, 1 and eight time slots of channel two illustrated.

Figure 13(b) is the 4.096 Mb/s bus clock.

Figure 13(c) illustrates the frame synchronisation which is a port synchronisation command, which occurs on bus 302 during channel 31, time slot E.

Figures 13(d) to 13(h) illustrate for ports 0, 1, 2, 14 and 15 of switching element 300 the time envelopes of the bus 302 transfer actions of their respective ports. Ports 3 to 13 are not shown, but are operationally identical. Each of the bus transfer envelopes 501, 502, 503, 504 and 505 for ports 0, 1, 2, 14 and 15 respectively are time multiplexed. Each envelope includes four time slots P, D, W, R, during which, specific actions occur on specific lines of the TDM bus 302 during specific times such that only one port is transmitting information on any one line of TDM bus 302 at any instant in time. The precise time of starting of any transfer envelope is determined by a unique port address code.

Referring now to Figure 14, 14(a) shows the system clock illustrated by Figure 13(b). Figures 14(b) to 14(e) are expansions of the time slot P, D, W and R of typical bus transfer envelopes 501, 502, 503, 504 or 505.

Bus 302 has thirty-six unidirectional lines for performing bus intercommunication functions between all sixteen ports, as illustrated by Figure 15. The signals that the receive logic 304 of the module presents to the bus 302 are DATA (16-bits each on a separate line) DESTINATION PORT ADDRESS (4-bits each on a separate line). DESTINATION CHANNEL ADDRESS (5-bits each on a separate line, DATA

VALID (1-bit), SELECT (1-bit), and MODE (1-bit). The signals received from the bus 302 are SELECTED CHANNEL (5-bits each on a separate line), ACKNOWLEDGE (1-bit), and MODULE BUSY (1-bit).

5 Depending on the FIFO DATA word from the FIFO buffer 402 and the contents of the RECEIVE CONTROL RAM 404 addressed by the channel number output of FIFO 402 various signals are presented to the bus 302 and accepted from it, and various words
10 written into the PORT, CHANNEL and RECEIVE CONTROL RAMS of the receive logic 304 for the enabled port. The SET WRITE ACTIVITY LINE of bus 302 is a special function line to override the occurrence of a predetermined function.

15 During time slot P shown on Figure 14(b) as (1), the currently enabled receive logic 304 transmit to bus 302 the destination transmit logic port number and also puts appropriate signals on bus lines DATA VALID, SELECT, MODE and MODULE BUSY. On the rising edge of the clock shown on Figure 14(a) as (2),
20 all transmit logics 306 of all sixteen ports put the state of the above mentioned bus lines into registers associated with decode port number circuit 420 and transmit control 424. During time slot D, shown on Figure 14(c) as (3), the receive logic of the enabled port puts information on the DATA LINES and DESTINATION CHANNEL ADDRESS LINES. On the next rising edge of the clock, shown on Figure 14(a) as (4), this information is transferred into buffer registers
25 associated with the data RAM 422. During time slot W, shown on Figure 14 (d) as (5), if the port number represented by the 4-bits on the DESTINATION PORT ADDRESS LINES which occurred during time slot P matches the port identification code of a particular port, which code is unique for each port, an operation occurs at the port's transmit logic. The operation may be a write into the data RAM 422 of that port or a response to a SELECT command. Also during time slot W, a proper value for the selected
30 channel number is coupled from first free channel search circuit 414 onto the SELECTED CHANNEL NUMBER LINES, if appropriate, and a value (either logic 1 or 0) for an acknowledge signal is evaluated. A NACK is simply the lack of an acknowledgement signal. During time slot R, shown on Figure 14(e), as (6), the destination port transmit logic places a response on the SELECTED CHANNEL number and acknowledges lines. The enabled receive logic transfers the state of these lines into a register associated
35 with receive control 406 on the next CLOCK leading edge shown as (7) by Figure 14(a), and some later time, shown as (8) by Figure 14(e), updates its own port channel and receive control RAMs 410, 408 and 406 respectively.

40 NACK channel numbers received by a NACK receiver 416 at the receive logic of a particular port will cause a reject bit to be set in the transmit logic of the same port at the address specified by the received NACK channel number, i.e., a NACK in
45 channel 16 may be decoded as "NACK channel 7" for example. The next time the receive logic which has set-up a path into channel 7 attempts to write into channel 7, it will get no acknowledge signal and will designate the channel with the path into channel
50 7 as being NACK'ed. The NACK search circuit 418

will then output the number of the NACK'ed channel from its transmit logic, in channel 16.

55 Delay through the network is automatically minimised by the use of the first free channel search technique. The first free channel search circuit 414 continuously looks at the "busy bit" of the transmit control RAM 424 for idle channels with the lowest channel number higher than the current output channel number coupled to the serial data on PCM line 310.

60 While the present invention has been described in connection with a preferred embodiment thereof, it is to be understood that additional embodiments, modifications, and applications which will become obvious to those skilled in the art are included within the spirit and scope of the invention as set forth by the claims appended hereto.

CLAIMS

1. A distributed control digital communication system including a number of terminal units for
65 interfacing a number of PCM communication terminals each associated with one of a number of subscribers' lines to one or more common communication paths, wherein:

(a) each of said PCM terminals is adapted to convey digitized speech in frames with each said frame containing a number of channels usable for the conveyance of said digitized speech;

(b) in-channel path selection control signals derived by respective ones of a group of processors each of which provides processing functions for a group of said PCM terminals are multiplexed with the digitized speech so that the same physical paths are used to convey digitized speech and said in-channel path selection control signals;

(c) a digital switching network is coupled to a number of paths such as said common communication paths for bit asynchronously interconnecting the PCM terminals through paths set up through the switching network in response to said path selection control signals; and

(d) means is provided at each of said terminal units for selectively multiplexing said digitized speech and said in-channel path selection control signals on the appropriate one of the common communication paths such that the path selection control signals precede the digitized speech in channels designated by said path selection control signals on the said common communication path.

2. A system in accordance with claim 1, wherein said switching matrix is a multistage group switch.

3. A system in accordance with claim 1 or 2, wherein some at least of said PCM terminals are each associated with a telephone trunk line.

4. A system in accordance with claim 1 and further including:

(a) a second group of processors, each of which provides other processing functions for a plurality of said groups of PCM terminals, and

(b) a means for coupling interprocessor control signals from one processor of a group of processors to any other processor through said paths established through said switching network by said path selection control signals to provide communication therebetween.

5. A system in accordance with claim 4, wherein



VALID (1-bit), SELECT (1-bit), and MODE (1-bit). The signals received from the bus 302 are SELECTED CHANNEL (5-bits each on a separate line), ACKNOWLEDGE (1-bit), and MODULE BUSY (1-bit).

- 5 Depending on the FIFO DATA word from the FIFO buffer 402 and the contents of the RECEIVE CONTROL RAM 404 addressed by the channel number output of FIFO 402 various signals are presented to the bus 302 and accepted from it, and various words
10 written into the PORT, CHANNEL and RECEIVE CONTROL RAMS of the receive logic 304 for the enabled port. The SET WRITE ACTIVITY LINE of bus 302 is a special function line to override the occurrence of a predetermined function.

- 15 During time slot P shown on Figure 14(b) as (1), the currently enabled receive logic 304 transmit to bus 302 the destination transmit logic port number and also puts appropriate signals on bus lines DATA VALID, SELECT, MODE and MODULE BUSY. On the
20 rising edge of the clock shown on Figure 14(a) as (2), all transmit logics 306 of all sixteen ports put the state of the above mentioned bus lines into registers associated with decode port number circuit 420 and transmit control 424. During time slot D, shown on
25 Figure 14(c) as (3), the receive logic of the enabled port puts information on the DATA LINES and DESTINATION CHANNEL ADDRESS LINES. On the next rising edge of the clock, shown on Figure 14(a) as (4), this information is transferred into buffer registers associated with the data RAM 422. During time slot
30 W, shown on Figure 14 (d) as (5), if the port number represented by the 4-bits on the DESTINATION PORT ADDRESS LINES which occurred during time slot P matches the port identification code of a particular port, which code is unique for each port, an
35 operation occurs at the port's transmit logic. The operation may be a write into the data RAM 422 of that port or a response to a SELECT command. Also during time slot W, a proper value for the selected channel number is coupled from first free channel
40 search circuit 414 onto the SELECTED CHANNEL NUMBER LINES, if appropriate, and a value (either logic 1 or 0) for an acknowledge signal is evaluated. A NACK is simply the lack of an acknowledgement
45 signal. During time slot R, shown on Figure 14(e), as (6), the destination port transmit logic places a response on the SELECTED CHANNEL number and acknowledges lines. The enabled receive logic transfers the state of these lines into a register associated
50 with receive control 406 on the next CLOCK leading edge shown as (7) by Figure 14(a), and some later time, shown as (8) by Figure 14(e), updates its own port channel and receive control RAMs 410, 408 and 406 respectively.

- 55 NACK channel numbers received by a NACK receiver 416 at the receive logic of a particular port will cause a reject bit to be set in the transmit logic of the same port at the address specified by the received NACK channel number, i.e., a NACK in
60 channel 16 may be decoded as "NACK channel 7" for example. The next time the receive logic which has set-up a path into channel 7 attempts to write into channel 7, it will get no acknowledge signal and will designate the channel with the path into channel
65 7 as being NACK'ed. The NACK search circuit 418

will then output the number of the NACK'ed channel from its transmit logic, in channel 16.

- Delay through the network is automatically minimised by the use of the first free channel search technique. The first free channel search circuit 414 continuously looks at the "busy bit" of the transmit control RAM 424 for idle channels with the lowest channel number higher than the current output channel number coupled to the serial data on PCM line 310.

- 75 While the present invention has been described in connection with a preferred embodiment thereof, it is to be understood that additional embodiments, modifications, and applications which will become obvious to those skilled in the art are included within the spirit and scope of the invention as set forth by the claims appended hereto.

CLAIMS

1. A distributed control digital communication system including a number of terminal units for
85 interfacing a number of PCM communication terminals each associated with one of a number of subscribers' lines to one or more common communication paths, wherein:

- (a) each of said PCM terminals is adapted to convey digitized speech in frames with each said frame containing a number of channels usable for the conveyance of said digitized speech;

- (b) in-channel path selection control signals derived by respective ones of a group of processors each of which provides processing functions for a
95 group of said PCM terminals are multiplexed with the digitized speech so that the same physical paths are used to convey digitized speech and said in-channel path selection control signals;

- (c) a digital switching network is coupled to a number of paths such as said common communication paths for bit asynchronously interconnecting the PCM terminals through paths set up through the switching network in response to said path selection
105 control signals- and

- (d) means is provided at each of said terminal units for selectively multiplexing said digitized speech and said in-channel path selection control signals on the appropriate one of the common
110 communication paths such that the path selection control signals precede the digitized speech in channels designated by said path selection control signals on the said common communication path.

2. A system in accordance with claim 1, wherein
115 said switching matrix is a multistage group switch.

3. A system in accordance with claim 1 or 2, wherein some at least of said PCM terminals are each associated with a telephone trunk line.

4. A system in accordance with claim 1 and
120 further including:

- (a) a second group of processors, each of which provides other processing functions for a plurality of said groups of PCM terminals, and

- (b) a means for coupling interprocessor control
125 signals from one processor of a group of processors to any other processor through said paths established through said switching network by said path selection control signals to provide communication therebetween.

- 130 5. A system in accordance with claim 4, wherein



at least one of the processing functions provided by each of the processors of said second group of processors includes call translation.

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd.,
Berwick-upon-Tweed, 1982.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.