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CLAIMS

What is claimed is:

- 5 1. A method of forming a semiconductor device, comprising:
forming a memory cell material in a peripheral region and in an array region of a
semiconductor device structure;
removing the memory cell material from the peripheral region; and
after removing the memory cell material from the peripheral region, selectively
10 removing portions of the memory cell material from the array region to define
individual memory cells in the array region.
2. The method of claim 1, wherein forming a memory cell material
comprises forming a phase change memory cell material.
- 15 3. The method of claim 1, further comprising:
after removing the memory cell material from the peripheral region, forming a
dielectric filler material in the peripheral region; and
planarizing the dielectric filler material in the peripheral region.
- 20 4. The method of claim 3, further comprising forming contact holes in the
peripheral region through the dielectric filler material.
5. The method of claim 1, wherein selectively removing portions of the
25 memory cell material from the array region to define individual memory cells
comprises:
forming first array trenches extending in a first direction; and
forming second array trenches extending in a second direction orthogonal to the first
direction.

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6. The method of claim 5, further comprising forming peripheral contacts in the peripheral region after forming the first array trenches and prior to forming the second array trenches.

5 7. The method of claim 5, further comprising filling the first array trenches and the second array trenches with at least one of a nitride material and an oxide material.

8. The method of any one of claim 1 through claim 7, further comprising:
10 forming a conductive pad material coupled to peripheral conductive contacts in the peripheral region and coupled to the memory cell material in the array region;
selectively removing portions of the conductive pad material to define conductive pads in the peripheral region and to define conductive lines in the array
15 region;
forming a spacer material over the conductive pads and the conductive lines; and
planarizing the semiconductor device structure using at least one of the conductive pad material and conductive lines, and the spacer material as a planarization stop material.

20 9. The method device of claim 8, wherein forming a conductive pad material coupled to the memory cell material comprises coupling the conductive pad material to the memory cell material through at least one of a cell contact material and a cell adhesion material.

25 10. The method of claim 8, further comprising forming a filler material over the spacer material, wherein planarizing the semiconductor device structure comprises removing portions of the filler material over the conductive pads and conductive lines.

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11. The method of claim 8, wherein selectively removing portions of the conductive pad material comprises forming peripheral trenches, further comprising filling the peripheral trenches with at least one of the spacer material and a filler material.

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12. The method of claim 11, wherein filling the peripheral trenches with at least one of the spacer material and a filler material comprises filling the peripheral trenches with at least one of a nitride spacer material and an oxide filler material.

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13. The method of claim 8, wherein selectively removing portions of the conductive pad material to define conductive pads in the peripheral region comprises forming the conductive pads to each have a relatively larger upper surface area than an upper surface area of a respective one of the peripheral conductive contacts.

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14. The method of claim 8, further comprising forming upper conductive contacts respectively coupled to the conductive pads and to the conductive lines.

15. A semiconductor device structure, comprising:
a peripheral region, comprising:

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peripheral conductive contacts coupled to at least one transistor;
conductive pads comprising a conductive material, the conductive pads coupled to respective peripheral conductive contacts, the conductive pads each having an upper surface area greater than an upper surface area of a peripheral conductive contact coupled thereto; and

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peripheral trenches separating the conductive pads; and
an array region, comprising:

an array of memory cells; and
conductive lines each coupled to memory cells of the array of memory cells, the conductive lines comprising the same conductive material as the conductive pads in the peripheral region.

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16. The semiconductor device structure of claim 15, further comprising at least one of a dielectric spacer material and a dielectric filler material within the peripheral trenches.

5 17. The semiconductor device structure of claim 15, further comprising upper peripheral conductive contacts respectively coupled to the conductive pads and upper array conductive contacts coupled to the conductive lines.

10 18. The semiconductor device structure of claim 17, wherein the upper peripheral conductive contacts and the upper array conductive contacts comprise a copper material and wherein the conductive pads and the conductive lines comprise a tungsten material.

15 19. The semiconductor device structure of any one of claim 15 through claim 18, wherein the array of memory cells comprises an array of phase change memory cells comprising phase change memory cell materials electrically isolated from one another in a first direction by first trenches and in a second direction by second trenches.

20 20. The phase change memory device of claim 17, wherein the peripheral trenches are filled with a nitride material and an oxide material.

CLAIMS

What is claimed is:

- 5 1. A semiconductor device structure, comprising:
a peripheral region, comprising:
 peripheral conductive contacts coupled to at least one transistor;
 conductive pads comprising a conductive material, the conductive pads coupled
 to respective peripheral conductive contacts, the conductive pads each
10 having an upper surface area greater than an upper surface area of a
 peripheral conductive contact coupled thereto; and
 peripheral trenches separating the conductive pads; and
an array region, comprising:
 an array of memory cells; and
15 conductive lines each coupled to memory cells of the array of memory cells,
 the conductive lines comprising the same conductive material as the
 conductive pads in the peripheral region.
- 20 2. The semiconductor device structure of claim 1, further comprising at
least one of a dielectric spacer material or a dielectric filler material within the
peripheral trenches.
- 25 3. The semiconductor device structure of claim 1, further comprising
upper peripheral conductive contacts respectively coupled to the conductive pads and
upper array conductive contacts coupled to the conductive lines.
- 30 4. The semiconductor device structure of claim 3, wherein the upper
peripheral conductive contacts and the upper array conductive contacts comprise a
copper material and wherein the conductive pads and the conductive lines comprise a
tungsten material.

5. The semiconductor device structure of claim 2, wherein the dielectric spacer material comprises a nitride material and the dielectric filler material comprises an oxide material.

5 6. The semiconductor device structure of claim 2, further comprising the dielectric spacer material within array trenches separating the conductive lines in the array region.

7. The semiconductor device structure of claim 6, further comprising the
10 dielectric spacer material over upper surfaces of the conductive lines.

8. The semiconductor device structure of claim 1, wherein the conductive material of the conductive lines and of the conductive pads is selected from the group consisting of copper, copper silicide, tungsten, tungsten nitride, titanium, and titanium
15 nitride.

9. The semiconductor device structure of claim 1, further comprising a cell adhesion material coupling the conductive lines to the memory cells of the array of memory cells.

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10. The semiconductor device structure of claim 1, wherein upper surfaces of the conductive pads are substantially coplanar with upper surfaces of the conductive lines.

25 11. The semiconductor device structure of claim 1, wherein the array of memory cells comprises an array of phase change memory cells.

12. A phase change memory device, comprising:
phase change memory cells comprising phase change memory cell materials
30 electrically isolated from one another in a first direction by first trenches and in a second direction by second trenches;

conductive lines coupled to phase change memory cells aligned in the second direction; and

peripheral conductive pads coupled to peripheral conductive contacts, the peripheral conductive pads having upper surfaces that are coplanar with upper surfaces
5 of the conductive lines.

13. The phase change memory device of claim 12, wherein each of the peripheral conductive pads has an upper surface area that is greater than an upper surface area of the peripheral conductive contact to which the peripheral conductive
10 pad is coupled.

14. The phase change memory device of claim 12, further comprising peripheral trenches separating the peripheral conductive pads from each other.

15. The phase change memory device of claim 14, wherein the peripheral trenches are filled with a nitride material and an oxide material.

16. The phase change memory device of claim 14, wherein the peripheral trenches are filled with a dielectric spacer material and a dielectric filler material.

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17. The phase change memory device of claim 16, wherein the dielectric spacer material is formed along surfaces defining the peripheral trenches and over upper surfaces of the peripheral conductive pads.

25 18. The phase change memory device of claim 12, wherein the first direction and the second direction are at least substantially orthogonal to each other.

19. The phase change memory device of claim 12, wherein the conductive lines have a pitch that is smaller than a pitch of the peripheral conductive pads.

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20. The phase change memory device of claim 12, wherein the conductive lines and the peripheral conductive pads each comprise the same conductive material.