with regard to synchronization between the rectifier circuit and the inverter, Fig. 10 is only shown in Non-Patent Document 1, and Fig. 12 is only shown in Patent Document 2.

[0005] Moreover, Non-Patent Document 1 describes that a direct power converter with a DC link is controlled by using a DSP (Digital Signal Processor) and a CPLD (Complex Programmable Logic Device). However, details of logic adopted in the DSP and the CPLD are not disclosed.

[0006] Meanwhile, as a modulation mode similar to those of Patent Document 1 and Non-Patent Documents 1 and 2, a modified symmetrical triangular wave mode is shown in Patent Document 2. Fig. 3 in Patent Document 2 shows a specific configuration of a modulator. An up/down command of an inverter-side carrier is outputted based on an up/down signal of a carrier on a rectifier side and on an output pulse obtained by a PWM (pulse width modulation) on the rectifier side. However, in Patent Document 2, as apparent from Fig. 4 thereof, the same thing as that in Non-Patent Document 1 is merely shown as a result.

[0007] Note that, in Fig. 8 of Patent Document 3, a mode of modulating by the inverter and the converter using the same carrier is shown.

[0008] Non-Patent Document 3 shows that a modulation is realized by a microcomputer and an FPGA (Field-Programmable Gate Array).

[0009] Note that Patent Document 4 and Non-Patent Documents 4 and 5, which are related to the present application, are listed in addition to the above.

Prior Art Documents

Patent Documents

[0010] Patent Document 1: United States Patent No. 6995992

Patent Document 2: Japanese Patent Application Laid-Open No. 2004-266972

Patent Document 3:Japanese Patent No. 4135026

Patent Document 4:Japanese Patent Application Laid-Open No. 2011-193678

Non-Patent Documents

[0011] Non-Patent Document 1: Wei, L., Lipo, T.A., Chan, H, "Matrix Converter Topologies With Reduced Number of Switches," PESC 2002, June 23-27, 2002, vol. 1, pp 57-63.

Non-Patent Document 2: L.Wei, T.A.Lipo, "Investigation of 9-switch Dual-bridge Matrix Converter Operating under Low Output Power Factor," IEEE IAS2003, vol.1, pp.176-181

Non-Patent Document 3: Fujita, Sakakibara, Matsuno, "Application and Development of the Three Phase Indirect Matrix Converter for Air Conditioners", The papers of Joint Technical Meeting on Semiconductor Power Converter/Vehicle Technology/Home and Consumer Appliances, SPC-12-174/VT-12-025/HCA-12-059, IEE Japan 2012(20), pp.31-36, 2012-12-06

Non-Patent Document 4: Renesas Electronics Application Note: RX62T Group - Usage Example of 12-Bit AD Converter in One Shunt Current Detection Method, R01AN0821JJ0100

Non-Patent Document 5: Renesas Electronics Application Note: RX62T - MTU3 Complementary PWM mode, R01AN0731JT0101

Summary of Invention

Problems to be Solved by the Invention

[0012] As described above, special logic has been required for the modulator of the conventional direct power converter, and it has been necessary to accompany with a logic IC such as a CPLD or an FPGA.

[0013] On the other hand, as a microcomputer suitable for controlling the inverter

using the PWM modulation, there are ones introduced in Non-Patent Documents 4 and 5. Hence, it is desirable to control the direct power conversion device by such a microcomputer without using the logic IC from a viewpoint of hardware reduction.

[0014] In this connection, embodiments of the present invention seek to provide a technology for controlling the direct power converter by the microcomputer without using the logic IC.

Means for Solving the Problems

[0015] A power converter control device according to the present invention is a power converter control device (1) for controlling a power converter (2) including a converter (21) that performs AC-DC conversion and an inverter (22) that receives a DC voltage (Vdc) from the converter and supplies a multi-phase AC current (Iv).

[0016] Then, a first aspect of the present invention includes: a converter control unit (11) that outputs a converter switching signal (Scnv) for determining switching of the converter based on a result of performing comparison between a converter carrier (K1) and a converter threshold value (Ccnv) in each of first periods (P) repeated while having a first period length (Tcnv); and an inverter control unit (12) that outputs an inverter switching signal (Sinv) for determining switching of the inverter based on a result of performing comparison between an inverter carrier (K2) and an inverter threshold value (Dpwm) in each of second periods (Q1, Q2) synchronized with the converter carrier and repeated while having a second period length (Tinv).

[0017] Then, in the first period, first data (Data1) and second data (Data2) are alternately given to the inverter control unit, the first data (Data1) including a first value (Tinv1) indicating a length of time from a start point of time of the first period to a matching point of time (J) as a point of time when the converter carrier takes the

converter threshold value and the inverter threshold value (Dpwm1) corresponding to the second period (Q1) having the first value as the second period length, and the second data (Data2) including a second value (Tinv2) indicating a length of time from the matching point of time to an end point of time of the first period and the inverter threshold value (Dpwm2) corresponding to the second period (Q2) having the second value as the second period length.

[0018] A second aspect of the power converter control device according to the present invention is the first aspect thereof further including: an arithmetic processing unit (10) that performs arithmetic processing for obtaining the first data (Data1) and the second data (Data2) for a pair of the second periods, the arithmetic processing being performed every first period.

[0019] Then, the inverter control unit (12) includes: a buffer register (124a, 124c) which stores the inverter threshold value (Dpwm) and the second period length (Tinv); a compare register (123a, 123c) to which contents stored by the buffer register are transferred at a boundary point of time as a point of time serving as a boundary between the second periods; a timer (121) that generates a count value that is compared with the second period length stored in the compare register and becomes the inverter carrier (K2); and a switching signal generation unit (128) that generates the inverter switching signal (Sinv) on the basis of the result of the comparison between the inverter threshold value stored in the compare register and the inverter carrier.

[0020] Then, the first data (Data1[k+1]) obtained by the arithmetic processing in one of the first periods (P[k]) is stored in the buffer register before the start of another (P[k+1]) of the first periods, the second data (Data2[k+1]) obtained by the arithmetic processing in the one of the first periods is stored in the buffer register on an occasion of the start of the another of the first periods, and the another of the first periods is present immediately

repeats a monotonic increase and a monotonic decrease every first period, and the inverter carrier (K2) repeats a monotonic increase and a monotonic decrease every second period.

[0026] An eighth aspect of the power converter control device according to the present invention is any one of the first to fifth aspects thereof, wherein the converter carrier (K1) exhibits a sawtooth wave having the first period length (Tcnv) as a cycle, and the inverter carrier (K2) repeats a monotonic increase and a monotonic decrease every second period.

[0027] In the first to eighth aspects of the power converter control device according to the present invention, for example, the converter (21) is a current source converter, and commutates at the matching point of time by the converter switching signal (Scnv).

[0028] In the first to eighth aspects of the power converter control device according to the present invention, for example, the converter (21) includes a rectifier circuit and a booster circuit, and it is determined whether or not the booster circuit contributes to the DC voltage (Vdc) on the basis of the converter switching signal (Scnv).

[0029]

Effects of the Invention

[0030] In accordance with the first aspect of the power converter control device according to the present invention, the number of complementary PWM modulators required is saved to be one, for the control for dividing one cycle for controlling the converter into two sections at the point of time when the converter commutates, and for controlling the inverter in the respective sections.

[0031] In accordance with the second aspect of the power converter control device according to the present invention, write into the buffer register follows transfer from the buffer register to the compare register, and accordingly, comparison between the first data and the second data, and the inverter carrier is appropriately performed.

[0032] The third to sixth aspects of the power converter control device according to the present invention contribute to the realization of the second aspect of each thereof.

[0033] In accordance with the seventh to eighth aspects of the power converter control device according to the present invention, responsiveness of the output of the inverter is improved.

[0034] In particular, in accordance with the eighth aspect of the power converter control device according to the present invention, a range of options for selecting the timer to be adopted is widened.

[0035] Objects, features, aspects and advantages of the present invention will be more obvious by the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0036] Fig. 1 is a block diagram illustrating a configuration of a power converter control device according to a first embodiment and a configuration of a power converter to be controlled thereby;

Fig. 2 is a block diagram illustrating a configuration of an inverter control unit in the first embodiment;

Fig. 3 is a block diagram illustrating a configuration of a converter control unit in the first embodiment;

Fig. 4 is a graph showing a relationship between a converter carrier and an inverter carrier;

Fig. 5 is a timing chart showing operations of the inverter control unit and an arithmetic processing unit;

Fig. 6 is a timing chart showing operations of the converter control unit, the inverter control unit and the arithmetic processing unit;

Figs. 7 and 8 are timing charts showing operations of a first method of the first embodiment;

Fig. 9 is a flowchart showing operations of higher interrupt handling in the first method of the first embodiment.

Figs. 10 and 11 are timing charts showing operations of a second method of the first embodiment;

Fig. 12 is a flowchart showing operations of higher interrupt handling in the second method of the first embodiment;

Fig. 13 is a block diagram illustrating a part of a configuration of an inverter control unit in a second embodiment

Fig. 14 is a block diagram illustrating a part of a configuration of a converter control unit in the second embodiment;

Fig. 15 is a timing chart showing operations in the second embodiment;

Fig. 16 is a timing chart showing operations in a third embodiment;

Fig. 17 is a block diagram illustrating a configuration of a power converter adopted in a fourth embodiment;

Fig. 18 is a graph showing operations of a power converter when compared

with the fourth embodiment;

Fig. 19 is a graph showing operations of the power converter in the fourth embodiment;

Fig. 20 is a block diagram illustrating a configuration of a power converter adopted in a fifth embodiment;

Fig. 21 is a circuit diagram showing an equivalent circuit of a circuit shown in Fig. 20;

Fig. 22 is a graph showing operations of a power converter when compared with the fifth embodiment;

Fig. 23 is a graph showing operations of a power converter of the fifth embodiment; and

Fig. 24 is a graph showing behaviors of a variety of amounts in an example of the fifth embodiment.

Description of Embodiments

[0037] <First embodiment>

A. Configuration.

Fig. 1 is a block diagram illustrating a configuration of a power converter control device 1 according to this embodiment and a configuration of a power converter 2 to be controlled thereby.

[0038] The power converter 2 supplies a multi-phase AC current Iv to a load 3. The power converter 2 includes a converter 21 and an inverter 22. The converter 21 performs AC/DC conversion for an AC voltage, which is obtained from an AC power supply 8, and outputs a DC voltage Vdc. The inverter 22 receives the DC voltage Vdc from the converter 21, and outputs the multi-phase AC current Iv. For example, the load

the arithmetic processing unit 10.

[0048] Contents stored by the buffer registers 124a, 124b and 124c are transferred to the compare registers 123a, 123b and 123c, respectively, simultaneously with occurrence of the interrupt command R2. In Fig. 2, an output of the comparator 122d functions as the interrupt command R2, and in addition, serves as a transfer command to the compare registers 123a, 123b and 123c.

[0049] The contents stored in the compare registers 123a, 123b and 123c are all compared with a count value outputted from the timer 121.

[0050] The timer 121 functions as an up/down counter. The timer 121 counts up by the interrupt command R2. The timer 121 counting up, and the count value reaching the second period length Tinv stored in the compare register 123a, an output of the comparator 122a is activated, and causes the timer 121 to count down. The timer 121 counting down and the count value reaching a predetermined minimum value (for example, 0), the interrupt command R2 occurs by a function of the comparator 122d.

[0051] By appropriately setting timing at which the count value of the timer 121 is updated, the count value concerned becomes an inverter carrier K2 exhibiting a single triangular wave in the second period length Tinv. Then, the interrupt command R2 occurs at a predetermined minimum value (for example, 0). That is, the interrupt command R2 occurs at a trough of the triangular wave in the inverter carrier K2. Hence, thereafter, the interrupt command R2 is sometimes referred to as "trough interrupt".

[0052] Note that timing at which the output of the comparator 122a is activated corresponds to a position of a crest of the triangular wave in the inverter carrier K2. Hence, when the activation of the output of the comparator 122a is adopted as such an interrupt command, the interrupt command concerned is sometimes referred to as "crest interrupt".

[0067] Then, the interrupt command R2 occurs at troughs of the triangular wave in the inverter carrier K2, and accordingly, results in occurring at boundary points of time between the second periods Q1 and Q2 (these points are illustrated by the times t10, t20 and t30 in Fig. 4).

[0068] Note that, in the following description, in some cases, the boundary point of time between the second periods Q1 and Q2 that divide the same first period P into two (this point is illustrated by the time t20 in Fig. 4) is particularly referred to as a matching point of time, and is distinguished from the boundary point of time between the second periods Q1 and Q2 that belong to the first periods P different from each other (this point is illustrated by each of the times t10 and t30 in Fig. 4).

[0069] The following expression can be obtained by using this matching point of time. The first value Tinv1 indicates a length of time from a start point of time of the first period P to the matching point of time at which the converter carrier K1 takes the converter threshold value Ccnv. The first data Data1 corresponds to the second period Q1 having the first value Tinv1 as the second period length, and includes an inverter threshold value Dwm1 considered in the second period Q1. The second value Tinv2 indicates a length of time from the matching point of time to an end point of time of the first period P. The second data Data2 corresponds to the second period Q2 having the second value Tinv2 as the second period length, and includes an inverter threshold value Dwm2 considered in the second period Q2. The sample timing signal Tad is included in the first data Data1 if the second period Q1 is longer than the second period Q2, and is included in the second data Data2 if the second period Q2 is longer than the second period Q1. Hereinafter, it is assumed that the second value Tinv2 is larger than the first value Tinv1, and the second data Data2 also includes the sample timing signal Tad.

[0070] In Fig. 4, in the second period Q1 in which the inverter carrier K2 has the

[0086] (b-2) Operation explanation of comparative example.

Next, for comparison with the technology described in Fig. 4, a description will be made of control, as in Patent Document 3 and Non-Patent Document 3, for dividing one cycle for controlling the converter 21 into two sections at the time when the converter 21 commutates, and for controlling the inverter 22 in each of the sections (hereinafter, this control will be tentatively referred to as "two-division control").

[0087] Fig. 6 is a timing chart showing operations of the converter control unit 11, the inverter control unit 12 and the arithmetic processing unit 10 when the inverter carrier K2 uses a triangular wave having the same cycle as that of the converter carrier K1. Note that, here, an interrupt command R1[k] from the converter control unit 11 and the interrupt command R2[k] from the inverter control unit 12 occur at the same timing.

[0088] The inverter carrier K2 and the converter carrier K1 start in synchronization with each other, and the inverter threshold value Dpwm[k] is divided into two groups at the time when the converter carrier K1 takes the converter threshold value Ccnv, whereby PWM signals of the inverter 22 and the converter 21 are synchronized with each other.

[0089] As described above, the two-division control can be performed by a single-chip microcomputer instead of adopting a logic IC such as a CPLD and an FPGA.

[0090] Indeed, Non-Patent Document 3 talks about a possibility of application of a microcomputer to a direct power converter, and describes that a configuration is available by nine-phase voltage-source carrier comparison and general-purpose logic. In this mode, in order to realize PWM modulations by one triangular wave carrier, two sets of complementary PWM timers are applied, and general-purpose timers are used for three phases, then the synchronization of the PWM modulations can be realized by starting the carriers in synchronization with each other.

[0091] However, when the multi-phase AC current Iv has three phases, four to six

[0110] It is possible to make such a determination by adopting a so-called interrupt flag for the interrupt command R2. Such an interrupt flag is set by the occurrence of the interrupt command R2, and is reset by the end of the lower interrupt handling or the operation by the higher interrupt handling.

[0111] Specifically, the release of the interrupt command R2 in Step S101 can be realized by resetting the interrupt flag set by the occurrence of the interrupt command R2. Hence, a determination result of Step S106 turns to a positive determination result or a negative determination result depending on whether the interrupt flag is set or reset, respectively.

[0112] The case where the determination result of Step S106 is negative, that is, the case where the interrupt command R2 is not present after the interrupt command R2 that occurs concurrently with the interrupt command R1[k] during the arithmetic processing in the first period P[k] is a case where the arithmetic processing is shorter than the period length of the second period Q1[k]. Hence, Fig. 8 corresponds to this case.

[0113] In this case, the higher interrupt handling is ended, and the processing of the arithmetic processing unit 10 returns to the main routine.

[0114] When the first interrupt command R2 occurs firstly after the arithmetic processing in the first period P[k] is ended, as lower interruption processing by this, writing of the first data Data1 [k+1] to the buffer register BuffReg is executed. However, since Fig. 9 is a flowchart for the higher interrupt handling, such lower interrupt handling is not shown.

[0115] There is a required time for writing the first data Data1[k+1] into the buffer register BuffReg by this lower interrupt handling. Specifically, there is a time required for branching from the main routine to the lower interrupt handling and writing to the buffer register BuffReg. Hence, the writing is delayed from the occurrence of the interrupt command R2. In Fig. 8, the lower interruption processing is drawn on a lower

the order of several microseconds). Then, the period length of the second period Q2[k+1] is not shortened to the dead time or less. This is because the second period Q2[k+1] of such a period length does not affect the multi-phase AC current Iv outputted by the inverter 22.

[0144] Since there is such a relationship with regard to the length of time, there is no practical significance of setting the period length of the second period Q2[k+1] to the required time for the lower interrupt handling or less. That is, a minimum value of the period length of the second period Q2[k+1] just needs to be limited to the required time or more.

[0145] <Second embodiment>

Fig. 13 is a block diagram illustrating a part of a configuration of an inverter control unit 12 in this embodiment. This configuration is different from the configuration of the inverter control unit 12 in the first embodiment in that the value inputted to the comparator 122d is caused to differ, and that not only the activation of the output of the comparator 122d but also activation of the comparator 122a is used as a trigger for the transfer from the buffer register BuffReg to the compare register CompReg. Moreover, an OR gate 129 is also added.

[0146] That is, the comparator 122d compares the count value of the timer 121 with the value (which is not a fixed minimum value as in the first embodiment) stored in the compare register 123a, and causes the timer 121 to count up when both of them match with each other. On the other hand, in a similar way to the first embodiment, the comparator 122a compares the count value of the timer 121 with the value stored in the compare register 123a, and causes the timer 121 to count down when both of them match with each other.

[0147] Then, the OR gate 129 causes the interrupt command R2 to occur when either

one of the comparators 122a and 122d is activated. That is, in this embodiment, the interrupt command R2 is both a crest interrupt and a trough interrupt.

[0148] However, the OR gate 129 is shown for convenience of explanation in the figure, and it is not necessary to provide the OR gate 129 as an actual constituent.

[0149] Moreover, the comparator 122d can be integrated with the comparator 122a, and an output thereof can be used as the interrupt command R2 and a transfer command for transfer from the buffer registers 124a, 124b and 124c to the compare registers 123a, 123b and 123c. The timer 121 in this case has a function to alternately count up/count down every time when the output of the integrated comparator 122a is activated.

[0150] Fig. 14 is a block diagram illustrating a part of a configuration of a converter control unit 11 in this embodiment. This configuration is different from the configuration of the converter control unit 11 in the first embodiment only in that an OR gate 119 and a comparator 112d are added thereto, and that the timer 111 is caused to function as an up/down counter.

[0151] That is, the comparator 112d compares the count value of the timer 111 with a fixed minimum value (for example, 0), and causes the timer 121 to count up when both of them match with each other. On the other hand, in a similar way to the first embodiment, the comparator 112a compares the count value of the timer 111 with the value (first period length Tcnv) stored in the compare register 113a, and causes the timer 111 to count down when both of them match with each other.

[0152] The OR gate 119 causes the interrupt command R1 to occur when either one of the comparators 112a and 112d is activated. That is, in this embodiment, the interrupt command R1 can be said to be both a crest interrupt and a trough interrupt when the interrupt command R1 is expressed in a similar way to the expression used for the interrupt command R2.

[0153] Note that the OR gate 119 is shown for convenience of explanation in the figure, and it is not necessary to provide the OR gate 119 as an actual constituent.

[0154] Note that the transfer timing from the buffer registers 114a and 114c to the compare registers 113a and 113c is the same as the occurrence of the interrupt command R1 in a similar way to the first embodiment. However, unlike the first embodiment, the output of the comparator 112a does not directly function as the interrupt command R1. Here, the case where the interrupt command R1 is adopted as the transfer command for transfer from the buffer registers 114a and 114c to the compare registers 113a and 113c is illustrated.

[0155] The converter control unit 11 and the inverter control unit 12, which are as described above, can be realized by a known configuration commonly called the multi-function timer pulse unit in a similar way to those in the first embodiment.

[0156] With the above-described configuration, the interrupt command R1 becomes the trough interrupt and the crest interrupt, which are based on the converter carrier K1, and the interrupt command R2 becomes the trough interrupt and the crest interrupt, which are based on the inverter carrier K2.

[0157] Fig. 15 is a timing chart showing operations in this embodiment. Also in Fig. 15, in a similar way to Figs. 7 and 8, the symbol [k] is appended to symbols indicating the variety of amounts in the k-th cycle.

[0158] Here, for the sake of simplicity, a description will be made while taking as an example the case where the arithmetic processing in the first period P[k], which is for obtaining the first data Data1[k+1] and the second data Data2[k+1], is longer than the second period Q1[k], and is naturally shorter than the first period P[k]. However, considering that the arithmetic processing in the first period P[k] may be shorter than the second period Q1[k], it is desirable that either of the first method and the second method, which are described in the first embodiment, be adopted.

[0159] Also in this embodiment, the timers 111 and 121 operate in synchronization with each other, and the converter carrier K1 and the inverter carrier K2 are synchronized with each other.

[0160] Since the timer 111 functions as the up/down counter, the converter carrier K1 apparently exhibits not a sawtooth wave but a triangular wave.

[0161] In Fig. 15, the second data Data2[n], which is already obtained in the first period P[n-1] and held as a variable by the interrupt command R1[n] serving as the trough interrupt for the converter carrier K1, is written into the buffer register BuffReg. However, before this writing, the first data Data1[n] is transferred from the buffer register BuffReg to the compare register CompReg at the same timing as the occurrence of the interrupt command R1[n]. In this way, from the beginning of the second period Q1[n], a variety of amounts (not shown) included in the first data Data1[n] are compared with the inverter carrier K2 in the second period Q1[n].

[0162] At the same timing as the occurrence of the interrupt command R1[n], the converter carrier K1 starts to rise, and the first period P[n] starts.

[0163] A second period length Tinv1[n] (not shown) included in the first data Data1[n] defines a minimum value of the inverter carrier K2. Since the inverter carrier K2 falls in the second period Q1[n], end timing of the second period Q1[n] is determined by the second period length Tinv1[n]. For the second period length Tinv1[n], a value corresponding to a time until the converter carrier K1 reaches the converter threshold value Ccnv from a minimum value (for example, 0) is set, and at the matching point of time J[n], the inverter carrier K2 starts rising.

[0164] The second period Q2[n] starts from the matching point of time J[n]. The second data Data2[n] is transferred from the buffer register BuffReg to the compare register CompReg at the matching point of time J[n], and accordingly, from the beginning

indicates that two elements are connected in parallel to each other, and that conduction directions of the two elements are opposite to each other.

[0197] Switching signals Syp and Syn are inputted to the switches Qyp and Qyn, respectively. Each of the switches Qyp is made conductive/nonconductive in response to active/non-active of the switching signal Syp, and each of the switches Qyn is made conductive/nonconductive in response to active/non-active of the switching signal Syn. Hence, the switching signals Sxp and Sxn compose the converter switching signal Scnv.

[0198] Such operations themselves of the converter 21 and the inverter 22, which are based on the switching signals Sxp, Sxn, Syp and Syn, are known, for example, by Patent Document 3 and Non-Patent Documents 1 to 3, and accordingly, a detailed description thereof will be omitted. However, a brief description will be made of portions serving as the premise of the description of this embodiment.

[0199] Now, it is assumed that the voltage Vt is the minimum phase, and the voltages Vr and Vs become the maximum phase and the intermediate phase, respectively. Due to symmetry of a phase voltage waveform, such assumption does not lose generality by exchanging a phase sequence and by exchanging phases of the switches Qxp and Qxn.

[0200] Then, when such an assumption is made, both of line-to-line voltages (Vr-Vt) and (Vs-Vt) are positive, and these are selectively outputted as the DC voltage Vdc. Such a selective output is realized in such a manner that there are selected: a first state in which the switches Qrp and Qtn are turned on and the switches Qrn and Qtp are turned off; and a second state in which the switches Qtn and Qrp are turned on and the switches Qtp and Qsn are turned off. A period while the first state is maintained is the first section mentioned above, and a period while the second state is maintained is the second section mentioned above. Then, switching between the first state and the second state is understood as commutation of the converter 21, which accompanies the exchange of the

maximum phase, the intermediate phase and the minimum phase among the voltages Vr, Vs and Vt.

[0201] FIG. 18 is a graph showing operations of the power converter 2 when the technology known from Patent Document 3 and Non-patent Document 3 is adopted, and is shown for comparison with this embodiment. Timing of the commutation of the converter 21 can be determined by a symmetric triangular wave C1 and flow ratios D6 and D4 (= 1-D6). When a cycle of the symmetric triangular wave is ts, a maximum value thereof is 1, and a minimum value thereof is 0, then the first section is present continuously in a length D6·ts, and the second section is present continuously in a length D4·ts.

[0202] Voltage-source trapezoidal waves are for signal waves Vr*, Vs* and Vt*, whereby the commutation of the converter 21 is performed on the basis of two voltage vectors. Hence, the converter 21 commutates at a point in time when the symmetric triangular wave C1 becomes equal to one of the flow ratios, for example, the flow ratio D4. As shown in Patent Document 3, such commutation of the converter 21, is realized by the switching pattern of the converter 21, which is obtained by performing current-source gate conversion.

[0203] A desirable way of selecting the flow ratios D4 and D6 is known, and accordingly, is omitted here. However, the first period length Tcnv, the converter carrier K1, and the converter threshold value Ccnv, which are described in the above-described "(b-2) Operation explanation of comparative example", correspond to the cycle ts, the symmetric triangular wave C1, and the flow ratio D4, respectively (refer to Fig. 6).

[0204] In Fig. 18, a symmetric triangular wave C2 takes the minimum value 0 and the maximum value 1. The symmetric triangular wave C2 is compared with voltage command values D4(1-d0-d4), D4(1-d0), D4+D6·d0 and D4+D6(d0+d4). The values

threshold values Dpwm, which are described in the above-described "(b-2) Operation explanation of comparative example", correspond to the symmetric triangular wave C2 and the voltage command values, respectively (refer to Fig. 6).

[0244] Fig. 22 shows a case where so-called two-phase modulation is performed, in which Vw* = 0 is adopted. In this case, the voltage command values drec·Vw* and drec+dz+dc(1-Vw*) become 0 and 1, respectively, which match with the minimum value and maximum value of the symmetric triangular wave C2, respectively. Hence, when the two-phase modulation is performed, the voltage command values drec·Vw* and drec+dz+dc(1-Vw*) can be omitted.

[0245] The voltage command value drec·Vy* is smaller than the rectification duty drec by a value drec(1-Vy*), and the voltage command value drec+dz+dc(1-Vy*) is smaller than the discharge complementation duty (1-dc) (= drec+dz) by a value dc(1-Vy*) (as mentioned above, the symbol y represents the symbols u, v and w).

[0246] The switching signals Sup, Svp and Swp are illustrated in a similar way to the fourth embodiment, and the switching signals Sun, Svn and Swn are omitted.

[0247] Hence, by using these voltage command values, the inverter 22 operates on the basis of the voltage vectors V0, V4 and V6, which are adopted in periods at a ratio (1-Vu*): (Vu*-Vv*): (Vv*-Vw*) in both of the periods tc and trec in the cycle ts, and the voltage vector V0 is adopted in the sections including the timing at which the converter commutates (the sections also include the periods tz/2), whereby the converter commutates in a state in which the DC current Idc does not flow.

[0248] Hence, if the pair of periods tz/2 and the period trec are collectively considered as a period trec', Fig. 22 shows the above-mentioned two-division control. Note that a fall of the signal, which is denoted by the symbol int, indicates a trough interrupt corresponding to the interrupt command R2 shown in Fig. 6.

correspond to the inverter threshold values Dpwm mentioned in the first embodiment.

[0255] The second period Q1 is determined by the second period length Tinv1, and the inverter carrier K2 takes the discharge duty dc as the maximum value in the period tc. Here, the two-phase modulation is adopted, and the voltage command value dc(1-Vw*) is equal to the discharge duty dc. Hence, the voltage command value dc(1-Vw*) as a comparison object of the inverter carrier K2 can be omitted. Whether or not such omission is present corresponds to the fact that there are a case where there are three types of the inverter threshold values Dpwm, and a case where there are two types thereof.

[0256] In the period trec' corresponding to the second period Q2, the inverter carrier K2 is compared with voltage command values dz+drec(1-Vu*), dz+drec(1-Vv*) and dz+drec(1-Vw*), which correspond to the inverter threshold values Dpwm mentioned in the first embodiment.

[0257] The second period Q2 is determined by the second period length Tinv2, and the inverter carrier K2 takes the discharge complementation duty (1-dc)(=dz+drec) as the maximum value in the period trec'. Here, the two-phase modulation is adopted, and the voltage command value dz+drec(1-Vw*) is equal to the discharge complementation duty (1-dc). Hence, the voltage command value dz+drec(1-Vw*) as a comparison object of the inverter carrier K2 can be omitted. Whether or not such omission is present also corresponds to the fact that there are a case where there are three types of the inverter threshold values Dpwm, and a case where there are two types thereof.

[0258] It is obvious that the periods in which the voltage vectors V0, V4 and V6 are adopted, the periods being obtained as described above, are obtained in the same way as in the case shown in Fig. 22. Note that the timing at which the interrupt command R2 shown in Fig. 7 occurs is shown as a fall of a signal denoted by a symbol int in Fig. 23.

[0265] More specifically, in the MTU0, the PWM 1 mode is adopted, and the values SSc* and carr* stored in the compare registers TGRA and TGRB are transferred from the values SSc0* and carr0* written in the buffer registers TGRC and TGRD, which correspond to the converter threshold value Ccnv and the first period length Tcnv, respectively.

[0266] The MTU0 outputs the signal SSc corresponding to the converter switching signal Scnv from an input/output terminal MTIOC0A, and controls the opening and closing of the switch Sc in the fifth embodiment. Specifically, when the signal SSc is "H", the switch Sc becomes conductive, and when the signal SSc is "L", the switch Sc becomes non-conductive.

[0267] In the MTU3 and the MTU 4, a complementary PWM mode is adopted. Values U*, V* and W*, which are stored in a compare register TGRB of the MTU3 and compare registers TGRA and TGRB of the MTU4, are values transferred from values U0*,V0* and W0*, written in a buffer register TGRE of the MTU3 and buffer registers TGRC and TGRD of the MTU4, respectively, and correspond to the inverter threshold values Dpwm. A value (carr+td) stored in the compare register TGRA of the MTU 3 is a value transferred from a value (carr+td0) stored in a buffer register TGRC of the MTU3, and corresponds to the second period length Tinv.

[0268] Signals U, X, V, W, Y and Z, which correspond to the switching signals Sup, Sun, Svp, Svn, Swp and Swn, are outputted from input/output terminals MTIOC3B and MTIOC3D of the MTU3 and input/output terminals MTIOC4A, MTIOC4B, MTIOC4C and MTIOC4D of the MTU4, respectively. From an input/output terminal MTIOC3A of the MTU3, a toggle output carr synchronized with the cycle corresponding to the second periods Q1 and Q2 is outputted.

[0269] Note that the above-mentioned compare registers and buffer registers of the

CLAIMS

1. A power converter control device for controlling a power converter including a converter that performs AC-DC conversion and an inverter that receives a DC voltage from said converter and supplies a multi-phase AC current, said power converter control device comprising:

a converter control unit that outputs a converter switching signal for determining switching of said converter based on a result of performing comparison between a converter carrier and a converter threshold value in each of first periods repeated while having a first period length; and

an inverter control unit that outputs an inverter switching signal for determining switching of said inverter based on a result of performing comparison between an inverter carrier and an inverter threshold value in each of second periods synchronized with said converter carrier and repeated while having a second period length,

wherein, in said first period, first data and second data are alternately given to said inverter control unit, said first data including a first value indicating a length of time from a start point of time of said first period to a matching point of time as a point of time when said converter carrier takes said converter threshold value and said inverter threshold value corresponding to said second period having said first value as said second period length, and said second data including a second value indicating a length of time from said matching point of time to an end point of time of said first period and said inverter threshold value corresponding to said second period having said second value as said second period length.

2. The power converter control device according to claim 1, further comprising:

an arithmetic processing unit that performs arithmetic processing for obtaining said first data and said second data for a pair of said second periods, said arithmetic processing being performed every said first period,

wherein said inverter control unit includes:

a buffer register which stores said inverter threshold value and said second period length;

a compare register to which contents stored by said buffer register are transferred at a boundary point of time as a point of time serving as a boundary between said second periods;

a timer that generates a count value that is compared with said second period length stored in said compare register and becomes said inverter carrier; and

a switching signal generation unit that generates said inverter switching signal on the basis of the result of said comparison between said inverter threshold value stored in said compare register and said inverter carrier, and

said first data obtained by said arithmetic processing in one of said first periods is stored in said buffer register before the start of another of said first periods, said second data obtained by said arithmetic processing in said one of said first periods is stored in said buffer register on an occasion of the start of said another of said first periods, and said another of said first periods is present immediately after said one of said first periods.

3. The power converter control device according to claim 2,

wherein said first data

(a) on and after an end time of said arithmetic processing when said boundary point of time is present after the start of said arithmetic processing and before the end of said arithmetic processing,

(b) when said boundary point of time is not present after the start of said arithmetic processing and before the end of said arithmetic processing, by processing by an interrupt command occurring at a first one of said boundary point of time after the end of said arithmetic processing,

is stored in said buffer register in these individual cases.

4. The power converter control device according to claim 3,

wherein said first data

(a1) is stored in said buffer register at the time when said arithmetic processing is ended when said boundary point of time is present after the start of said arithmetic processing and before the end of said arithmetic processing.

5. The power converter control device according to claim 3,

wherein said first data

(a2) when said boundary point of time is present after the start of said arithmetic processing and before the end of said arithmetic processing, is stored in said buffer register by interrupt handling by an interrupt command occurring at a first one of said boundary point of time after the end of said arithmetic processing.

6. The power converter control device according to any one of claims 1 to 5, wherein said inverter carrier exhibits a single triangular wave in each of said second periods.

7. The power converter control device according to any one of claims 1 to 5,

wherein said converter carrier repeats a monotonic increase and a monotonic decrease every said first period, and

said inverter carrier repeats a monotonic increase and a monotonic decrease every said second period.

8. The power converter control device according to any one of claims 1 to 5, wherein said converter carrier exhibits a sawtooth wave having said first period length as a cycle, and

said inverter carrier repeats a monotonic increase and a monotonic decrease every said second period.

9. The power converter control device according to any one of claims 1 to 8, wherein said converter is a current source converter, and commutates at said matching point of time by said converter switching signal.

10. The power converter control device according to any one of claims 1 to 8, wherein said converter includes a rectifier circuit and a booster circuit, and it is determined whether or not said booster circuit contributes to said dc voltage on the basis of said converter switching signal.