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CACHE POLLUTION AVOIDANCE INSTRUCTIONS



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ABSTRACT

A computer system and method for providing cache memory management. The computer system comprises a main memory having a plurality of main memory addresses each having a corresponding data entry, and a processor coupled to the main memory. At least one cache memory is coupled to the processor. The at least one cache memory has a cache directory with a plurality of addresses and a cache controller having a plurality of data entries corresponding to the plurality of addresses. The processor receives an instruction having an operand address and determines if the operand address matches one of the plurality of addresses in the cache directory. If so, the processor updates a data entry in the cache controller corresponding to the matched address. Otherwise, a data entry corresponding to the operand address in the main memory is updated.

Figure 1