PATENT SPECIFICATION (11) 1369357

1369357

(21) Application No. 5763/72 (22) Filed 8 Feb. 1972

(31) Convention Application No. 114861 (32) Filed 12 Feb. 1971 in

(33) United States of America (US)

(44) Complete Specification published 2 Oct. 1974

(51) International Classification H01L 7/44

(52) Index at acceptance

H1K 211 238 243 246 248 273 277 306 312 353 41Y 422 574 578 579 581 583 597 611 615 618 61Y 62Y 650

(72) Inventor JERRY MAR

(19)

(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a method of making semiconductive devices which contain a p-n junction that is operable in avalanche breakdown, and to devices made thereby. The invention finds particular, though not exclusive, application in the production of avalanche transistors for use as memory cells.

In a p-n diode, such as the emitter-base junction of the n-p-n transistor described in copending application no. 60662/71 (Serial no. 1358190), when a sufficiently large reverse-bias is applied to the junction it breaks down and conducts in the reverse direction. This characteristic is known as avalanche breakdown. Typically, junctions of this type are formed by the diffusion through apertures in masks of impurities to convert the conductivity of the diffused region. The resulting junction has a planar central portion and a curved surrounding edge portion which extends to the surface. This geometry of the junction favours the occurrence of breakdown at the surface or at the curved edge of the junction. It can be shown that such breakdown at the surface tends to degrade the performance of the junction and therefore transistor performance.

Various techniques have been suggested to prevent breakdown at the surface of a p-n junction avalanche device, e.g., in U.S. patents 3,514,846 and 3,345,221 which describe the use of a p-type layer on top of a p^+-type layer to increase the reverse breakdown potential at the surface of the device in order to force breakdown to occur below the surface. However these techniques use at least two separate oxide masking steps and two diffusing steps to fabricate a diode. Extending these techniques to the fabrication of an avalanche transistor would require three or more separate masking and diffusing steps. These relatively complicated fabrication processes are undesirable in many instances since they would add substantially to the cost of the devices produced.

According to this invention there is provided a method of making a semiconductive device including the steps of diffusing into a portion of a semiconductive layer of a first conductivity type exposed by an aperture in a mask masking said layer a first impurity to convert the conductivity type of said portion, increasing the area exposed of said portion, and diffusing into the increased exposed portion a second impurity to convert the conductivity type of a region of the first diffused portion, whereby the impurity concentration at the surface part of the p-n junction thereby formed between said region and said portion is significantly less than that at said junction below said surface part.

Preferably said layer comprises an epitaxial layer formed on a relatively low resistivity substrate of said first conductivity type.

Preferably said first diffused portion extends through the depth of said layer.

Preferably the diffusion of said first impurity extends into said substrate.

The invention will now be described by way of example with reference to the accompanying drawing, in which:

Fig. 1 shows in cross section a transistor fabricated in accordance with the invention;

Figs. 2A to 2D show the transistor of Fig. 1 in various stages of its manufacture; and

Fig. 3 is a graph of surface impurity concentration as a function of distance.

In the transistor 10 shown in Fig. 1, a monocrystalline silicon wafer 11 is composed of a bulk portion 12 which is of low resistivity n-type material and a surface portion which includes a higher resistivity n-type region 14 which surrounds a localized low resistivity

n-type region 18. Region 18 forms a substantially flat p-n^+ junction with region 16. Region 16 also forms a substantially flat p-n junction 20A with the bulk portion 12 of the substrate and a curved edge portion 20B with the n-type region 14.

When the p-n junction formed by regions 16 and 18 is sufficiently reverse-biased avalanche breakdown operation is achieved. The breakdown would normally tend to occur at the surface of the junction 22A or along the curved portion of the junction 22B. One reason for the undesired preferential breakdown at the surface is the effect of the discontinuity of the junction on electric field lines. Repeated breakdown at the surface 22A tends to damage the device and then degrade its performance. If the concentration of impurities at the junction surface 22A is significantly lowered, breakdown will tend to occur away from the surface along curved portion 22B or the relatively flat portion of the junction 22C, thereby avoiding such degradation of transistor performance.

Metal contact 24 is attached to region 18 which serves as the emitter. The epitaxial layer 14 and bulk portion 12 serve as the collector. Metal contact 26 is attached to the n^+-type region 28 which is surrounded by and in electrical contact with the epitaxial layer 14.

A noncontacted base transistor of the kind shown in Fig. 1 may be made as follows. Referring to Fig. 2A, on one surface of a monocrystalline silicon wafer 12 in which arsenic is the predominant significant impurity with a concentration of about 10^{18} atoms per cc. to result in an n^+-type resistivity of about 0.03 ohm per square cm., there is grown, using conventional techniques, an epitaxial layer 32 about 2 microns thick in which arsenic is the predominant impurity with a concentration of about 10^{15} atoms per cc. to result in an n-type resistivity of about 0.5 ohm-cm. Next, using conventional techniques, an 8000 angstrom layer of oxide 30, typically silicon dioxide, is grown on top of the epitaxial layer 32 and then an aperture in the oxide is formed. Then, using well-known techniques, boron impurities are diffused through the entire aperture in the masking layer into the exposed central portion of the epitaxial layer down to and into the substrate. The boron impurities convert the diffused-into region, which serves as the base 34 of the transistor, from n-type to p-type material. The p-type base diffusion 34 forms a p-n junction with the n^+-type substrate 12 and the n-type epitaxial layer 32.

Normally, the lateral extent of diffusion of a p-n junction is about equal to its vertical extent; however, in this case, the lateral extent of the base was about 3 microns while the vertical extent was only about 2 microns. The increased lateral diffusion is due to the fact that when the vertical base diffusion reaches the n^+-type substrate the concentration of p-impurities is less than the concentration of n-impurities and therefore the vertical advance of the junction is effectively halted, while the lateral diffusion continues in the epitaxial layer.

The wafer is then subjected to a buffered hydrofluoric etch solution which removes about 2500 angstroms from the oxide layer and any impurities that may have formed over the exposed epitaxial region. The resulting structure is shown in Fig. 2B where the diameter of the aperture in the oxide mask 36 has been increased by an amount $2x_a$.

Referring now to Fig. 2C, a photoresist coating, typically KPR, is then placed over the entire wafer and using conventional techniques a second aperture in the oxide layer is formed exposing a second region in the epitaxial layer. The wafer is then placed in a phosphorus diffusion furnace where an n^+-type acceptor impurity is diffused through both the enlarged first aperture and the second aperture to form n^+-type regions 18 and 28. This diffusion converts region 18 of the p-type material to an n^+-type emitter and region 28 of the n-type material epitaxial layer to an n^+-type material region.

The base region 16 surrounds region 18 forming a p-n^+ junction having a surface portion 22A, a curved portion 22B, and a relatively flat portion 22C. The n^+-type region 28 provides a low resistivity surface on which to deposit a metal contact. Using conventional techniques, a metal contact 26 is formed on top of n^+-type region 28 and another metal contact 24 is formed on top of n^+-type region 18. These contacts may be transparent.

Now referring to Fig. 2D, there is shown an enlarged partial view of Fig. 2C. The amount of decrease in the edge of the aperture in the oxide mask is shown by x_a. With the edge of the original aperture used as a reference point, the distance at which the surface portion of the emitter-base junction forms is shown as x_2. The distance at which the junction would have formed had the aperture not been increased prior to the emitter diffusion is shown as x_1 and the curved portion of the junction 38 is shown as a dashed line.

Now referring to Fig. 3, there is illustrated a semilog plot of emitter and base surface impurity concentration as a function of distance from the original aperture edge in the $+x$ direction. The point $x=0$ corresponds to the edge of the original aperture prior to enlargement. Curve 1 is a plot of base surface impurity concentration as a function of distance from the reference point $x=0$. Dotted curve 2 is a hypothetical plot of emitter surface impurity concentration versus distance, assuming that the emitter and base diffusion were both diffused through the original

unincreased aperture. Curve 3 is a plot of the actual emitter surface impurity concentration obtained when the aperture is increased by an amount x_a (see Fig. 2D) prior to the emitter diffusion.

The value of the y coordinate y_1, which is the intersection of curves 1 and 2, is the impurity concentration that would occur at the surface of a p-n junction formed by diffusing the base and emitter impurities through the original unincreased aperture. The value of impurity concentration along the flat bulk region of such a fabricated diode would be about equal to this surface value. As has been discussed, this is an undesirable situation since avalanche breakdown in this case will tend to occur along the surface of the p-n junction which degrades transistor performance. It is therefore desirable to reduce the surface concentration of impurities without affecting the bulk concentration so as to cause breakdown to occur below the surface.

Curve 3, which is a plot of the actual emitter surface impurity concentration versus distance from the original aperture, is identical to curve 2 except that it is offset from curve 2 by an amount x_a. The amount of offset of curve 3 with respect to curve 2 is determined by moving curve 2 in the $+x$ direction until it intersects curve 1 at y coordinate y_2, which is at least 1 order of magnitude lower than y_1. The amount of the offset x_a is the effective amount that the aperture must be increased before the emitter diffusion in order to lower the surface concentration of impurities of the resulting p-n junction to ensure that avalanche breakdown occurs below the surface of the junction.

The x coordinate of the intersection of curves 1 and 2, x_1, represents the lateral distance from the edge of the original aperture that the resulting surface region of the p-n junction would form if the emitter and base were diffused through the exact same aperture. The x coordinate of the intersection of curves 1 and 3, x_2, represents the distance from the edge of the original aperture where the surface region of the actual emitter-base junction formed. As is clear from the graph coordinate x_2 is more positive than coordinate x_1, and therefore the surface region of the p-n junction formed when the aperture is increased by an amount x_a prior to the emitter diffusion is located at a point along the surface of the transistor further from the original aperture edge and closer to the n-type epitaxial collector than would be the case if both the base and emitter diffusions were made through the same aperture. This decrease in distance between the emitter and collector tends to cause emitter-collector shorts which are very undesirable.

A solution to the problem of emitter-collector shorts is to increase the extent of the lateral diffusion of the base without changing the extent of the lateral diffusion of the emitter. An increased extent of the lateral diffusion of the base would provide a greater initial distance between the original unincreased aperture edge and the n-type epitaxial layer collector than normally occurs. This increased distance compensates for the increased extent of the lateral diffusion of the emitter caused by increasing the aperture prior to the emitter diffusion.

One conventional method used to increase the extent of the lateral diffusion of the base is to increase the extent of the vertical diffusion of the base since the extent of the latheral diffusion generally is directly proportional to the vertical diffusion. This method has the undesired effect of increasing the effective base width of the transistor and therefore limiting transistor parameters such as beta and base transit time. In the example described, however, an increase in the extent of the lateral diffusion of the base without an increase in the effective base width of the transistor has been achieved, as explained in the discussion of Fig. 2A, by depositing on an n^+-type substrate 12 an n-type epitaxial layer 32 and diffusing a p-type material base 34 completely through the epitaxial layer into the substrate. The resultant increase in the extent of the lateral diffusion of the base with virtually no increase in the effective base width lessens the problem of emitter-collector shorts without limiting transistor parameters.

Clearly of course various modifications are possible. For example, the base region may be made photosensitive so as to form a photo-avalanche transistor. Materials other than those specifically mentioned may, where suitable, be used instead. The substrate may be used as the emitter and the n^+ diffusion used as the collector.

WHAT WE CLAIM IS:—

1. A method of making a semiconductive device including the steps of diffusing into a portion of a semiconductive layer of a first conductivity type exposed by an aperture in a mask masking said layer a first impurity to convert the conductivity type of said portion, increasing the area exposed of said portion, and diffusing into the increased exposed portion a second impurity to convert the conductivity type of a region of the first diffused portion, whereby the impurity concentration at the surface part of the p-n junction thereby formed between said region and said portion is significantly less than that at said junction below said surface part.

2. A method as claimed in claim 1 wherein said layer comprises an epitaxial layer formed on a relatively low resistivity substrate of said first conductivity type.

3. A method as claimed in claim 2 wherein said first diffused portion extends through the depth of said layer.

unincreased aperture. Curve 3 is a plot of the actual emitter surface impurity concentration obtained when the aperture is increased by an amount x_a (see Fig. 2D) prior to the emitter diffusion.

The value of the y coordinate y_1, which is the intersection of curves 1 and 2, is the impurity concentration that would occur at the surface of a p-n junction formed by diffusing the base and emitter impurities through the original unincreased aperture. The value of impurity concentration along the flat bulk region of such a fabricated diode would be about equal to this surface value. As has been discussed, this is an undesirable situation since avalanche breakdown in this case will tend to occur along the surface of the p-n junction which degrades transistor performance. It is therefore desirable to reduce the surface concentration of impurities without affecting the bulk concentration so as to cause breakdown to occur below the surface.

Curve 3, which is a plot of the actual emitter surface impurity concentration versus distance from the original aperture, is identical to curve 2 except that it is offset from curve 2 by an amount x_a. The amount of offset of curve 3 with respect to curve 2 is determined by moving curve 2 in the $+x$ direction until it intersects curve 1 at y coordinate y_2, which is at least 1 order of magnitude lower than y_1. The amount of the offset x_a is the effective amount that the aperture must be increased before the emitter diffusion in order to lower the surface concentration of impurities of the resulting p-n junction to ensure that avalanche breakdown occurs below the surface of the junction.

The x coordinate of the intersection of curves 1 and 2, x_1, represents the lateral distance from the edge of the original aperture that the resulting surface region of the p-n junction would form if the emitter and base were diffused through the exact same aperture. The x coordinate of the intersection of curves 1 and 3, x_2, represents the distance from the edge of the original aperture where the surface region of the actual emitter-base junction formed. As is clear from the graph coordinate x_2 is more positive than coordinate x_1, and therefore the surface region of the p-n junction formed when the aperture is increased by an amount x_a prior to the emitter diffusion is located at a point along the surface of the transistor further from the original aperture edge and closer to the n-type epitaxial collector than would be the case if both the base and emitter diffusions were made through the same aperture. This decrease in distance between the emitter and collector tends to cause emitter-collector shorts which are very undesirable.

A solution to the problem of emitter-collector shorts is to increase the extent of the lateral diffusion of the base without changing the extent of the lateral diffusion of the emitter. An increased extent of the lateral diffusion of the base would provide a greater initial distance between the original unincreased aperture edge and the n-type epitaxial layer collector than normally occurs. This increased distance compensates for the increased extent of the lateral diffusion of the emitter caused by increasing the aperture prior to the emitter diffusion.

One conventional method used to increase the extent of the lateral diffusion of the base is to increase the extent of the vertical diffusion of the base since the extent of the latheral diffusion generally is directly proportional to the vertical diffusion. This method has the undesired effect of increasing the effective base width of the transistor and therefore limiting transistor parameters such as beta and base transit time. In the example described, however, an increase in the extent of the lateral diffusion of the base without an increase in the effective base width of the transistor has been achieved, as explained in the discussion of Fig. 2A, by depositing on an n^+-type substrate 12 an n-type epitaxial layer 32 and diffusing a p-type material base 34 completely through the epitaxial layer into the substrate. The resultant increase in the extent of the lateral diffusion of the base with virtually no increase in the effective base width lessens the problem of emitter-collector shorts without limiting transistor parameters.

Clearly of course various modifications are possible. For example, the base region may be made photosensitive so as to form a photo-avalanche transistor. Materials other than those specifically mentioned may, where suitable, be used instead. The substrate may be used as the emitter and the n^+ diffusion used as the collector.

WHAT WE CLAIM IS:—

1. A method of making a semiconductive device including the steps of diffusing into a portion of a semiconductive layer of a first conductivity type exposed by an aperture in a mask masking said layer a first impurity to convert the conductivity type of said portion, increasing the area exposed of said portion, and diffusing into the increased exposed portion a second impurity to convert the conductivity type of a region of the first diffused portion, whereby the impurity concentration at the surface part of the p-n junction thereby formed between said region and said portion is significantly less than that at said junction below said surface part.

2. A method as claimed in claim 1 wherein said layer comprises an epitaxial layer formed on a relatively low resistivity substrate of said first conductivity type.

3. A method as claimed in claim 2 wherein said first diffused portion extends through the depth of said layer.

* C L M S *

4. A method as claimed in claim 3 wherein the diffusion of said first impurity extends into said substrate.

5. A method as claimed in any one preceding claim wherein said second impurity is diffused into another portion of said layer to decrease the resistivity thereof, and contacts to said other diffused portion and said region are provided.

6. A method as claimed in claim 5 wherein said contacts are transparent.

7. A method of making a semiconductive device substantially as herein described with reference to the accompanying drawing.

8. A semiconductive device made by a method as claimed in any one preceding claim.

C. S. T. BUCKLEY,
Chartered Patent Agent,
5, Mornington Road,
Woodford Green, Essex.
Agent for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1974.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

