

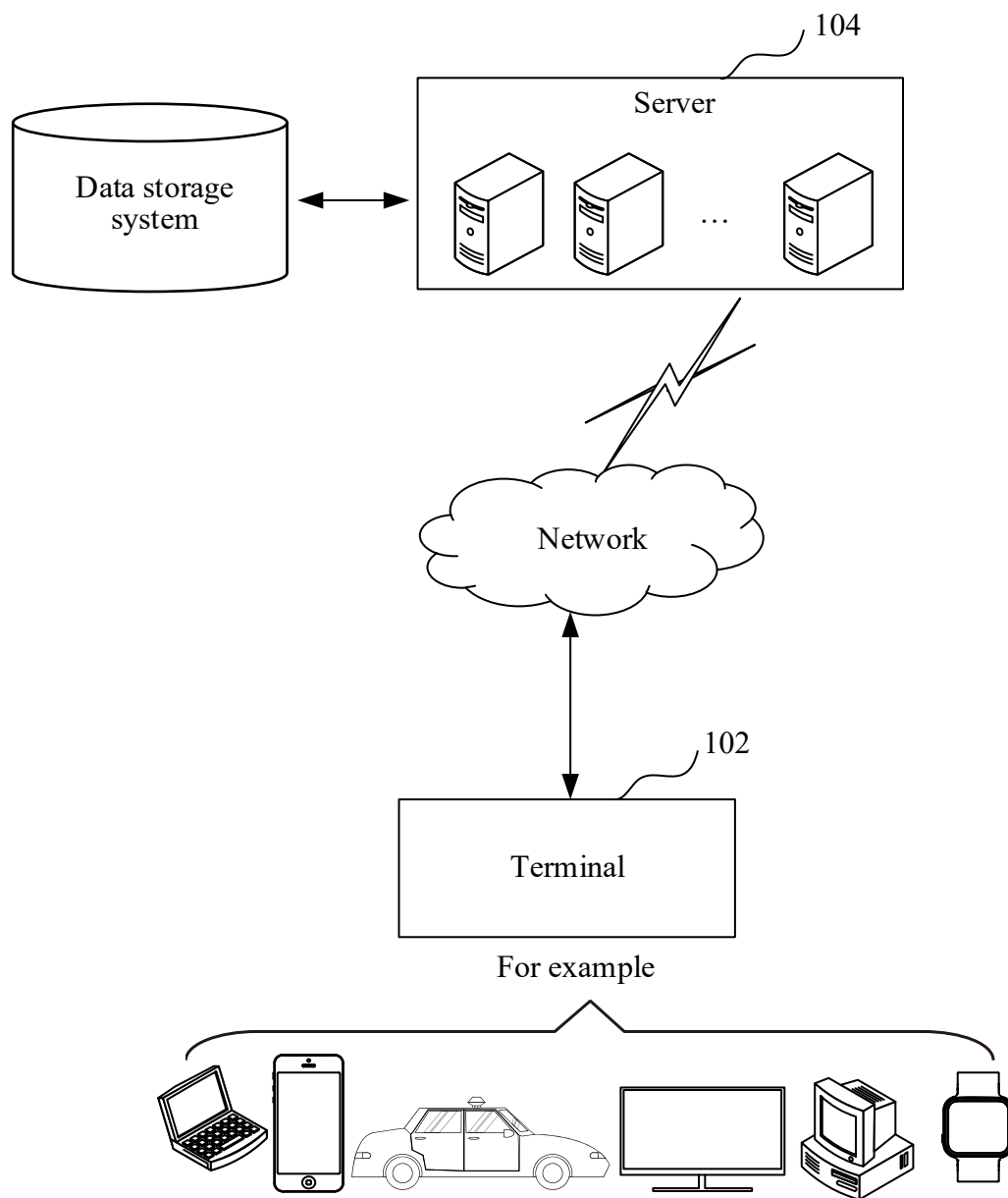


FIG. 1

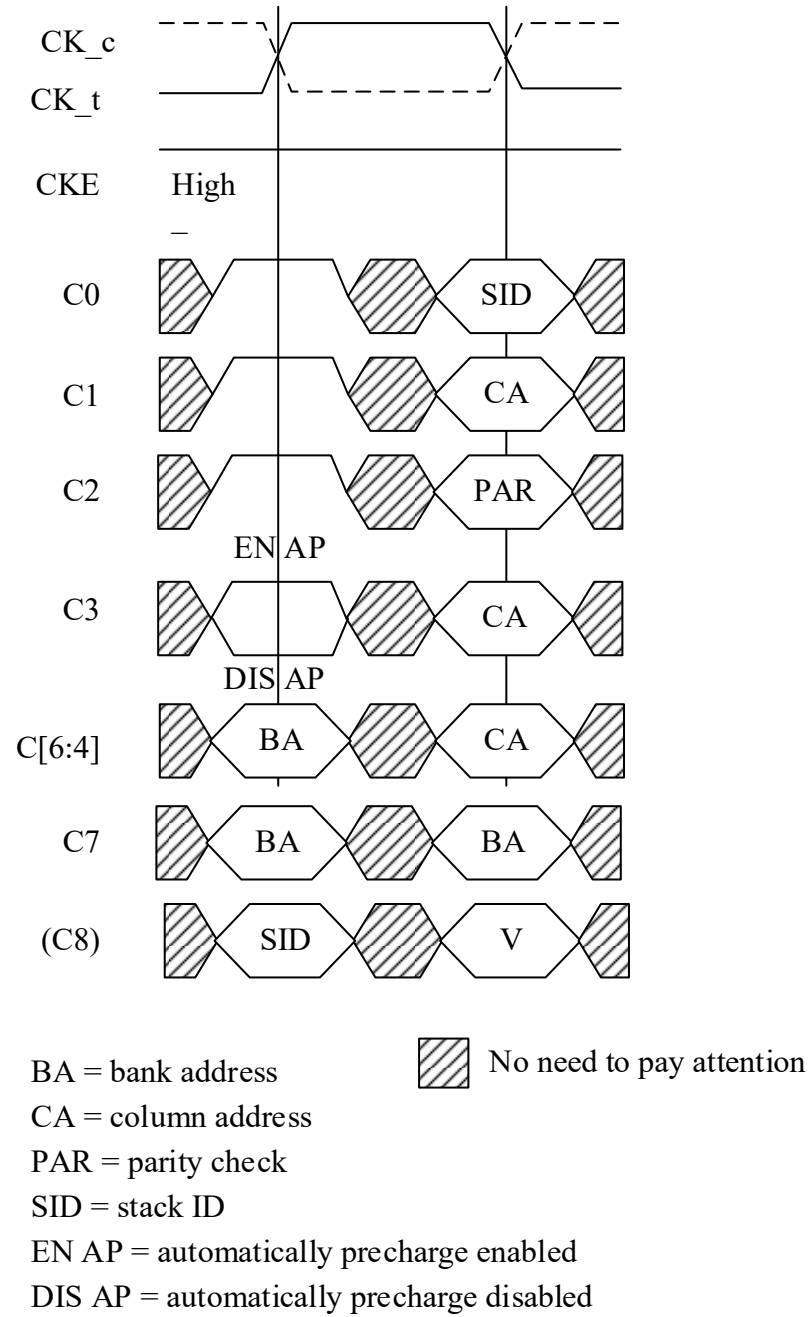
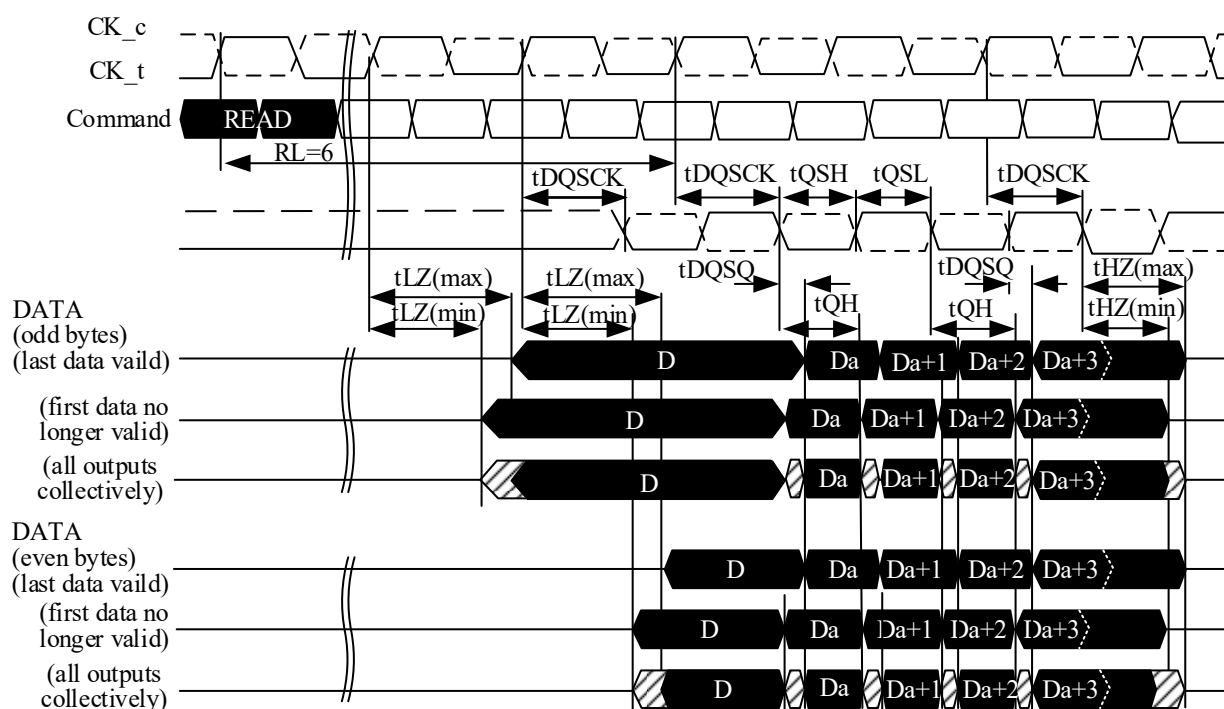


FIG. 2



1. $tDQSK$ may span multiple clock periods.

2. A burst length of 4 is shown.

3. Early/Late data transition of a DQ or DBI can vary within a burst.

4. $D_a, a+1, a+2, a+3 = \text{data-out for READ command } a$.

$D = \text{last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read)}$.

No need to pay attention

FIG. 3

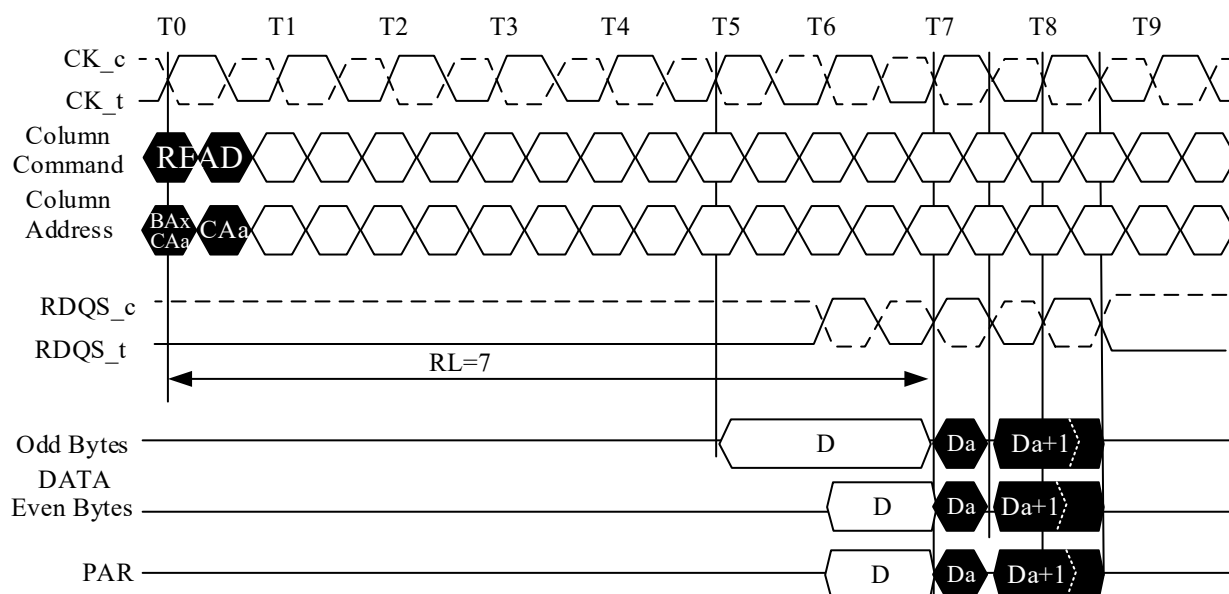


FIG. 4

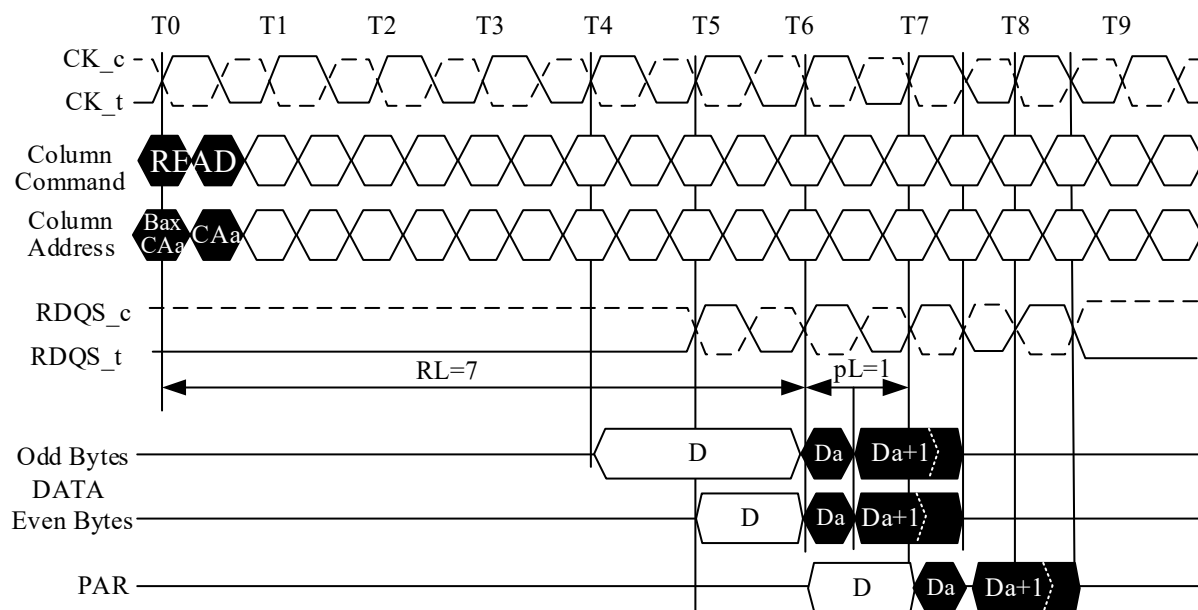


FIG. 5

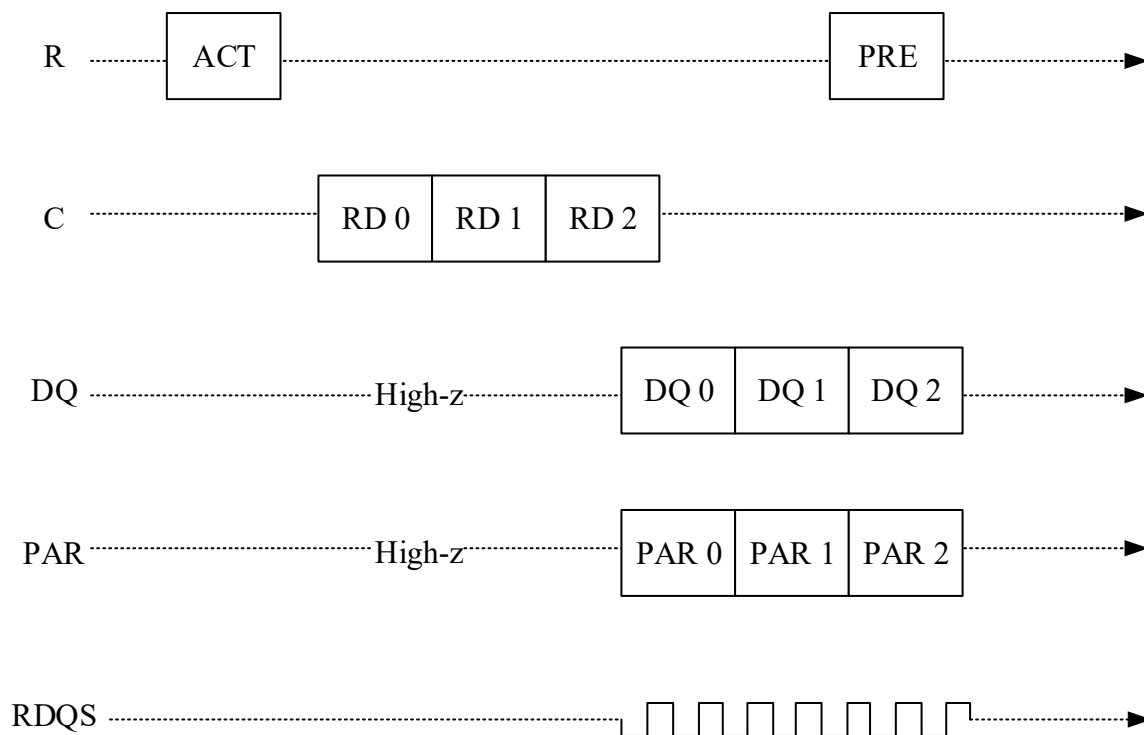


FIG. 6

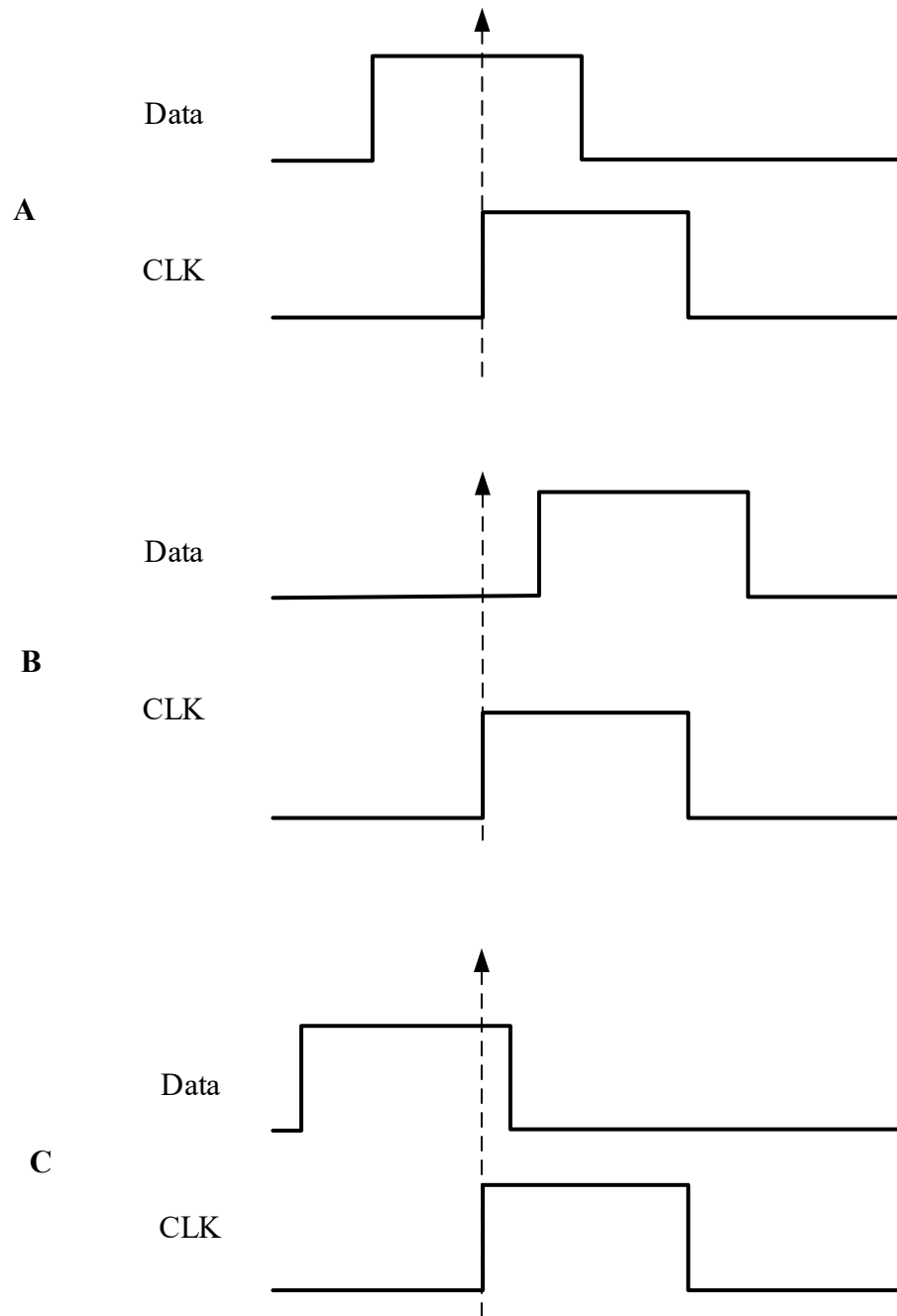


FIG. 7

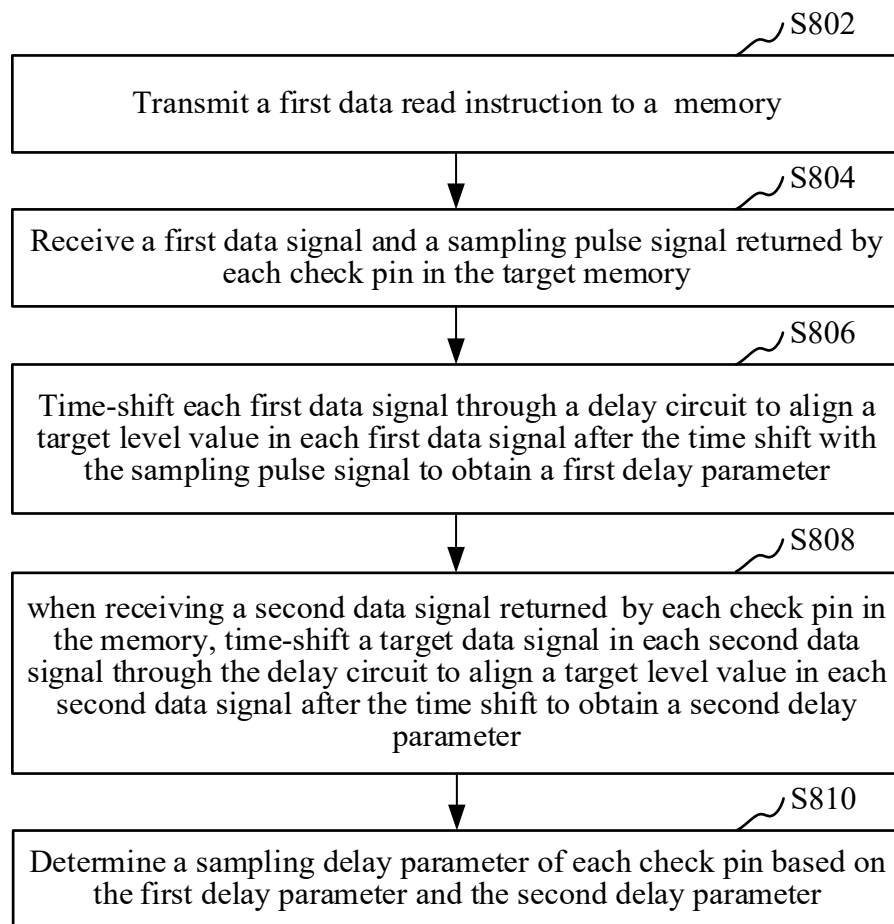


FIG. 8

Mode register 7 (MR7)

Field	Bit	Function description
CATTRIP	OP7	0 - Clear CATTRIP pin (default) 1 - Assert the CATTRIP pin to "1"
Reserved word	OP6	0
DWORD MISR control	OP[5:3]	Only valid when a loopback function is enabled under OP0 000 - Preset value MISR/lfsr of DWORD is 0xAAAAh, and LFSR_COMPARE_STICKY bits of DWORD are all set to 0. 001 - LFSR mode (read direction) 010 - Register mode (read and write instructions) DWORD write is captured directly into a MISR register without compression. The MISR register will include the most recent write data. 011 - MISR mode (write direction) 100 - LFSR compare mode (write direction)
DWORD read multiplex control	OP[2:1]	Only valid when a loopback function is enabled under OP0 00 - Reserved word 01 - Reply data from the MISR register (default) 10 - Reply data from an Rx path sampler 11 - Reply LFSR COMPARE STICKY (optional)
DWORD loopback	OP0	0 - Disabled (default) 1 - Enabled; supporting a link test circuit All write and read come to/from MISR (No additional activation required for write/read - column addresses are ignored in this mode)

FIG. 9

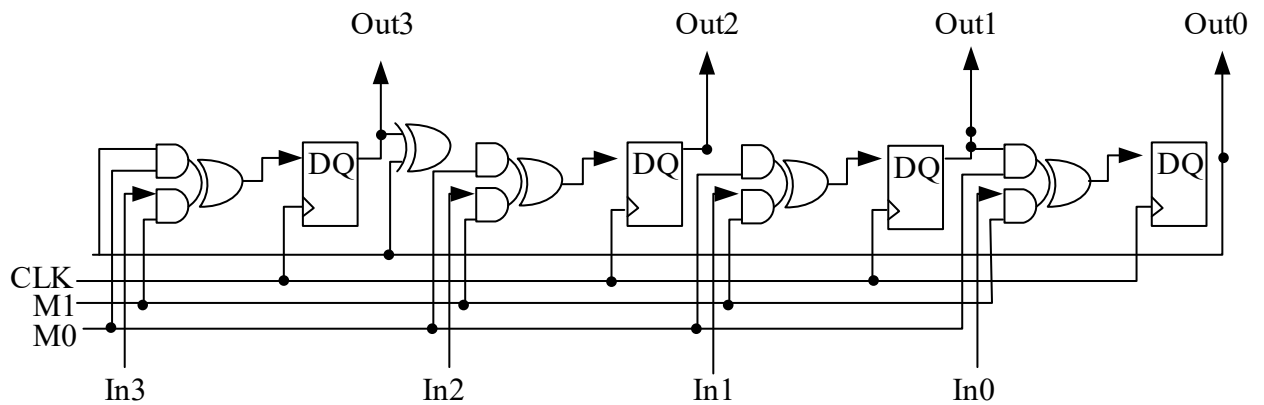


FIG. 10

Mode register 0 (MR0)

Field	Bit	Function description
Test mode	OP7	0 - Normal operation (default) 1 - Test mode (vendor specific)
Address, instruction bus, and row and column bus parity check	OP6	0 - Disabled (default) 1 - Enabled
DQ bus write parity check	OP5	0 - Disabled (default) 1 - Enabled
DQ bus read parity check	OP4	0 - Disabled (default) 1 - Enabled
Reserved word	OP3	0
Temperature compensated self-refresh (TCSR)	OP2	0 - Disabled 1 - Enabled (default)
Write DBIac	OP1	0 - Disabled 1 - Enabled (default)
Read DBIac	OP0	0 - Disabled 1 - Enabled (default)

FIG. 11

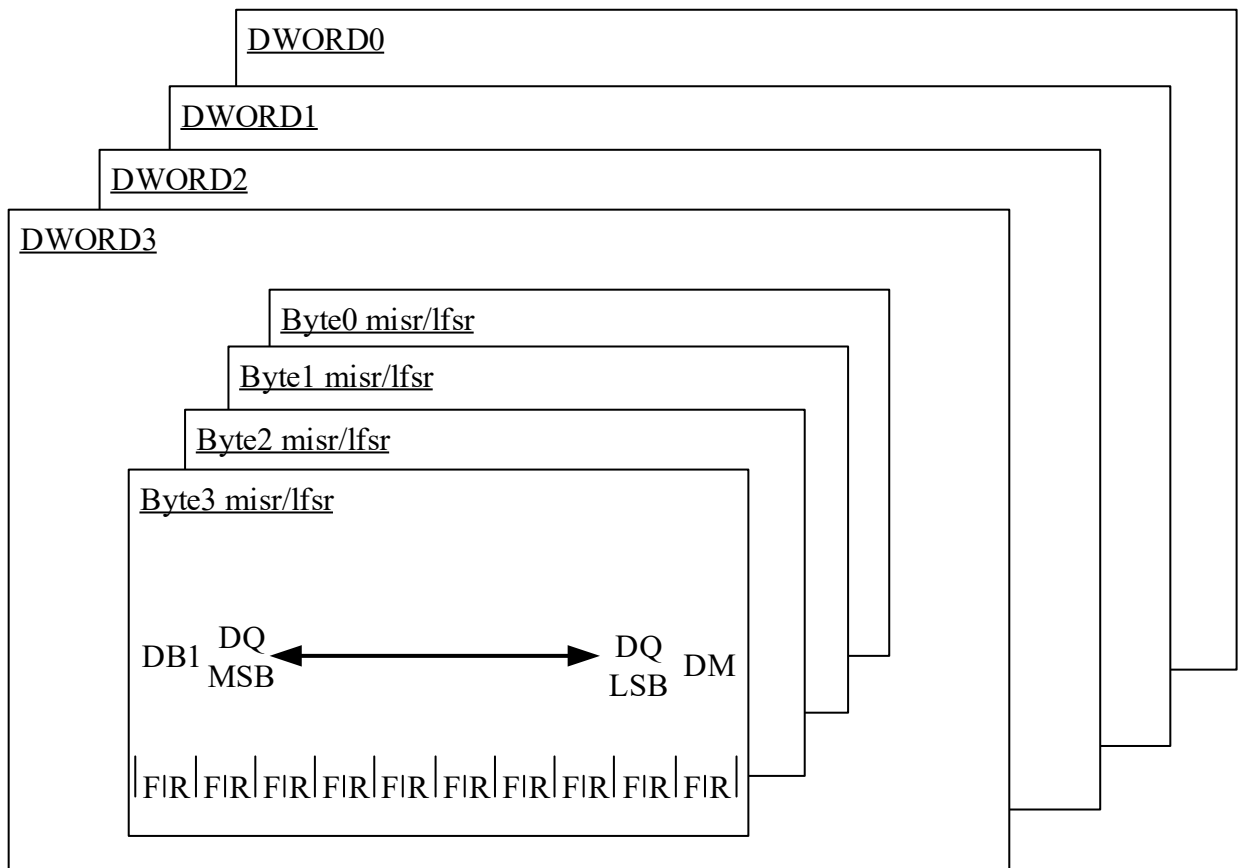


FIG. 12

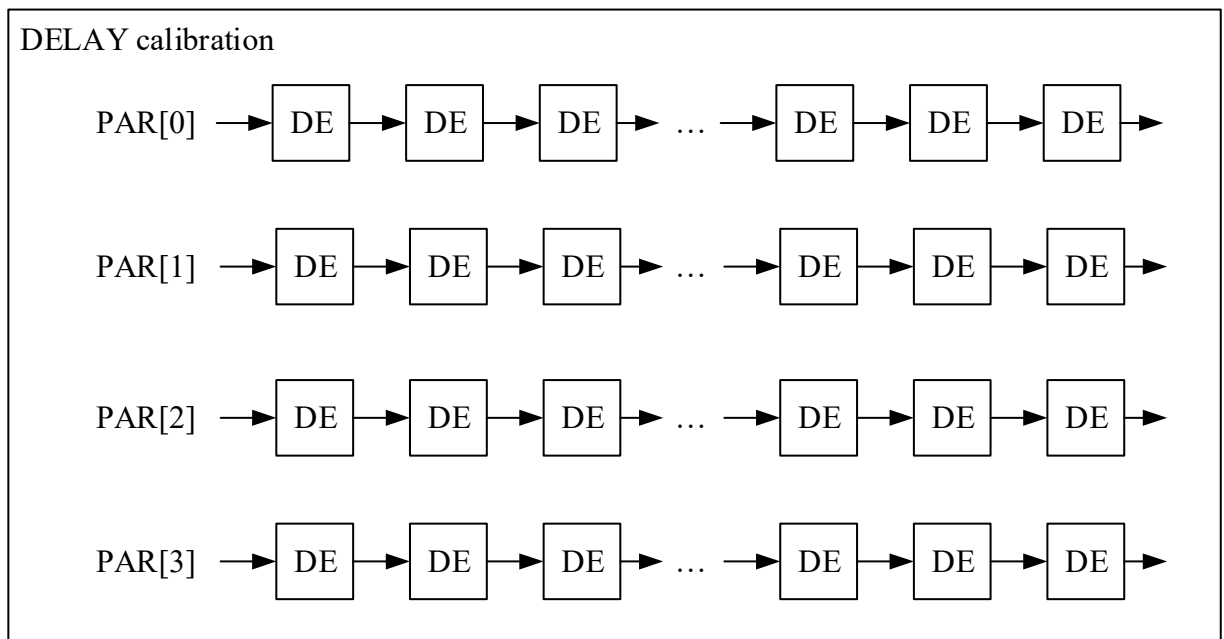


FIG. 13

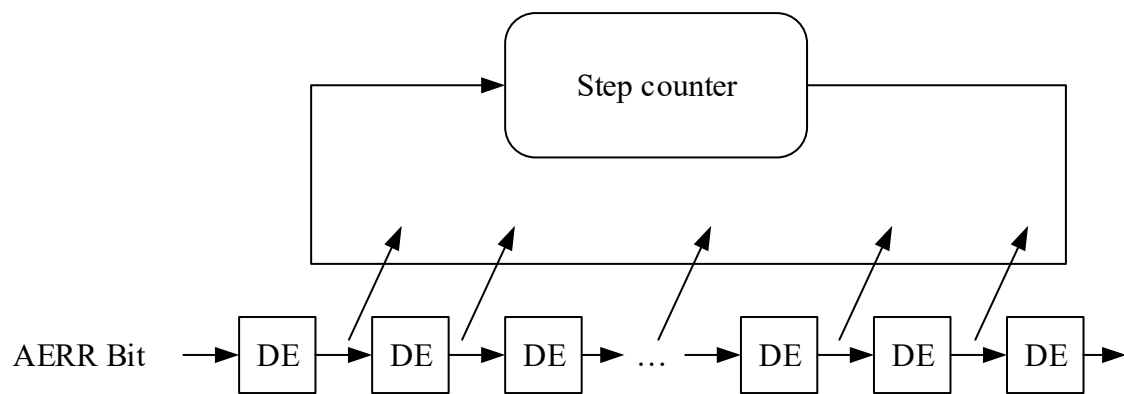


FIG. 14

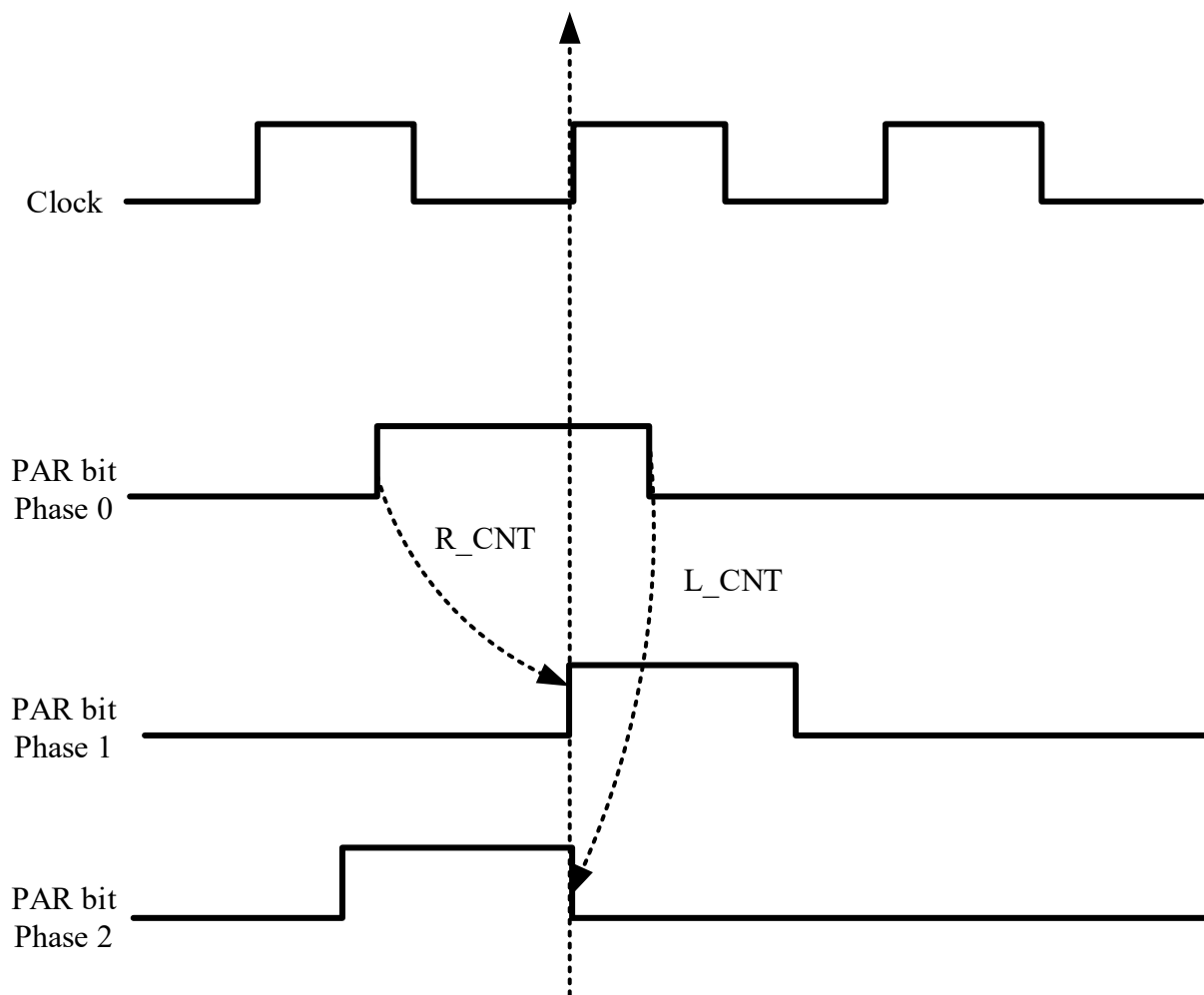


FIG. 15

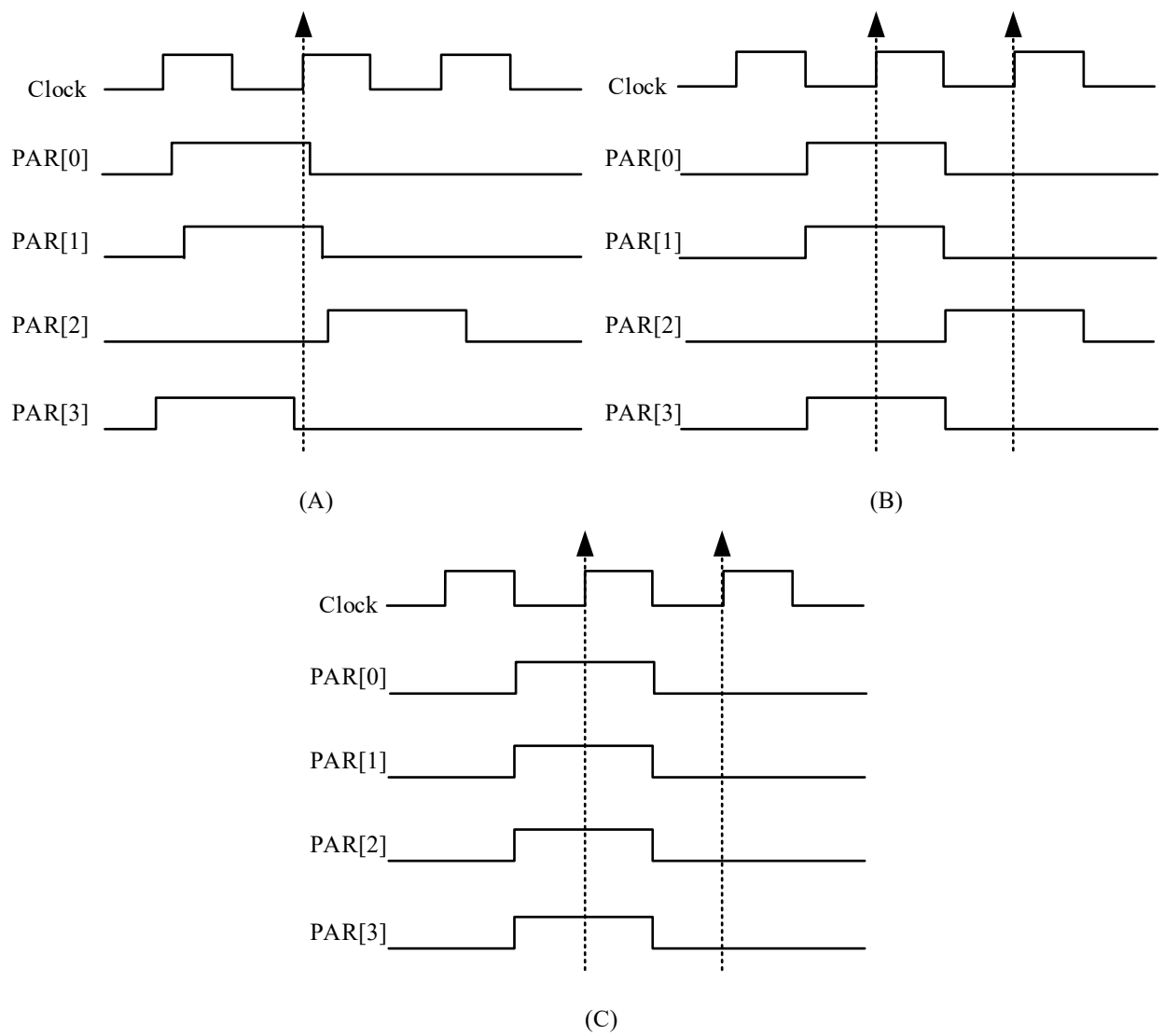


FIG. 16

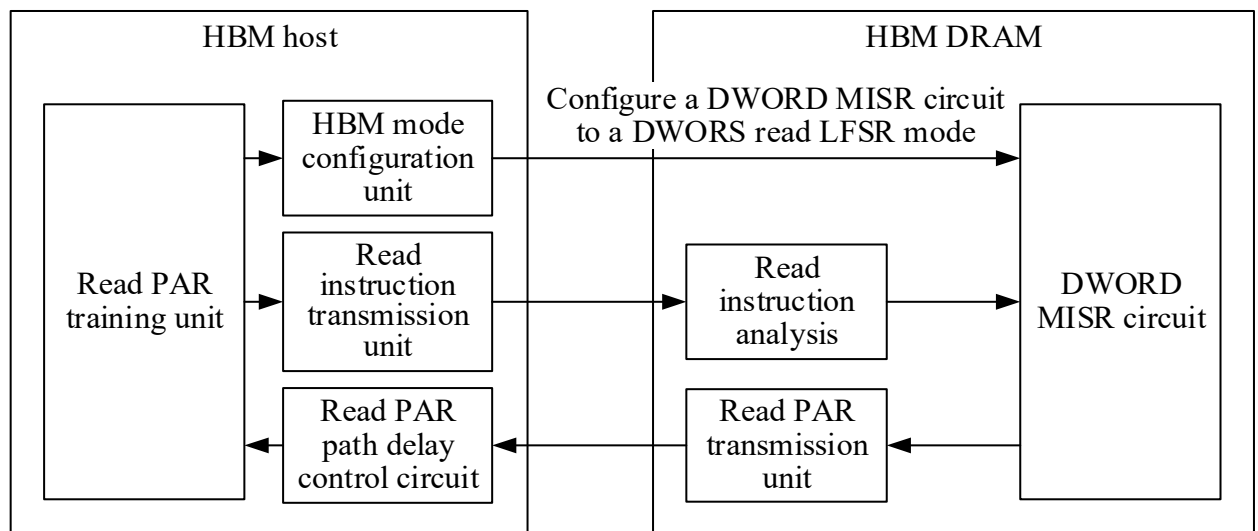


FIG. 17

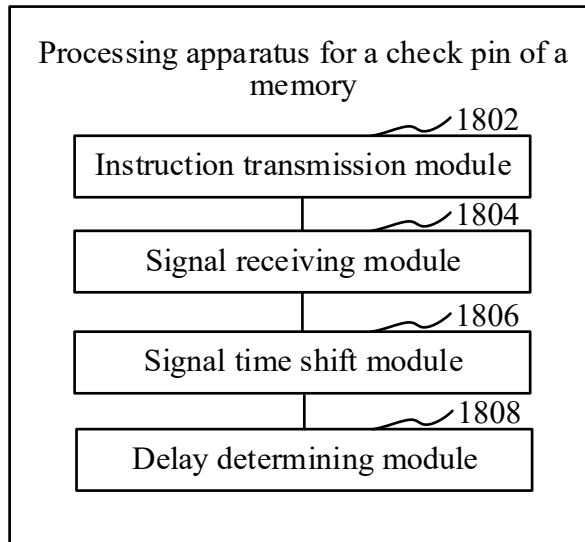


FIG. 18

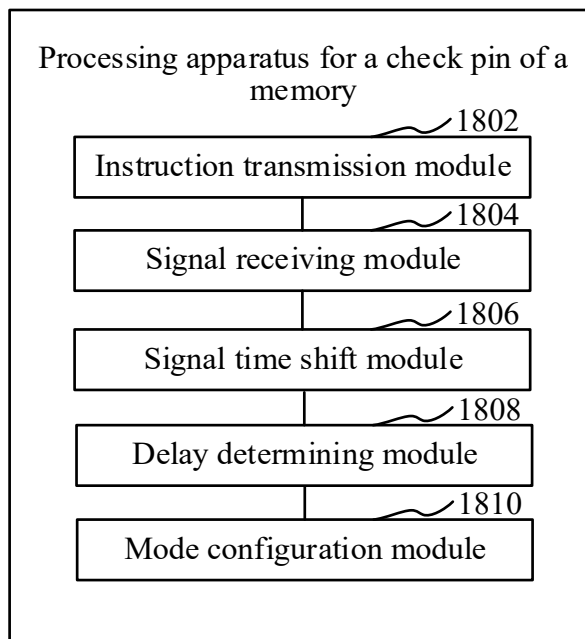


FIG. 19

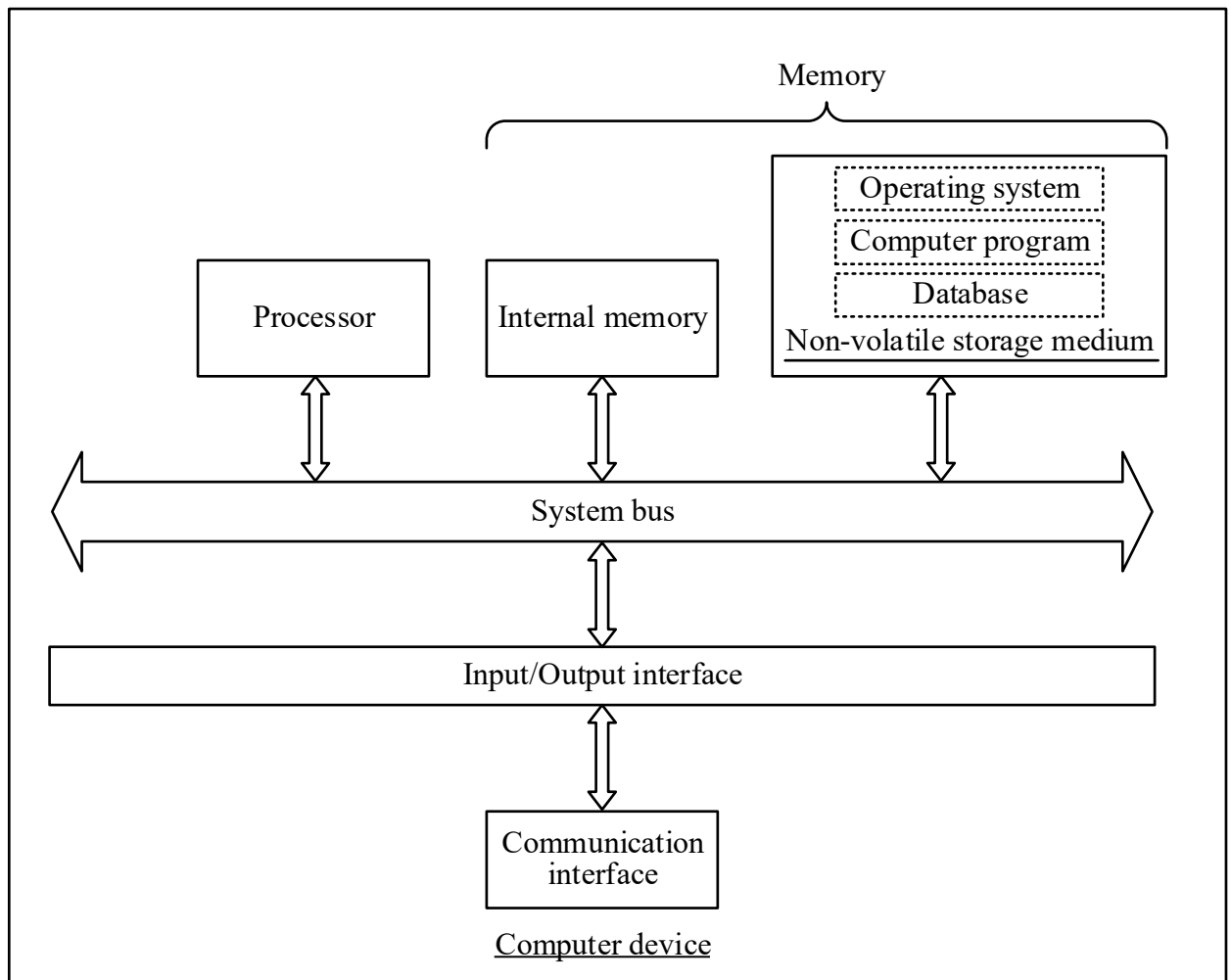


FIG. 20

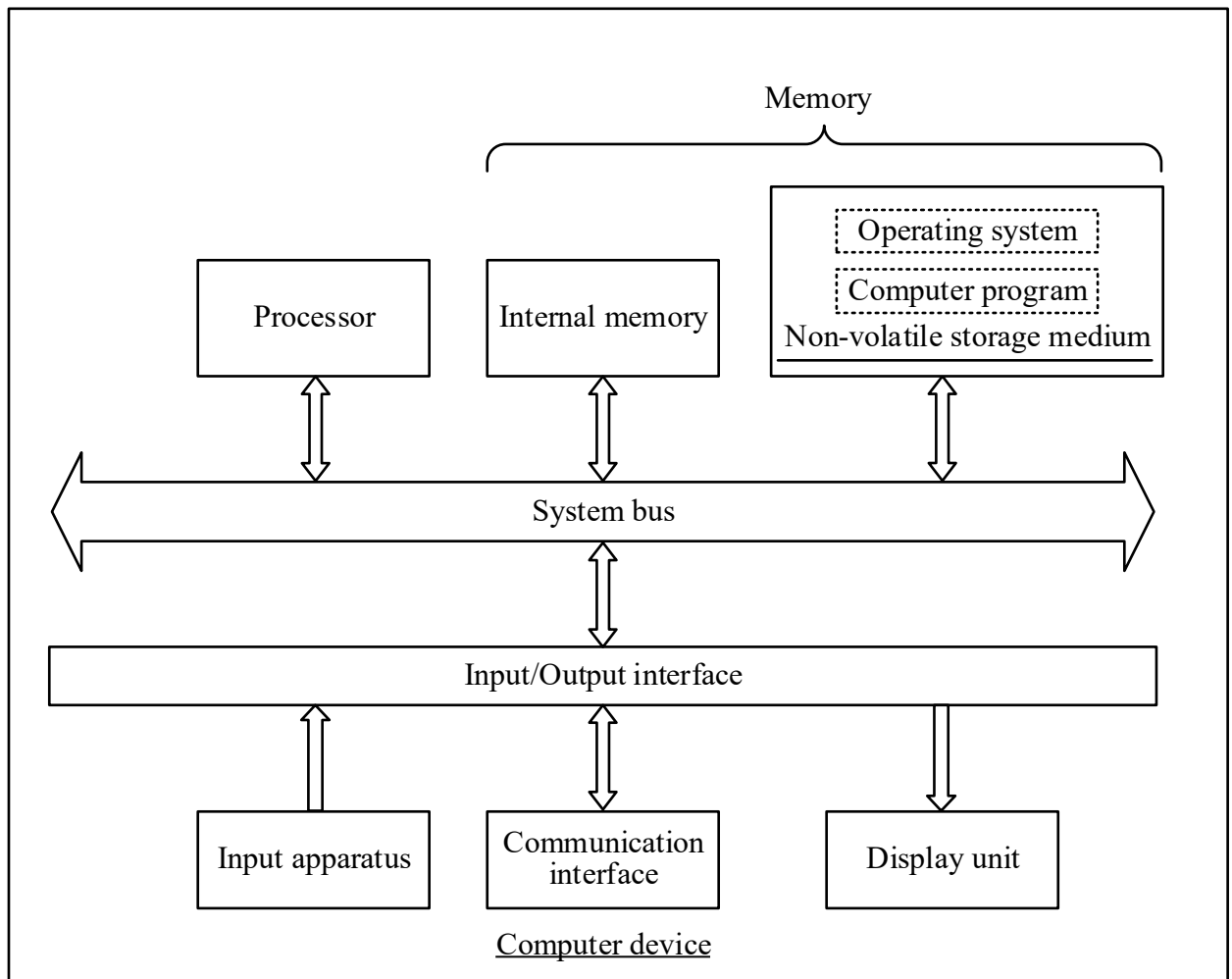


FIG. 21