CLAIMS

1. A data sampling circuit, comprising:

a first sampling module connected to a data signal terminal, a reference signal terminal, a first node, and a second node, wherein the first sampling module is configured to respond to a signal from the data signal terminal and a signal from the reference signal terminal and to act on the first node and the second node;

a second sampling module connected to the first node, the second node, a third node, and a fourth node, wherein the second sampling module is configured to respond to a signal from the first node and a signal from the second node and to act on the third node and the fourth node;

a latch module connected to the third node, the fourth node, a first output terminal, and a second output terminal, wherein the latch module is configured to, according to a signal from the third node and a signal from the fourth node, input a high level signal to the first output terminal and input a low level signal to the second output terminal, or input the low level signal to the first output terminal and input the high level signal to the second output terminal; and

a decision feedback equalization module connected in parallel to the second sampling module and configured to reduce intersymbol interference;

characterized in that the decision feedback equalization module is connected to the third node, the fourth node, a first control signal terminal and a second control signal terminal, and is configured to respond to signals from the first control signal terminal and the second control signal terminal and to act on the third node and the fourth node.

2. The data sampling circuit according to claim 1, further comprising:

an offset compensation module connected in parallel to the second sampling module and configured to compensate for an offset voltage of the second sampling module.

3. The data sampling circuit according to claim 1, wherein

the first sampling module is further connected to a first clock signal terminal and is configured to start a sampling action in response to a signal from the first clock signal terminal;

wherein the data sampling circuit further comprises:

a reset module connected to the first clock signal terminal, a second clock signal terminal, the first node, the second node, the third node, the fourth node, the first output terminal, and the second output terminal, wherein the reset module is configured to reset the first node and the second node in response to the signal from the first clock signal terminal, and to reset the third node, the fourth node, the first output terminal and the second output terminal in response to a signal from the second clock signal terminal.

4. The data sampling circuit according to claim 1, wherein the first sampling module comprises:

a first P-type transistor, a first terminal of the first P-type transistor being connected to a high-level signal terminal, a control terminal of the first P-type transistor being connected to a first clock signal terminal, and a second terminal of the first P-type transistor being connected to a fifth node;

a second P-type transistor, a first terminal of the second P-type transistor being connected to the second terminal of the first P-type transistor, a control terminal of the second P-type transistor being connected to the data signal terminal, and a second terminal the second P-type transistor being connected to the second node; and

a third P-type transistor, a first terminal of the third P-type transistor being connected to the second terminal of the first P-type transistor, a control terminal of the third P-type transistor being connected to the reference signal terminal, and a second terminal of the third P-type transistor being connected to the first node.

5. The data sampling circuit according to claim 2, wherein the second sampling module comprises:

a fourth N-type transistor, a first terminal of the fourth N-type transistor being connected to a low-level signal terminal, a control terminal of the fourth N-type transistor being connected to the second node, and a second terminal of the fourth N-type transistor being connected to the third node; and

a fifth N-type transistor, a first terminal of the fifth N-type transistor being connected to the low-level signal terminal, a control terminal of the fifth N-type transistor being

connected to the first node, and a second terminal of the fifth N-type transistor being connected to the fourth node.

6. The data sampling circuit according to claim 1, wherein the latch module comprises:

a sixth P-type transistor, a first terminal of the sixth P-type transistor being connected to a high-level signal terminal, a control terminal of the sixth P-type transistor being connected to the second output terminal, and a second terminal of the sixth P-type transistor being connected to the first output terminal;

a seventh N-type transistor, a first terminal of the seventh N-type transistor being connected to the third node, a second terminal of the seventh N-type transistor being connected to the first output terminal, and a control terminal of the seventh N-type transistor being connected to the second output terminal;

an eighth P-type transistor, a first terminal of the eighth P-type transistor being connected to the high-level signal terminal, a control terminal of the eighth P-type transistor being connected to the first output terminal, and a second terminal of the eighth P-type transistor being connected to the second output terminal; and

a ninth N-type transistor, a first terminal of the ninth N-type transistor being connected to the fourth node, a second terminal of the ninth N-type transistor being connected to the second output terminal, and a control terminal of the ninth N-type transistor being connected to the first output terminal.

7. The data sampling circuit according to claim 5, wherein the decision feedback equalization module comprises:

a first decision feedback equalization module, connected in parallel between a source terminal of the fourth N-type transistor and a drain terminal of the fourth N-type transistor and configured to compensate for a parameter of the fourth N-type transistor; and

a second decision feedback equalization module, connected in parallel between a source terminal of the fifth N-type transistor and a drain terminal of the fifth N-type transistor and configured to compensate for a parameter of the fifth N-type transistor;

wherein the first decision feedback equalization module and the second decision feedback equalization module are controlled by two signals inverse to each other and are

driven by one of the two signals.

8. The data sampling circuit according to claim 7, wherein the first decision feedback equalization module comprises:

a plurality of tenth N-type transistors, a first terminal of each of the plurality of tenth N-type transistors being connected to the third node, and a control terminal of each of the plurality of tenth N-type transistors being connected to the second node;

a plurality of eleventh transistors arranged in one-to-one correspondence with the plurality of tenth N-type transistors, a first terminal of each of the plurality of eleventh transistors being connected to a second terminal of each of the plurality of tenth N-type transistors, and a control terminal of each of the plurality of eleventh transistors being respectively connected to a different control signal terminal; and

a plurality of twelfth N-type transistors arranged in one-to-one correspondence with the plurality of eleventh transistors, a first terminal of each of the plurality of twelfth N-type transistors being connected to a second terminal of each of the plurality of eleventh transistors, a control terminal of each of the plurality of twelfth N-type transistors being connected to the first control signal terminal, and a second terminal of each of the plurality of twelfth N-type transistors being connected to the low-level signal terminal.

9. The data sampling circuit according to claim 8, wherein the second decision feedback equalization module comprises:

a plurality of thirteenth N-type transistors, a first terminal of each of the plurality of thirteenth N-type transistors being connected to the fourth node, and a control terminal of each of the plurality of thirteenth N-type transistors being connected to the first node;

a plurality of fourteenth transistors arranged in one-to-one correspondence with the plurality of thirteenth N-type transistors, a first terminal of each of the plurality of fourteenth transistors being connected to a second terminal of each of the plurality of thirteenth N-type transistors, and a control terminal of each of the plurality of fourteenth transistors being respectively connected to a different control signal terminal; and

a plurality of fifteenth N-type transistors arranged in one-to-one correspondence with the plurality of fourteenth transistors, a first terminal of each of the plurality of fifteenth

N-type transistors being connected to a second terminal of each of the plurality of fourteenth transistors, a control terminal of each of the plurality of fifteenth N-type transistors being connected to the second control signal terminal, and a second terminal of each of the plurality of fifteenth N-type transistors being connected to the low-level signal terminal;

wherein a signal from the first control signal terminal and a signal from the second control signal terminal are inverse to each other.

10. The data sampling circuit according to claim 8, wherein a number of the plurality of tenth N-type transistors, a number of the plurality of eleventh transistors and a number of the plurality of twelfth N-type transistors are two, respectively.

11. The data sampling circuit according to claim 9, wherein a number of the plurality of thirteenth N-type transistors, a number of the plurality of fourteenth transistors and a number of the plurality of fifteenth N-type transistors are two, respectively.

12. The data sampling circuit according to claim 5, wherein the offset compensation module comprises:

a first offset compensation module, connected in parallel between a source terminal of the fourth N-type transistor and a drain terminal of the fourth N-type transistor and configured to compensate for a parameter of the fourth N-type transistor; and

a second offset compensation module, connected in parallel between a source terminal of the fifth N-type transistor and a drain terminal of the fifth N-type transistor and configured to compensate for a parameter of the fifth N-type transistor.

13. The data sampling circuit according to claim 12, wherein the first offset compensation module comprises:

a plurality of sixteenth transistors, a first terminal of each of the plurality of sixteenth transistors being connected to the low-level signal terminal, and a control terminal of each of the plurality of sixteenth transistors being respectively connected to a different control signal terminal; and

a plurality of first capacitors arranged in one-to-one correspondence with the plurality

of sixteenth transistors, each of the plurality of first capacitors being connected between a second terminal of each of the plurality of sixteenth transistors and the third node.

14. The data sampling circuit according to claim 12, wherein the second offset compensation module comprises:

a plurality of seventeenth transistors, a first terminal of each of the plurality of seventeenth transistors being connected to the low-level signal terminal, and a control terminal of each of the plurality of seventeenth transistors being respectively connected to a different control signal terminal; and

a plurality of second capacitors arranged in one-to-one correspondence with the plurality of seventeenth transistors, wherein each of the plurality of second capacitors is connected between a second terminal of each of the plurality of seventeenth transistors and the third node.

15. The data sampling circuit according to claim 3, wherein the reset module comprises:

an eighteenth N-type transistor, a first terminal of the eighteenth N-type transistor being connected to a low-level signal terminal, a second terminal of the eighteenth N-type transistor being connected to the second node, and a control terminal of the eighteenth N-type transistor being connected to the first clock signal terminal;

a nineteenth N-type transistor, a first terminal of the nineteenth N-type transistor being connected to the low-level signal terminal, a second terminal of the nineteenth N-type transistor being connected to the first node, and a control terminal of the nineteenth N-type transistor being connected to the first clock signal terminal;

a twentieth P-type transistor, a first terminal of the twentieth P-type transistor being connected to a high-level signal terminal, a second terminal of the twentieth P-type transistor being connected to the third node, and a control terminal of the twentieth P-type transistor being connected to the second clock signal terminal;

a twenty-first P-type transistor, a first terminal of the twenty-first P-type transistor being connected to the high-level signal terminal, a second terminal of the twenty-first P-type transistor being connected to the first output terminal, and a control terminal of the

twenty-first P-type transistor being connected to the second clock signal terminal;

a twenty-second P-type transistor, a first terminal of the twenty-second P-type transistor being connected to the high-level signal terminal, a second terminal of the twenty-second P-type transistor being connected to the second output terminal, and a control terminal of the twenty-second P-type transistor being connected to the second clock signal terminal; and

a twenty-third P-type transistor, a first terminal of the twenty-third P-type transistor being connected to the high-level signal terminal, a second terminal of the twenty-third P-type transistor being connected to the fourth node, and a control terminal of the twenty-third P-type transistor being connected to the second clock signal terminal.

16. A data sampling device, comprising a plurality of cascaded data sampling circuits according to any of claims 1 to 15, wherein a first output terminal of a given one of the plurality of data sampling circuits at a previous stage is connected to a first control terminal of an adjacent one of the plurality of data sampling circuits at a next stage, and a second output terminal of the data sampling circuit at the previous stage being connected to a second control terminal of the adjacent data sampling circuit at the next stage;

wherein a first output terminal of the data sampling circuit at a last stage is connected to a first control terminal of the data sampling circuit at a first stage, and a second output terminal of the data sampling circuit at the last stage being connected to a second control terminal of the data sampling circuit at the first stage.

17. The data sampling device according to claim 16, further comprising a plurality of latches, the plurality of latches being arranged in one-to-one correspondence with the plurality of data sampling circuits, wherein the plurality of latches are configured to latch data from the first output terminals of the plurality of data sampling circuits at a third output terminal, and latch data from the second output terminals of the plurality of data sampling circuits at a fourth output terminal.

18. The data sampling device according to claim 17, wherein each of the plurality of latches comprises:

a twenty-fourth P-type transistor, a first terminal of the twenty-fourth P-type transistor

being connected to a high-level signal terminal, a second terminal of the twenty-fourth P-type transistor being connected to the third output terminal, and a control terminal of the twenty-fourth P-type transistor being connected to the first output terminal of each of the plurality of data sampling circuits;

a twenty-fifth P-type transistor, a first terminal of the twenty-fifth P-type transistor being connected to the high-level signal terminal, a second terminal of the twenty-fifth P-type transistor being connected to the third output terminal, and a control terminal of the twenty-fifth P-type transistor being connected to the fourth output terminal;

a twenty-sixth P-type transistor, a first terminal of the twenty-sixth P-type transistor being connected to the high-level signal terminal, a second terminal of the twenty-sixth P-type transistor being connected to the fourth output terminal, and a control terminal of the twenty-sixth P-type transistor being connected to the third output terminal;

a twenty-seventh P-type transistor, a first terminal of the twenty-seventh P-type transistor being connected to the high-level signal terminal, a second terminal of the twenty-seventh P-type transistor being connected to the fourth output terminal, and a control terminal of the twenty-seventh P-type transistor being connected to the second output terminal of each of the plurality of data sampling circuits;

a twenty-eighth N-type transistor, a first terminal of the twenty-eighth N-type transistor being connected to a low-level signal terminal, a second terminal of the twenty-eighth N-type transistor being connected to the third output terminal, and a control terminal of the twenty-eighth N-type transistor being connected to the first output terminal of each of the plurality of data sampling circuits;

a twenty-ninth N-type transistor, a first terminal of the twenty-ninth N-type transistor being connected to the low-level signal terminal, a second terminal of the twenty-ninth N-type transistor being connected to the third output terminal, and a control terminal of the twenty-ninth N-type transistor being connected to the fourth output terminal;

a thirtieth N-type transistor, a first terminal of the thirtieth N-type transistor being connected to the low-level signal terminal, a second terminal of the thirtieth N-type transistor being connected to the fourth output terminal, and a control terminal of the thirtieth N-type transistor being connected to the third output terminal; and

a thirty-first N-type transistor, a first terminal of the thirty-first N-type transistor being

connected to the low-level signal terminal, a second terminal of the thirty-first N-type transistor being connected to the fourth output terminal, and a control terminal of the thirty-first N-type transistor being connected to the second output terminal of each of the plurality of data sampling circuits.

19. The data sampling device according to claim 16, wherein the data sampling device comprises four data sampling circuits, the data sampling device further comprising:

a clock circuit, configured to provide clock sampling signals to first clock signal terminals of the four data sampling circuits, wherein a phase difference between the clock sampling signals on the first clock signal terminals of the adjacent data sampling circuits is 90 degrees, and a period of each of the clock sampling signals on the first clock signal terminals being twice that of a signal on a data signal terminal.