What is claimed is:

1. An electrocardiogram signal processing system comprising:

a wavelet transformation unit comprising a plurality of outputs, each output being connected to one of a plurality of scales, wherein the wavelet transformation unit is adapted to transform an input electrocardiogram signal into a set of wavelets, each wavelet being output to one of the scales;

a plurality of signal processing blocks, each of the signal processing blocks coupled to a respective output of the wavelet transformation unit and configured to receive and process the wavelet from the respective output, wherein the signal processing blocks provide processing functions which differ from one another;

wherein the scales comprise a first scale, a second scale, a third scale, a fourth scale, a fifth scale, a sixth scale, a seventh scale, and an eighth scale;

wherein each scale corresponds to a pre-determined band-width;

wherein the signal processing blocks comprise an electrocardiogram signal reconstruction block;

wherein the electrocardiogram signal reconstruction block further comprises:

a first reconstruction block for the fifth to the eighth scales;

a second reconstruction block for the first to the fourth scales; and

a third reconstruction block for the first to the eighth scales;

wherein the first reconstruction block outputs synchronized signals belonging to high-pass filtered components of the fifth to the eighth scales; the second reconstruction block outputs synchronized signals belonging to high-pass filtered components of the first to the fourth scales; and the third reconstruction block outputs signals belonging to low-pass filtered components of the first to the seventh scales.

2. The system of claim 1, wherein each scale has a different bandwidth, wherein the wavelet output to one of the scales is derived from the wavelet output to an earlier scale.

3. The system of claim 2, wherein the number of scales is at least eight, the scales having 3 dB bandwidths of around 250 to 500 Hz; 72 to 234 Hz; 32 to 108 Hz; 16 to 54 Hz; 8 to 26 Hz; 4 to 13 Hz; 2 to 6.5 Hz; and 1 to 3.25 Hz for the first to the eighth scales respectively, when the sampling rate of the input signal is 1 kHz.

4. The system of claim 1, wherein the wavelet transformation unit comprises a plurality of low pass filters and a plurality of high pass filters.

5. The system of claim 4, wherein the low pass filter for the first scale is given by the expression

$$l_{D,1}(k)=\frac{1}{8}\{\delta(k+2)+3\delta(k+1)+3\delta(k)+\delta(k-1)\}$$

and the high pass filter for the first scale is given by the expression

$$h_{D,1}(k)=2\{\delta(k+1)-\delta(k)\},$$

wherein δ(k) is the Kronecker delta function and for scale numbers n>1, $l_{D,n}(k)$ and $h_{D,n}(k)$ are obtained by inserting $2^{n-1}-1$ zeros between each of the non-zero coefficients of $l_{D,1}(k)$ and $h_{D,1}(k)$.

6. The system of claim 4, wherein the low pass filters and the high pass filters have a cascaded arrangement, wherein an output of at least one of the low pass filters is coupled to an input of at least one of the high pass filters.

7. The system of claim 4, wherein the wavelet transformation unit comprises a first memory array to achieve delay, the first memory array coupled to the last low pass filter of the cascaded chain of high pass filters and low pass filters.

8. The system of claim 1, wherein the signal processing blocks comprise at least one wavelet denoising unit to suppress high frequency noise.

9. The system of claim 8, wherein each of the at least one wavelet denoising unit is coupled to one of the respective outputs of the wavelet transforming unit emitting wavelets coupled to the first three scales and wherein the suppressed high frequency noise falls in a range of above 32 Hz.

10. The system of claim 8, wherein the signal processing blocks comprise a QRS detection unit, the QRS detection unit coupled to the output of the at least one wavelet denoising unit and the output of the wavelet transforming unit emitting wavelets belonging to the fourth scale.

11. The system of claim 10, wherein the QRS detection unit comprises a wavelet summation unit to sum the denoised wavelets from the at least one wavelet denoising unit and the wavelets from the wavelet transforming unit, wherein QRS peaks are detected when the summed wavelets exceed an adaptive threshold value.

12. The system of claim 11 wherein the QRS detection unit is realized using any of a Field Programmable Gate Array (FPGA), Application Specific Integrated Circuits (ASIC) or software implemented; the wavelet summation unit comprising an adder; and the QRS peaks are detected using a subtractor and multiplexer.

13. The system of claim 11, wherein the adaptive threshold value is derived from a standard deviation of a number of sampled summed wavelets.

14. The system of claim 10, further comprising a heart beat rate (HBR) analysis unit, the HBR analysis unit coupled to an output of the QRS detection unit.

15. The system of claim 14, wherein the HBR analysis unit comprises a counter; two multiplication blocks; an adder and a delay block, wherein the HBR analysis unit is realized by a Field Programmable Gate Array (FPGA), Application Specific Integrated Circuits (ASIC) or software implemented.

16. The system of claim 14, wherein the HBR analysis unit is adapted to predict QRS peak intervals based on a forward prediction algorithm.

17. The system of claim 14, wherein the forward prediction algorithm is based on summing previous QRS peak intervals weighted with a forgetting factor, the forgetting factor determining the number of previous QRS peak intervals included for HBR analysis.

18. The system of claim 1, wherein the first reconstruction block, the second reconstruction block and the third reconstruction block comprise shift registers to achieve delay.

19. The system of claim 1, wherein the first reconstruction block, the second reconstruction block and the third reconstruction block comprise memory arrays to achieve delay for both filtering and synchronization.

20. The system of claim 19, wherein SRAM is used for the memory arrays.

21. The system of claim 1, wherein the output of the first to the third reconstruction blocks is a reconstructed electrocardiogram signal.

22. The system of claim 1, wherein the electrocardiogram signal reconstruction block processes wavelets belonging to the first to the eighth scales.

23. The system of claim 1, wherein the second reconstruction block is coupled to an output of a wavelet denoising unit to receive denoised wavelets belonging to the first to the third scales.

24. The system of claim 1, the system further comprising a data compression block, the data compression block receiving wavelets of the fifth to the eighth scales, wherein an output of the data compression block is coupled to the input of the first reconstruction block.

25. The system of claim 24, wherein the data compression block is realized using finite-impulse-response filters with zeros and infinite-impulse-response filters with poles, wherein the zeros of the finite-impulse-response filters compensate the poles of the infinite-impulse-response filters.

26. The system of claim 1, wherein the signal processing blocks comprises a baseline drift removal unit, the baseline drift removal unit coupled to the respective output of the wavelet transforming unit emitting wavelets belonging to the seventh and the eighth scales.

27. The system of claim 26, wherein the baseline drift removal block is realized by an adaptive cascaded filter arrangement, the cascaded filter arrangement comprising at least one filter stage.

28. The system of claim 27, wherein the adaptive cascaded filter arrangement comprises chebyshev IIR filters.

29. The system of claim 27, wherein the adaptive cascaded filter arrangement automatically switches off filter stages unnecessary for performing baseline drift removal.

30. The system of claim 29, wherein the unnecessary filter stages are those larger than a filter stage in which the difference in the output value of the filter stage and an output value of the largest filter stage is smaller than a specified threshold.

CLAIMS

1. An electrocardiogram signal processing system comprising:

a wavelet transformation unit comprising a plurality of outputs, each output being connected to one of a plurality of scales, wherein the wavelet transformation unit is adapted to transform an input electrocardiogram signal into a set of wavelets, each wavelet being output to one of the scales;

a plurality of signal processing blocks, each of the signal processing blocks coupled to a respective output of the wavelet transformation unit and configured to receive and process the wavelet from the respective output, wherein the signal processing blocks provide processing functions which differ from one another.

2. The system of claim 1, wherein each scale has a different bandwidth, wherein the wavelet output to one of the scales is derived from the wavelet output to an earlier scale.

3. The system of claim 2, wherein the number of scales is at least eight, the scales having 3 dB bandwidths of around 250 to 500 Hz; 72 to 234 Hz; 32 to 108 Hz; 16 to 54 Hz; 8 to 26 Hz; 4 to 13 Hz; 2 to 6.5 Hz; and 1 to 3.25 Hz for the first to the eighth scales respectively, when the sampling rate of the input signal is 1 kHz.

4. The system of any one of the preceding claims, wherein the wavelet transformation unit comprises a plurality of low pass filters and a plurality of high pass filters.

5. The system of claim 4, wherein the low pass filter for the first scale is given by the expression

$$l_{D,1}(k)=\frac{1}{8}\{\delta(k+2)+3\delta(k+1)+3\delta(k)+\delta(k-1)\}$$

and the high pass filter for the first scale is given by the expression

$$h_{D,1}(k)=2\{\delta(k+1)-\delta(k)\}$$

, wherein δ(k) is the Kronecker delta function and for scale numbers $n>1$, $l_{D,n}(k)$ and $h_{D,n}(k)$ are obtained by inserting $2^{n-1}-1$ zeros between each of the non-zero coefficients of $l_{D,1}(k)$ and $h_{D,1}(k)$.

6. The system of claims 4 or 5, wherein the low pass filters and the high pass filters have a cascaded arrangement, wherein an output of at least one of the low pass filters is coupled to an input of at least one of the high pass filters.

7. The system of claims 4 to 6, wherein the wavelet transformation unit comprises a first memory array to achieve delay, the first memory array coupled to the last low pass filter of the cascaded chain of high pass filters and low pass filters.

8. The system of any one of the preceding claims, wherein the signal processing blocks comprise at least one wavelet denoising unit to suppress high frequency noise.

9. The system of claim 8, wherein each of the at least one wavelet denoising unit is coupled to one of the respective outputs of the wavelet transforming unit emitting wavelets coupled to the first three scales and wherein the suppressed high frequency noise falls in a range of above 32 Hz.

10. The system of any one of the preceding claims, wherein the signal processing blocks comprise an electrocardiogram signal reconstruction block.

11. The system of claim 10, wherein the electrocardiogram signal reconstruction block further comprises

a first reconstruction block for the fifth to the eighth scales;

a second reconstruction block for the first to the fourth scales; and

a third reconstruction block for the first to the eighth scales.

12. The system of claim 11, wherein the first reconstruction block, the second reconstruction block and the third reconstruction block comprise shift registers to achieve delay.

13. The system of claim 11, wherein the first reconstruction block, the second reconstruction block and the third reconstruction block comprise memory arrays to achieve delay.

14. The system of claim 13, wherein SRAM is used for the memory arrays.

15. The system of claims 11 to 14, wherein the first reconstruction block outputs synchronized signals belonging to the high-pass filtered components of the fifth to the eighth scales; the second reconstruction block outputs synchronized signals belonging to

the high-pass filtered components of the first to the fourth scales; and the third reconstruction block outputs signals belonging to the low-pass filtered components of the first to the seventh scales.

16. The system of claims 11 to 15, wherein the output of the first to the third reconstruction blocks is a reconstructed electrocardiogram signal.

17. The system of claims 10 to 16, wherein the electrocardiogram signal reconstruction block processes wavelets belonging to the first to the eighth scales.

18. The system of claims 11 to 17, wherein the second reconstruction block is coupled to an output of a wavelet denoising unit to receive denoised wavelets belonging to the first to the third scales.

19. The system of claims 11 to 18, the system further comprising

a data compression block, the data compression block receiving wavelets of the fifth to the eighth scales, wherein an output of the data compression block is coupled to the input of the first reconstruction block.

20. The system of claim 19, wherein the data compression block is realized using finite-impulse-response filters and infinite-impulse-response filters, wherein either filter compensates poles and zeros of the other filter.

21. The system of any one of the preceding claims, wherein the signal processing blocks comprises a baseline drift removal unit, the baseline drift removal unit coupled to the respective output of the wavelet transforming unit emitting wavelets belonging to the seventh and the eighth scales.

22. The system of claim 21, wherein the baseline drift removal block is realized by an adaptive cascaded filter arrangement, the cascaded filter arrangement comprising at least one filter stage.

23. The system of claim 22, wherein the adaptive cascaded filter arrangement automatically switches off filter stages unnecessary for performing baseline drift removal.

24. The system of claim 23, wherein the unnecessary filter stages are those larger than a filter stage in which the difference in the output value of the filter stage and an output value of the largest filter stage is smaller than a specified threshold.

25. The system of claims 22 to 24, wherein the adaptive cascaded filter arrangement comprises chebyshev IIR filters.

26. The system of claims 8 to 25, wherein the signal processing blocks comprise a QRS detection unit, the QRS detection unit coupled to the output of the at least one wavelet denoising unit and the output of the wavelet transforming unit emitting wavelets belonging to the fourth scale.

27. The system of claim 26, wherein the QRS detection unit comprises

a wavelet summation unit to sum the denoised wavelets from the at least one wavelet denoising unit and the wavelets from the wavelet transforming unit, wherein QRS peaks are detected when the summed wavelets exceed an adaptive threshold value.

28. The system of claim 27 wherein the QRS detection unit is realized using any of a Field Programmable Gate Array (FPGA), Application Specific Integrated Circuits (ASIC) or software implemented; the wavelet summation unit comprising an adder; and the QRS peaks are detected using a subtractor and multiplexer.

29. The system of claims 27 or 28, wherein the adaptive threshold value is derived from a standard deviation of a number of sampled summed wavelets.

30. The system of claims 26 to 29, further comprising a HBR analysis unit, the HBR analysis unit coupled to an output of the QRS detection unit.

31. The system of claim 30, wherein the HBR analysis unit comprises a counter; two multiplication blocks; an adder and a delay block, wherein the HBR analysis unit is realized by a Field Programmable Gate Array (FPGA), Application Specific Integrated Circuits (ASIC) or software implemented.

32. The system of claims 30 or 31, wherein the HBR analysis unit is adapted to predict QRS peak intervals based on a forward prediction algorithm.

33. The system of claim 30, wherein the forward prediction algorithm is based on summing previous QRS peak intervals weighted with a forgetting factor, the forgetting factor determining the number of previous QRS peak intervals included for HBR analysis.