

MULTIPLE VIDEO INPUT CLAMPING ARRANGEMENT

This invention relates to video processing systems generally and particularly to video signal clamping circuits for use
5 in video processing systems.

Image information represented by a composite television signal is defined by a luminance component and additionally a chrominance component in the case of a color video signal. A brightness reference level is contained in a black level of
10 the luminance component, and any variations in this DC level result in undesirable image brightness variations.

In a video signal processing system having multiple video input signals, changing the selected input video signal will result in undesirable image brightness variations (e.g., picture
15 flashing) if the black level of the old and new input signals are different. In addition, in a video signal processing system, such as a television system, having the capability of displaying a secondary or auxiliary image as well as a main image, such as in a picture-in-picture (PIP) system, it is desirable that the brightness
20 levels of the main and secondary images are approximately the same. Video processing systems capable of displaying main and secondary images may allow individual selection of a number of different video input signals for display as either the main or secondary image, making the balancing of image brightness even
25 more difficult.

To prevent black level differences in a multiple input system it is known to clamp a reference level, such as the black levels or peaks of the synchronization pulses ("sync tips") of the synchronization intervals of all of the video input signals to a
30 common reference level.

Signal processing errors may occur even though the video input signals are all clamped to a common reference signal. For example, if a synchronization signal separator including a level comparator ("sync slicer") is used to extract the synchronization
35 components, offsets in the signal processing channel between the input selection switch and the sync separator will introduce

errors. Such errors occur whether the signal processing channel is analog or digital.

Feedback from the output of the signal processing channel to the clamping circuit may be used to reduce clamping errors. An analog feedback clamp is described in U.S. Patent No. 4,197,557 (Tuma et al.). A prior art digital feedback clamping circuit is shown in Figure 2. This digital feedback clamp will clamp the DC level of an A/D converter output to a level determined by a digital comparator.

10 Unfortunately, such known feedback clamping arrangements are only operative upon a single video input signal. Accordingly, in a multiple input video signal processing system, the unselected video input signals will not be clamped to the same DC level as the selected video input signal. As such, this circuit
15 arrangement is susceptible to the undesirable image brightness variations during input reselection and during simultaneous display of main and PIP images, as previously described.

This invention concerns a video signal clamping apparatus having a first mode of operation for clamping an input
20 signal to a first reference level, a second mode of operation for clamping a signal derived from the input signal to a second reference signal and a means for selecting the mode of operation.

Illustratively, the invention allows a video signal processing system having multiple video inputs, a video
25 processing channel to selectively clamp a video input signal using a predetermined DC reference level or a DC reference level derived from the output signal of the signal processing channel. Accordingly, a selected video signal can be clamped to the DC reference level derived from the output of the signal processing
30 channel and an unselected signal can be clamped to the predetermined DC reference level. Brightness variations are reduced because the selected and unselected video input signals are both clamped to DC reference levels.

The invention will be described with reference to the
35 accompanying Drawing, in which:

Figure 1 shows a multiple video input television system including signal clamping apparatus embodying the invention;

Figure 2 shows a prior art signal clamping apparatus which is employed as part of an embodiment of the invention in accordance with another aspect of the invention;

Figure 3 shows a multiple video input television system including signal clamping apparatus embodying the invention; and

10 Figure 4 shows an A/D converter circuit suitable for use with the television systems of Figures 1 and 3.

Like reference designators in the various Figures refer to the same or similar elements.

Referring to Figure 1, a video signal processing system, 15 illustratively a television system, includes N video inputs, although only two, 101 and 201, of the N inputs are shown. First CV1 and second CV2 composite video input signals are coupled by respective capacitors C1 and C2 to switch 300 and to switch 400. Capacitors C1 and C2 include respective output nodes 102 and 20 202. The capacitor output nodes 102 and 202 are coupled to respective clamping circuits for controlling the DC levels of the signals present at the respective capacitor output nodes. Elements 100 and 200 comprise portions of clamping circuits for CV1 and CV2.

25 A portion of the clamping circuitry used to control the DC level for the CV2 input signal is shown as 200 in Figure 1.

The television system of Figure 1 includes a main picture processing channel and a picture-in-picture (PIP) processing channel. When a video input signal is selected for PIP 30 processing, the selected video signal is clamped by the clamping arrangement to a DC reference level derived from the selected input signal after it has been processed by the PIP processing channel so as to reduce offsets due to the processing. However, even when a video input signal is not selected for processing by 35 the PIP processing channel, the DC level of the unselected video signal is clamped to a DC reference level such that subsequent

selection of the video signal will not result in undesirable image brightness variations.

The main processing channel includes a switch 400, responsive to a controller 350, for selectively coupling one of the
 5 N video input signals to an analog to digital converter 410. The A/D converter 410 converts the selected input video signal into an 8-bit data stream which is presented to a comb filter 420 for processing into separate digital luminance DYM and chrominance DCM data streams. The digital luminance DYM and chrominance
 10 DCM data streams are converted into respective analog luminance AYM and chrominance ACM signals by respective digital to analog converters 430 and 440. The main analog luminance AYM and chrominance ACM signals are then coupled to a first pair of input terminals of a switch 500.

15 The PIP processing channel includes a switch 300, responsive to a controller 350, for selectively coupling one of the N video input signals to an analog to digital converter 310. The A/D converter 310 converts the input video signal into an 8-bit data stream which is presented to a digital signal processor (DSP)
 20 320 and a digital comparator 360. The DSP 320 is responsive to the controller 350 for processing the digital video data stream to produce a digital luminance data stream DYP and a digital chrominance data stream DCP representative of the secondary or small image. The DSP 320 reduces the size of the image
 25 represented by the secondary luminance and chrominance video signals by deleting pixels and lines of these components. The digital luminance DYP and chrominance DCP data streams are converted into respective analog luminance AYP and chrominance ACP signals by respective digital to analog converters 330 and
 30 340. The PIP analog luminance AYP and chrominance ACP signals are then coupled to a second pair of input terminals of switch 500.

Switch 500, responsive to controller 350 operating in a "main" mode, couples only the main analog luminance AYM and chrominance ACM signals to a luminance and chrominance
 35 processor 600. The luminance signal is processed to control the contrast, sharpness and brightness properties of the picture. The

chrominance signal is demodulated to produce red R-Y, green G-Y and blue B-Y color difference signals and processed to control the saturation and tint properties of the picture. The processed luminance signal Y and the color difference signals R-Y, G-Y, B-Y
 5 are coupled to an output amplifier and matrix or "driver" 700 which supplies high level red R, green G and blue B signals to a display device 800.

Switch 500, responsive to controller 350 operating in a "PIP" mode, additionally couples the PIP analog luminance AYP
 10 and chrominance ACP signals to luminance and chrominance processor 600 during a predetermined portion of the main image such that the video signal processed by the PIP processing channel is displayed as a small picture within the larger main picture by the display device 800.

15 Clamp 100 receives a reference signal CLAMP_REF1, a switch control signal ADC_FB and a selection signal USE_ADC_FB1. Similarly, clamp 200 receives a reference signal CLAMP_REF2, a switch control signal which is the same as ADC_FB and a selection signal USE_ADC_FB2. The remainder of the description will refer
 20 primarily to clamp 100, since clamps 100 and 200 are similar.

The respective reference signals CLAMP_REF1 and CLAMP_REF2 are DC voltage levels. These voltage levels may be from different voltage sources or a common voltage source. The purpose of the respective reference signals CLAMP_REF1 and
 25 CLAMP_REF2 is to establish the clamping levels for respective video signals which are not selected for processing by PIP video processing channel.

The switch control signal ADC_FB is produced by the PIP video processing channel in the exemplary embodiment. This
 30 switch control signal is derived, e.g., by comparing the output of an A/D converter 310 to a digital word representing a DC signal reference level, e.g., corresponding to the sync tip level. The purpose of the switch control signal ADC_FB is to establish the clamping level for a video signal which is selected for processing
 35 by the PIP video processing channel.

The selection signal USE_ADC_FB is produced by controller 350. The construction of controller 350 is not critical to the invention; it may comprise a microprocessor or microcontroller circuit, a state machine, a combinational logic circuit or an analog control circuit. Controller 350 may also incorporate a user input, e.g., remote control input(s).

Clamps 100 and 200 have two modes of operation; a first (unselected) mode is used to clamp inputs which are not selected for processing by the PIP video processing channel and a second (selected) mode is used to clamp inputs which are selected for PIP processing. Unselected mode and selected mode are determined by, respectively, a logic low and logic high level of the USE_ADC_FB reference selection signal.

In the illustrated embodiment clamping circuit 100 is a sync tip clamp. The sync-tip clamp 100 includes coupling capacitor C1, comparator 120, switch 140, switch 150, current sources 160 and 170. Sync tip clamp 100 may also include an optional low pass filter (not shown), the purpose of which will be described after the basic operation of the sync tip clamp 100 is described.

The video signal to be clamped is applied to the input terminal 101 of a coupling capacitor C1. In the illustrative example, the horizontal synchronizing pulses are negative-going pulses and positive-going excursions of active video represent white areas of the images. The DC restored or clamped video output signal is provided at the output terminal 102 of the capacitor C1.

The video signal at output terminal 102 of capacitor C1 is coupled to an inverting input terminal of comparator 120. A reference potential CLAMP_REF1 is applied to a non-inverting input terminal of comparator 120. Comparator 120 generates a bilevel output signal which is relatively positive when the amplitude of the video signal is less than CLAMP_REF1 and relatively negative when the amplitude of the video signal is greater than CLAMP_REF1.

In the non-selected mode ($USE_ADC_FB=0$), the bilevel output of comparator 120 is coupled to switch 150 via switch 140. Switch 150 closes in response to a relatively positive level output from comparator 120. When switch 150 closes a constant current from current source 160 is coupled to terminal 102 of capacitor C1. The current begins to charge capacitor C1 such that DC voltage level of the signal at terminal 102 increases. As the DC level of the signal at terminal 102 increases, the DC level of the video signal applied to the inverting input of comparator 120 also increases. When the video signal at the inverting input of comparator 120 exceeds the CLAMP_REF signal at the non-inverting input of comparator 120, the bilevel output signal generated by comparator 120 will become relatively negative. This relatively negative level will cause switch 150 to open, thereby decoupling current source 160 from terminal 102. At this time current source 170 will begin to discharge capacitor C1 such that DC level of the video signal at terminal 102 decreases. Current source 170 is coupled to terminal 102 and sinks current (e.g., 1 mA) from the capacitor C1 tending to drive terminal 102 to a relatively negative potential. The current source 170 insures that the system does not lock up at an erroneous relatively positive DC value. The first control loop operates to clamp the DC level of the signal at terminal 102 to the DC level of the reference voltage CLAMP_REF1.

In selected mode ($USE_ADC_FB=1$), switch 140 couples the clamp control signal ADC_FB to switch 150. During the operation of the second control loop, the switch control signal ADC_FB is used to directly control switch 150 and comparator 120 is bypassed. Clamp control signal ADC_FB is derived by comparing the output of A/D converter 310 to a digital word representing a -40 IRE reference level. ADC_FB is also a bilevel signal which indicates whether or not the output level of A/D converter 310 exceeds the -40 IRE clamping level.

Assuming that the instantaneous video signal applied to comparator 360 contains amplitude levels below -40 IRE (representing the "blacker-than-black" level of the tip of a

synchronizing pulse), the bilevel output ADC_FB of comparator 360 will be relatively positive. As such, switch 150 will close and a constant current (e.g., 25uA) from current source 160 will begin to charge capacitor C1 such that DC voltage level of the signal at terminal 102 increases. As the DC level of the video signal at terminal 102 increases the video signal applied to the A/D converter 310 also increases and the A/D converter 310 responsively increases the DC level of the digital video output signal. When the instantaneous level video signal applied to comparator 360 does not fall below -40 IRE, the bilevel output ADC_FB of comparator 360 will become relatively negative. This relatively negative signal will cause switch 150 to open, thereby decoupling current source 160 from terminal 102. At this time current source 170 will begin to discharge capacitor C1 such that DC voltage level of the signal at terminal 102, and therefore the DC level of the video signal, decreases. This second control loop operates to clamp the minimum amplitude level of the video signal to the -40 IRE level.

The video signal from the output terminal 102 of capacitor C1 may be coupled to comparator 120 via an optional low pass filter (LPF). The LPF is used when the input video signal is a composite video signal containing both luminance and chrominance components. When used, the LPF may comprise, e.g., a series resistor and a shunt capacitor. The 3dB frequency rolloff point of the LPF should be selected to pass horizontal synchronizing pulses while attenuating noise and the higher frequency components of the active video signal including burst. In addition, the series resistor in the LPF should be sufficiently large to preclude loading of terminal 102.

Referring to Figure 4, A/D converter circuit 310 is depicted along with comparator 360. An analog video signal A_CLAMPED received from a clamping circuit (e.g., clamp 100 via switch 300) is coupled to an A/D converter 310A. The A/D converter 310A converts the analog video signal A_CLAMPED into a digital video signal D_CLAMPED comprising a series of digital words corresponding to respective samples of the analog video

signal A_CLAMPED at a sampling rate determined by the frequency of a clocking signal CLOCK. In the exemplary embodiment an 8-bit A/D converter is used. The digital signal D_CLAMPED is coupled to a digital signal processor 320 (shown in Figure 1).

Clamp control signal ADC_FB is derived by coupling the digital video signal D_CLAMPED to comparator 360. A chrominance notch filter 310B may be inserted between A/D converter 310A and comparator 360 for the reasons discussed below. Chrominance notch filter 310B may be used to strip away chrominance components when the digital video signal D_CLAMPED contains both luminance and chrominance components. Comparator 410C compares the digital video signal D_CLAMPED to a signal representative of the -40 IRE level, as previously described. It will be appreciated by those skilled in the art that optional chrominance notch 310B and comparator 360 described above may be implemented by a variety of circuits, e.g., discrete logic, state machines, digital signal processors (DSPs), etc..

The A/D converter circuit 310 includes a resistor ladder network 310G comprising a number of series-connected resistors, although the only resistors shown are top (V+ connected), bottom (ground connected), R1, R8, R24 and R256 resistors. The upper and lower conversion range of A/D converter 310A is set by the voltage reference taps at the top and bottom resistors. The remaining resistors determine the discrete reference voltage steps used by A/D converter 310A to convert the analog video signal A_CLAMPED into the digital video signal D_CLAMPED.

The signal CLAMP_REF is derived from the voltage level at ladder resistor R8 via a buffer amplifier 310D. This voltage corresponds to the appropriate reference level for the sync tip of the video signal A_CLAMPED. The CLAMP_REF signal may be provided to each of the clamp circuits to replace the reference signals CLAMP_REF1, CLAMP_REF2 . . . CLAMP_REFN. By using CLAMP_REF as the unselected mode reference level, the unselected input video signals CV1 and CV2 through CVN are

clamped to a brightness level directly related to the operating range of A/D converter 310A. As such, when an unselected video input is selected for video processing, there will be little (if any) undesirable image brightness variations.

5 When an input video signal is not selected for processing, the inventive clamping arrangement clamps the unselected video signal to a DC voltage level. When the unselected video input is subsequently selected for processing, the inventive clamping arrangement will be able to change from unselected to
10 selected mode while keeping the clamped video signal within the DC level limits of the PIP processing channel. The transitional response is fairly rapid because the unselected video signal was previously clamped to a DC level approximating the level required for the selected video signal. As previously discussed, this
15 approximation may be improved by using an inactive mode clamping level derived from the ladder network of the A/D converter in the selected channel.

Referring to Figure 3, a video signal processing system similar to the system of Figure 1 is shown. The television system
20 of Figure 3 includes N video inputs, although only three, 101, 201 and 301, of the N inputs are shown. First composite video input signal CV1 is clamped by CLAMP1, which includes capacitor C1 and (not shown) comparator 120, switch 140, switch 150, and current sources 160 and 170. Second composite video input signal
25 CV2 is clamped by CLAMP2, which includes capacitor C2. Third composite video input signal CV3 is clamped by CLAMP3, which includes capacitor C3. Unlike the video signal processing system of Figure 1, the system of Figure 3 provides for switch selectable feedback to the clamp circuits from either the main A/D converter
30 circuit 410 or the PIP A/D converter circuit 310.

The output signals of the two A/D converter circuits 310 and 410 are coupled to a feedback switch and comparator circuit 900 which is responsive to controller 350. The feedback switch and comparator circuit 900 includes a first comparator for
35 comparing the output of the main A/D converter to a digital word representing -40 IRE and a second comparator for comparing the

output of the PIP A/D converter to a digital word representing -40 IRE. Each of the comparator circuits operate in the manner previously described with respect to comparator 360 and each comparator produces a respective output signal. The feedback switch and comparator circuit 900 also includes a switching network which controllably couples the output of either comparator to any of the three clamp circuits CLAMP1-CLAMP3 as clamping switch control signals ADC_FB1, ADC_FB2 or ADC_FB3 respectively. In addition, feedback switch and comparator network 900 provides the three respective clamp selection signals USE_ADC_FB1, USE_ADC_FB2 and USE_ADC_FB3 in response to controller 350.

The video signal processing system of Figure 3 allows clamping of the main and PIP input video signals to levels determined by the respective main and PIP analog to digital converter circuits.

The invention has been described in terms of conventional video signals including horizontal synchronizing components, however, it should be appreciated that it is applicable to any signals having, e.g., pulsed intervals, the amplitude of which bears some relationship to the DC reference value of the signal.

It will be apparent to those skilled in the art, that although the invention has been described in terms of specific examples, modifications and changes may be made to the disclosed embodiments without departing from the essence of the invention. For example, although the invention has been described in terms of certain types of video signals such as composite video signals, it is also applicable when other types of video signals, such as component video signals, are processed. In addition, although the invention has been described with reference to an embodiment in which a digital processing channel is utilized, it is also applicable when an analog signal processing channel is utilized. It is, therefore, to be understood, that the appended claims are intended to cover all modifications which naturally flow from the foregoing description and examples.



Claims:

1. Apparatus comprising:
means for comparing a first signal to a first reference
5 level and for comparing a second signal to a second reference
level, said second signal being derived from said first signal;
means responsive to said comparison means for
adjusting said first signal such that during a first mode of
operation said first signal is clamped to said first reference level
10 and during a second mode of operation said second signal is
clamped to said second reference level; and
means for selecting said mode of operation.
2. The apparatus of Claim 1 further comprising
15 analog to digital converter means for deriving said second signal
from said first signal.
3. The apparatus of Claim 1 wherein said first
signal is a composite video signal.
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4. The apparatus of Claim 1 wherein said first
signal is a component video signal.
5. The apparatus of Claim 2 wherein said first
25 signal is a composite video signal.
6. The apparatus of claim 5 wherein said first
reference level represents the nominal level of the most negative
excursion of said first signal and said second reference level
30 represents the nominal level of the most negative excursion of
said second signal.



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7. The apparatus of claim 6 wherein:

said comparison means includes an analog comparator for comparing said first signal to said first reference level and a digital comparator for comparing said second signal to said second
5 reference level; and

said comparison means couples an output of said first comparator to said adjusting means in said first mode of operation and couples an output of said second comparator to said adjusting means in said second mode of operation.

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8. The apparatus of Claim 7 wherein said adjusting means comprises:

charging means for increasing a DC level of said first signal responsive to a first output level from said comparison
15 means; and

discharging means for decreasing said DC level of said first signal responsive to a second output level from said comparison means.

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9. The apparatus of claim 8 wherein said first signal is coupled to said analog comparator by a low pass filter circuit.

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10. Method comprising the steps of:

selecting a first or second mode of operation;

comparing a first signal to a first reference level in
said first mode of operation;

deriving a second signal from said first signal;

comparing said second signal to a second reference
30 level in said second mode of operation; and

responsively adjusting said first signal such that said first signal is clamped to said first reference level in said first mode of operation and said second signal is clamped to said second reference level in said second mode of operation.

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11. The method as recited in claim 10 wherein said first signal is an analog signal and said second signal is a digital signal which is derived from said first signal using an analog to digital converter.