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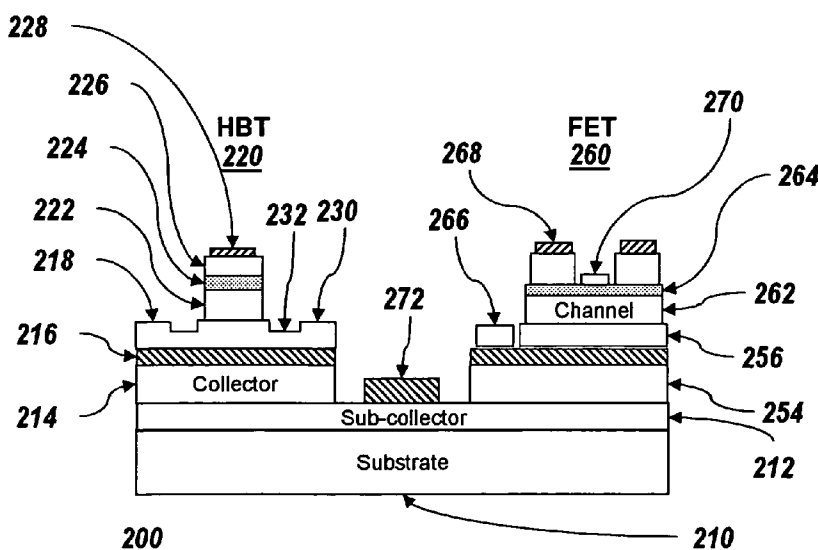


Fig. 2

(57) Abstract: Methods and systems for fabricating an integrated BiFET using two separate growth procedures are disclosed. Performance of the method fabricates the FET portion of the BiFET in a first fabrication environment. Performance of the method fabricates the HBT portion of the BiFET in a second fabrication environment. By separating the fabrication of the FET portion and the HBT portion in two or more separate reactors, the optimum device performance can be achieved for both devices.



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