

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
27 March 2008 (27.03.2008)

PCT

(10) International Publication Number
WO 2008/036047 A1

(51) International Patent Classification:
H01L 21/822 (2006.01) **H04B 1/44** (2006.01)
H01L 27/088 (2006.01)

(21) International Application Number:
PCT/SG2006/000278

(22) International Filing Date:
21 September 2006 (21.09.2006)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US):
NANYANG TECHNOLOGICAL UNIVERSITY
[SG/SG]; 50 Nanyang Avenue, Singapore 639798 (SG).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ZHANG, Yue Ping**
[CN/SG]; 75A Nanyang View, Singapore 639656 (SG). **LI, Qiang** [CN/SG]; 35 Jurong East Ave 1, #10-05, Singapore 609774 (SG).

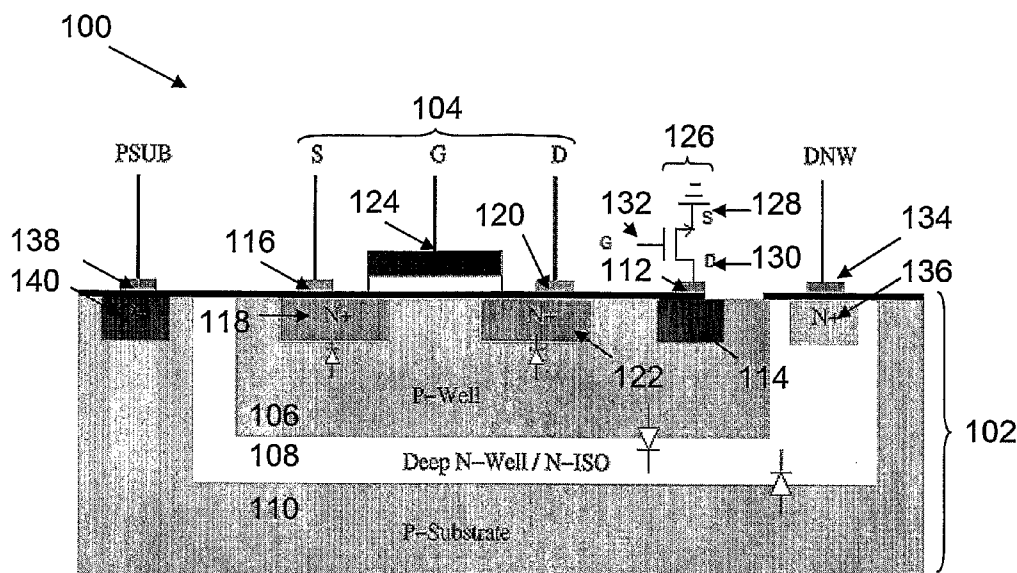
(74) Agent: **BOGSCH, Adam**; Viering, Jentschura & Partner,
P.O. Box 1088, Rochor Post Office, Rochor Road, Singapore 911833 (SG).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

(54) Title: TRIPLE WELL TRANSMIT-RECEIVE SWITCH TRANSISTOR



(57) Abstract: A transistor arrangement including a triple well structure, the triple well structure including a substrate of a first conductivity type, a first well region of a second conductivity type formed within the substrate and a second well region of the first conductivity type being separated from the substrate by the first well region. The transistor arrangement further includes a first transistor formed on or in the second well region, the first transistor including a body terminal being connected to the second well region and a second well region switch being connected to the body terminal of the first transistor.