material.

In FIG. 3b, an encapsulant material or molding compound 132 is dispensed into area 130, between upper plate 120a and lower plate 120b, using compressive molding, transfer molding, liquid encapsulant molding, or other suitable applicator. Encapsulant 132 can be a liquid, granular, or powder form, or sheet form of polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler from 40% up to 95% content. When cured and removed from mold chase 120, encapsulant 132 forms a polymer matrix composite substrate wafer or panel 134 with laminated film 128, as shown in FIG. 3c. Alternatively, laminated film 128 can cover the full surface of substrate 134. The polymer matrix composite substrate 134 has high resistivity, low loss tangent, lower dielectric constant, coefficient of thermal expansion (CTE) matching the overlaying IPD structure, and good thermal conductivity.

In FIG. 3d, film layer 128 is patterned and etched to provide a first conductive layer 128a-128c, as well as to form an indentation or shallow cavity 136 with surface 138 in polymer matrix composite substrate 134. Cavity 136 is optional with film layer 128 fully covering the surface of panel 134. The individual portions of conductive layer 128a-128c can be electrically common or electrically isolated depending on the connectivity of the individual semiconductor die.

In FIG. 3e, an optional planarization insulating layer 142 can be formed over polymer matrix composite substrate 134 and conductive layer 128 as one or more layers of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), silicon oxynitride (SiON), tantalum pentoxide (Ta_2O_5), aluminum oxide (Al_2O_3), polyimide, benzocyclobutene (BCB), polybenzoxazoles (PBO), WPR,

Claims

What is claimed:

1. A semiconductor device, comprising:

a polymer matrix composite substrate;

a first insulating layer completely covering a surface of the polymer matrix composite substrate;

an inductor formed over the first insulating layer; and

an interconnect structure formed over the inductor and first insulating layer and configured to electrically and mechanically connect the semiconductor device to a second substrate.

2. The semiconductor device of claim 1, further including a capacitor formed over the polymer matrix composite substrate, the capacitor including,

a first conductive layer formed over the polymer matrix composite substrate;

a second insulating layer formed over the first conductive layer; and

a second conductive layer formed over the second insulating layer.

3. The semiconductor device of claim 2, further including a third insulating layer formed over the second insulating layer.

4. The semiconductor device of claim 1, further including a second insulating layer formed over the first insulating layer and inductor.

5. The semiconductor device of claim 1, wherein the interconnect structure includes a bump.

6. The semiconductor device of claim 1, further including a resistive layer formed over the polymer matrix composite substrate.

7. A semiconductor device, comprising:

a polymer matrix composite substrate;

a first insulating layer formed over the polymer matrix composite substrate;

an integrated passive device formed over the first insulating layer; and

an interconnect structure formed over the first insulating layer to couple the integrated passive device to a second substrate.

8. The semiconductor device of claim 7, wherein the integrated passive device includes an inductor.

9. The semiconductor device of claim 7, wherein the integrated passive device includes a capacitor comprising,

a first conductive layer formed over the polymer matrix composite substrate;

a second insulating layer formed over the first conductive layer; and

a second conductive layer formed over the second insulating layer.

10. The semiconductor device of claim 7, wherein the interconnect structure includes a bump.

11. The semiconductor device of claim 7, further including a resistive layer formed over the polymer matrix composite substrate.

12. The semiconductor device of claim 7, further including a second insulating layer formed over the first insulating layer and integrated passive device.

13. The semiconductor device of claim 7, wherein a coefficient of thermal expansion of the polymer matrix composite substrate matches a coefficient of thermal expansion of the integrated passive device.

14. A semiconductor device, comprising:

a polymer matrix composite substrate;

an integrated passive device formed over the polymer matrix composite substrate; and

an interconnect structure formed over the integrated passive device and configured to attach the semiconductor device to a second substrate.

15. The semiconductor device of claim 14, wherein the integrated passive device includes an inductor.

16. The semiconductor device of claim 14, wherein the integrated passive device includes a capacitor comprising,

a first conductive layer formed over the polymer matrix composite substrate;

an insulating layer formed over the first conductive layer; and

a second conductive layer formed over the insulating layer.

17. The semiconductor device of claim 14, wherein the interconnect structure includes a bump.

18. The semiconductor device of claim 14, further including a resistive layer formed over the polymer matrix composite substrate.

19. The semiconductor device of claim 14, further including:

a first insulating layer formed over the polymer matrix composite substrate; and

a second insulating layer formed over the first insulating layer and integrated passive device.

20. The semiconductor device of claim 14, wherein a coefficient of thermal expansion of the polymer matrix composite substrate matches a coefficient of thermal expansion of the integrated passive device.

21. A semiconductor device, comprising:

a polymer matrix composite substrate;

an integrated passive device formed over the polymer matrix composite substrate; and

an interconnect structure disposed over the integrated passive device to couple the integrated passive device to a second substrate.

22. The semiconductor device of claim 21, wherein the interconnect structure includes a bump.

23. The semiconductor device of claim 22, further including a printed circuit board, wherein the bump is bonded to the printed circuit board.

24. The semiconductor device of claim 21, wherein a coefficient of thermal expansion of the polymer matrix composite substrate matches a coefficient of thermal expansion of the integrated passive device.