SEMICONDUCTOR DEVICE AND METHOD FOR FORMING PASSIVE CIRCUIT ELEMENTS WITH THROUGH SILICON VIAS TO BACKSIDE INTERCONNECT STRUCTURES

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device with integrated passive circuit elements interconnected to backside solder bumps.

Background of the Invention

Semiconductor devices are found in many products in the fields of entertainment, communications, networks, computers, and household markets. Semiconductor devices are also found in military, aviation, automotive, industrial controllers, and office equipment. The semiconductor devices perform a variety of electrical functions necessary for each of these applications.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each semiconductor die contains hundreds or thousands of transistors and other active and passive devices performing a variety of electrical functions. For a given wafer, each die from the

wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and environmental isolation.

One goal of semiconductor manufacturing is to produce a package suitable for faster, reliable, smaller, and higher-density integrated circuits (IC) at lower cost. Flip chip packages or wafer level chip scale packages (WLCSP) are ideally suited for ICs demanding high speed, high density, and greater pin count. Flip chip style packaging involves mounting the active side of the die facedown toward a chip carrier substrate or printed circuit board (PCB). The electrical and mechanical interconnect between the active devices on the die and conduction tracks on the carrier substrate is achieved through a solder bump structure comprising a large number of conductive solder bumps or balls. The solder bumps are formed by a reflow process applied to solder material deposited on contact pads which are disposed on the semiconductor substrate. The solder bumps are then soldered to the carrier substrate. The flip chip semiconductor package provides a short electrical conduction path from the active devices on the die to the carrier substrate in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

In many applications, it is desirable to form passive circuit elements, including inductors, resistors, and capacitors, on the semiconductor wafer. The inductor and capacitor allows the IC to perform reactive circuit functions

without using external circuit components. The passive circuit elements, particularly inductors, occupy significant area on the die. The inductors are typically formed as coiled or wound metal layers on the surface of the substrate which consumes a large area. The die must also accommodate interconnect structures, such as solder bumps, which also occupy significant space. The demand for smaller die with high feature density is challenging to achieve when taking into account the interconnect requirements.

A need exists to integrate passive circuit elements and interconnect structures with the demand for smaller and denser semiconductor die.

Summary of the Invention

In one embodiment, the present invention is a semiconductor device comprising a substrate and via formed through the substrate. A first insulating layer is formed over a first surface of the substrate. A first conductive layer is formed over the first insulating layer. A resistive layer is formed over the first conductive layer. A second insulating layer is formed over the resistive layer. A third insulating layer is formed over the first insulating layer and first conductive layer. A second conductive layer is formed over the second and third insulating layers and first conductive layer. The first and second conductive layers extend into the via to form a conductive via. A fourth insulating layer is formed over a second surface of the substrate opposite the first surface of the substrate. A UBM is formed over the second surface of the substrate and electrically connected to the conductive via.

In another embodiment, the present invention is a semiconductor device comprising a substrate and first conductive layer formed over a first surface of the substrate. A conductive via is formed through the substrate and electrically common with the first conductive layer. A first insulating layer is formed over the first conductive layer. A second insulating layer is formed over the substrate and first conductive layer. A second conductive layer is formed over the first and second insulating layers and first conductive layer. A UBM is formed over a second surface of the substrate and electrically connected to the conductive via.

In another embodiment, the present invention is a semiconductor device comprising a substrate having first and second surfaces and first conductive layer formed over the first surface of the substrate. An interconnect structure is formed between the first surface and second surface of the substrate and electrically common with the first conductive layer. A first insulating layer is formed over the first conductive layer. A second insulating layer is formed over the substrate and first conductive layer. A second conductive layer is formed over the first and second insulating layers and first conductive layer. A third conductive layer is formed over the second surface of the substrate and electrically connected to the interconnect structure.

In another embodiment, the present invention is a semiconductor device comprising a substrate and interconnect structure formed between a first surface and second surface of the substrate. An IPD is formed over the substrate and electrically connected to the interconnect structure. A UBM is formed over the second surface of the substrate and electrically connected to the interconnect structure.

Brief Description of the Drawings

FIG. 1 is a flip chip semiconductor device with solder bumps providing electrical interconnect between an active area of the die and a chip carrier substrate;

FIGs. 2a-2f illustrate a process of forming passive circuit elements with through silicon vias to backside solder bumps on the semiconductor package;

FIG. 3 illustrates a semiconductor package with passive circuit elements and backside RDL to solder bumps;

FIG. 4 illustrates a semiconductor package with passive circuit elements interconnected to topside wire bond pads and through silicon vias to backside solder bumps;

FIG. 5 illustrates a semiconductor package with passive circuit elements interconnected to other semiconductor packages; and

FIGs. 6a-6e illustrate an alternate process of forming passive circuit elements with through silicon vias to backside solder bumps on the semiconductor package.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as

defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing one or more electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

A semiconductor wafer generally includes an active surface having semiconductor devices disposed thereon, and a backside surface formed with bulk semiconductor material, e.g., silicon. The active side surface contains a plurality of semiconductor die. The active surface is formed by a variety of semiconductor processes, including layering, patterning, doping, and heat treatment. In the layering process, semiconductor materials are grown or deposited on the substrate by techniques involving thermal oxidation, nitridation, chemical vapor deposition, evaporation, and sputtering. Photolithography involves the masking of areas of the surface and etching away undesired material to form specific structures. The doping process injects concentrations of dopant material by thermal diffusion or ion implantation.

Flip chip semiconductor packages and wafer level packages (WLP) are commonly used with integrated circuits (ICs)

demanding high speed, high density, and greater pin count. Flip chip style semiconductor device 10 involves mounting an active area 12 of die 14 facedown toward a chip carrier substrate or printed circuit board (PCB) 16, as shown in FIG. 1. Active area 12 contains active and passive devices, conductive layers, and dielectric layers according to the electrical design of the die. Analog circuits may be created by the combination of one or more passive device formed within active area 12 and electrically interconnected. For example, an analog circuit may include one or more inductor, capacitor and resistor formed within active area 12. The electrical and mechanical interconnect is achieved through a solder bump structure 20 comprising a large number of individual conductive solder bumps or balls 22. The solder bumps are formed on bump pads or interconnect sites 24, which are disposed on active area 12. The bump pads 24 connect to the active circuits by conduction tracks in active area 12. The solder bumps 22 are electrically and mechanically connected to contact pads or interconnect sites 26 on carrier substrate 16 by a solder reflow process. The flip chip semiconductor device provides a short electrical conduction path from the active devices on die 14 to conduction tracks on carrier substrate 16 in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

FIG. 2a illustrates semiconductor wafer 28 having a substrate 30 made of silicon or other bulk semiconductor material. Trenches or vias 34 and 36 are cut into substrate 30 using a deep reactive ion etch (DRIE) process or silicon wet etching with potassium hydroxide (KOH) process. Trenches 34 and 36 will become through substrate vias (TSV) in later stages. An insulating layer 38 is deposited by chemical vapor

deposition (CVD) over substrate 30. The insulating layer 38 follows the contour of the substrate and provides a via liner for trenches 34 and 36. The insulating layer 38 can be made with silicon dioxide (SiO2), silicon oxynitride (SiON), silicon nitride (SixNy), tantalum pentoxide (Ta2O5), zirconium (Zr) oxide, or other material having dielectric properties. The thickness of insulating layer 38 ranges from 500 angstroms (Å) to 30 micrometers (μm) with a typical value of about 1000 Å.

In FIG. 2b, an electrically conductive layer 40 is deposited and patterned on insulating layer 38. Conductive layer 40 can be made with aluminum (Al), Al alloy, copper (Cu), nickel (Ni), gold (Au), silver (Ag), or other electrically conductive material. Cu is typically used in conjunction with an adhesion layer and barrier layer. Conductive layer 40 can have multiple layers such as titanium (Ti)/titanium nitride (TiN)/Al/TiN. The deposition of conductive layer 40 uses a physical vapor deposition (PVD), CVD, evaporation, electrolytic plating, or electroless plating process. The conductive layers 40 can be electrically common or electrically isolated depending on the connectivity of the individual devices formed on substrate 30. The pattern of conductive layer 40 in vias 34 and 36 is optional.

A resistive layer 42, noted as resistive layers 42a and 42b, is deposited and patterned on insulating layer 38 and connected to conductive layer 40 to form a resistor. Alternatively, resistive layer 42 can be connected through plating layer 50 and Cu layer 54 to form a resistor, see FIG. 2c. Resistive layer 42b is patterned between conductive layer 40 and insulating layer 46 to suppress the Hillock growth. Resistive layer 42 is made with silicide, doped poly silicon, tantalum nitride (TaN), nickel chromium (NiCr), or TiN having a

sheet resistivity up to about 100 ohm/square. The deposition of resistive layer 42 may involve PVD or CVD with a thickness ranging from 200-5000 Å.

An insulating layer 46 is deposited and patterned on resistive layer 42b. The insulating layer 46 may cover other circuit regions for insulation purposes. The insulating layer 46 can be made with SiO2, SixNy, SiON, Ta2O5, Zr oxide, or other dielectric material. The deposition of insulating layer 46 may involve PVD or CVD.

A passivation layer 48 is formed over the structure created in FIGs. 2a-2b for structural support and electrical isolation. Passivation layer 48 can be made with SiO2, SixNy, SiON, polyimide (PI), benzocyclobutene (BCB), polybenzoxazole (PBO), or other insulating material. A portion of passivation layer 48 is removed using a mask-defined photolithography process to expose conductive layers 40 and insulating layers 38 and 46.

In FIG. 2c, a metal plating layer 50, e.g. Cu plating, is deposited. The plating layer 50 has an adhesion layer and seed layer. The adhesion layer can be made with Ti, TiW, Ta/TaN, or Cr. The seed layer is typically Cu. A layer of photoresist 52 is patterned over plating layer 50 for Cu layer 54. Cu layer 54 can be deposited as a conformal coating over trenches 34 and 36. Alternatively, Cu layer 54 can be a via fill process which deposits Cu into vias 34 and 36. Cu layer 54 can be used to form interconnection as well as inductor wings or transmission lines. The inductor wings are formed together with TSV metal deposition through Cu plating. The Cu material in trenches 34 and 36 can be formed at the same time as Cu layer 54 and 54a on passivation layer 48. Alternately, a dual plating of the Cu layers fills trenches 34

and 36 and forms Cu layer 54a at different times. The optional conductive layer 40 in vias 34 and 36 improves metal step coverage and Cu fill process in the vias. Cu layers 54 can be electrically common or electrically isolated depending on the connectivity of the individual devices formed on substrate 30.

In FIG. 2d, photoresist 52 is removed. A portion of plating layer 50 is removed by etching. Passivation layer 58 is coated over the structure formed in FIGs. 2a-2c for structural support and electrical isolation. Passivation layer 58 can be made with SiO2, SixNy, SiON, PI, BCB, PBO, epoxy, or other insulating material.

In FIG. 2e, semiconductor wafer 28 is back grinded to expose TSV 34 and 36. Accordingly, conductive vias 34 and 36 pass through silicon substrate 30. A passivation layer 60 is deposited and patterned on the backside of semiconductor wafer 28. Passivation layer 60 can be made with SiO2, SixNy, SiON, PI, BCB, PBO, epoxy, or other insulating material. An under bump metallization (UBM) 62 is deposited and patterned to electrically contact Cu layer 54 in TSV 34 and 36. UBMs 62 can be made with Ti, Ni, NiV, Cu, or Cu alloy. UBMs 62 can be a multiple metal stack with adhesion layer, barrier layer, and wetting layer. The adhesion layer is made with Ti, Cr, Al, TiW, or titanium nitride (TiN). The barrier layer can be made with Ni, NiV, CrCu, or TiW. The wetting layer can be made with Cu, Au, or Ag. The exposed TSV 34 and 36 can be used for alignment of UBMs 62. Alternatively, a back side alignment (BSA) infrared (IR) alignment can be used to form UBMs 62.

An electrically conductive solder material is deposited over UBMs 62 through an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The solder material can be any metal alloy or

electrically conductive material, e.g., Sn, lead (Pb), Ni, Au, Ag, Cu, bismuthinite (Bi), and alloys thereof. The solder material is typically lead-free such as Sn96.5Ag3.5. The solder material is reflowed by heating the conductive material above its melting point to form spherical balls or bumps 66. In some applications, solder bumps 66 are reflowed a second time to improve electrical contact to UBMs 62. UBMs 62 and solder bumps 66 represent one type of interconnect structure.

In FIG. 2f, an optional polymer glue layer 70 is applied over passivation layer 58. Chip carrier 72 is bonded to semiconductor wafer 28 with polymer glue layer 70. Alternatively, backgrinding tape or permanent molding compound is applied without carrier 72. When permanent molding compound is applied, passivation layer 58 can be optional. The backgrinding tape or polymer glue with carrier 72 is removed before or after dicing. Alternatively, the glue and carrier may remain permanently attached and become part of the die.

The passive circuit elements, such as resistors, inductors, and capacitors, occupy a significant portion of the limited space on the surface of substrate 30. The interconnect structures like UBMs 62 and solder bumps 66 are disposed on the backside of the die. Semiconductor package 68 uses many TSVs like 34 and 36 to electrically connect the passive circuit elements on the topside of the die through UBMs 62 to solder bumps 66 on the backside of the die to provide for greater use of die area and improve reliability.

The semiconductor device in FIG. 2e has a number of passive circuit elements. Cu layer 54a represents a cross-sectional view of an inductor coiled on the surface of substrate 30. The inductor is formed as coiled or wound metal

layers on the surface of the substrate. The conductive layers 40 and Cu layers 54 can be electrically common or electrically isolated to connect the passive circuit elements according to the desired circuit function. For example, the portion of CU layer 54 overlying TSVs 34 and 36 can electrically contact Cu layer 54a to connect both ends of the inductor formed by Cu layer 54a through UBMs 62 to solder bumps 66 under TSVs 34 and 36, respectively.

In a similar manner, the resistive layer 42a also provides a passive circuit element, i.e., a resistor connected between conductive layers 40. The portion of Cu layers 54 overlying conductive layers 40 between resistive layer 42a can electrically contact Cu layers 54 overlying TSVs 34 and 36 to connect both ends of the resistor formed by resistive layer 42a through UBMs 62 to solder bumps 66 under TSV 34 and 36, respectively.

In another example, the combination of conductive layer 40, resistive layer 42b, insulating layer 46, conductive layer 50, and Cu layer 54 constitute a passive circuit, i.e., a resistor in series with a metal-insulator-metal (MIM) capacitor. The portion of Cu layer 54 in contact with conductive layer 40 under resistive layer 42b can electrically contact Cu layer 54 overlying TSV 34. The portion of Cu layer 54 overlying insulating layer 46 can electrically contact Cu layer 54 overlying TSV 36.

Accordingly, TSVs 34 and 36 allow the passive circuit elements to be placed on the topside of the die and to be electrically connected to the interconnect structures, which are disposed on the backside of the die. The placement of passive circuit elements on the topside of substrate 30 and the interconnect structures on the backside of substrate 30

provides for greater use of die area and improves reliability. The TSVs provide for electrical connection between the topside passive circuit elements and the backside interconnect structures. The inductor and MIM capacitor allow the semiconductor device to perform reactive circuit functions without using external circuit components.

FIG. 3 illustrates an alternate embodiment of the semiconductor package. Redistribution layers (RDL) 74 and 80 are formed over passivation layer 60. In one embodiment, RDLs 74 and 80 may include a wetting layer, barrier layer, and adhesive layer. RDLs 74 and 80 provide electrical contact between the Cu material in TSV 34 and solder bumps 78 and 82, respectively. RDLs 74 and 80 can be made with Al, aluminum copper alloy (AlCu), Cu, or Cu alloy with an adhesion and barrier layers. The adhesion layer can be Ti, TiN, TiW, Cr, or Ta. The barrier layer can be NiV, TaN, TiW, or CrCu. RDLs 74 and 80 operate as an intermediate conduction layer to route electrical signals from solder bumps 78 and 82 to various areas of the die, including active and passive circuits, and provides various electrical interconnect options during integration of semiconductor package 86. RDLs 74 and 80 provide routing options to relocate solder bumps 78 and 82 away from TSV 34 and 36. A passivation layer 84 is formed over RDLs 74 and 80 and passivation layer 60.

FIG. 4 illustrates an alternate embodiment of the semiconductor package. A TSV 34 is formed on the left side of the semiconductor package using the steps described in FIGs. 2a-2f. A wire bonding pad 90 is formed on the right side of semiconductor package.

FIG. 5 illustrates another embodiment of the semiconductor package. In this embodiment, multiple TSVs 34

and 36 and solder bumps 66 are provided on both ends of the semiconductor package. Passive devices and/or analog circuits 110 are mounted on passivation layer 58 with underfill material 114 and are electrically connected by contact pad 112. Semiconductor die 116 is mounted to passivation layer 58 with underfill material 118 and is electrically connected to Cu layers 54 with solder bumps 120. Semiconductor die 122 is mounted to passivation layer 58 with underfill material 124 and is electrically connected to Cu layers 54 with solder bumps 126. Molding compound 128 or other composite polymer materials with proper coefficient of thermal expansion (CTE) is deposited over the structures formed on FIG. 5. Topside grinding may be used to get a flatter surface.

FIG. 6a illustrates semiconductor wafer 129 having a substrate 130 made of silicon or other bulk semiconductor material. Trenches or vias 134 and 136 are cut into substrate 130 using wet silicon etching process such as KOH. Trenches 134 and 136 will become TSVs in later stages. An insulating layer 138 is deposited by CVD over substrate 130, following the contour of the substrate and providing a via liner for trenches 134 and 136. The insulating layer 138 can be made with SiO2, SiON, SixNy, Ta2O5, ZrO, or other material having dielectric properties. The thickness of insulating layer 138 ranges from 500Å to 30μm with a typical thickness of about 1000Å.

In FIG. 6b, an electrically conductive layer 140 is deposited and patterned on insulating layer 138. Conductive layer 140 can be made with Al, Al alloy, Ti/TiN/Al/TiN, Cu, Ni, Au, Ag, or other electrically conductive material. The pattern of conductive layer 140 in vias 134 and 136 is optional. The deposition of conductive layer 140 uses a PVD, CVD, evaporation, electrolytic plating, electroless plating, or

screen printing process. The conductive layers 140 can be electrically common or electrically isolated depending on the connectivity of the individual devices formed on substrate 130.

A resistive layer 142, noted as resistive layers 142a and 142b, is deposited and patterned on insulating layer 138 and conductive layer 140. Resistive layer 142 is made with silicide, doped poly Si, TaN, or NiCr having a resistivity up to about 100 ohm/square. The deposition of resistive layer 142 may involve PVD or CVD.

An insulating layer 146 is patterned and deposited on resistive layer 142b. The insulating layer 146 can be made with SiO2, SixNy, SiON, Ta2O5, Zr2O5, or other dielectric material. The deposition of insulating layer 146 may involve PVD or CVD with typical thickness of 200-4000Å.

A passivation layer 148 is formed over the structure created in FIGs. 6a-6b for structural support and electrical isolation. Passivation layer 148 can be made with SiO2, SixNy, SiON, PI, BCB, PBO, or other insulating material. A portion of passivation layer 148 is removed using a mask-defined photolithography process to expose conductive layers 140 and insulating layers 138 and 146.

In FIG. 6c, a metal plating 150, e.g. Cu plating, is deposited and patterned with thick photo resist 152. The plating layer 150 has an adhesion layer and seed layer. The adhesion layer can be made with Ti, TiW, Ta/TaN, or Cr. The seed layer is typically Cu. A layer of photoresist 152 patterns plating layer 150 for Cu layer 154. Cu layer 154 can also be deposited as a conformal coating over trenches 134 and 136. Alternatively, Cu layer 154 can be formed via a fill process which deposits Cu into vias 134 and 136. Cu layer 154 can be used to form interconnection as well as inductor wings

or transmission lines. The inductor wings are formed together with TSV metal deposition through Cu plating. The Cu layer 154 is a conductive material deposited in trenches 134 and 136 as well as other locations on the surface of substrate 130 to form conductive layers and passive devices or analog circuits. The Cu material in trenches 134 and 136 can be formed at the same time as Cu layer 154 and 154a on passivation layer 148. Alternately, a dual plating of the Cu layers fills trenches 134 and 136 and forms Cu layer 154a at different times. The Cu plating rate in trenches 134 and 136 improves with conductive layer 140. Cu layers 154 can be electrically common or electrically isolated depending on the connectivity of the individual devices formed on substrate 130.

In FIG. 6d, photoresist 152 is removed. A portion of Cu plating layer 150 is removed by etching. Passivation layer 158 is coated over the structure formed in FIGs. 6a-6c for structural support and electrical isolation. Passivation layer 158 can be made with SiO2, SixNy, SiON, PI, BCB, PBO, or other insulating material.

In FIG. 6e, semiconductor wafer 170 is back grinded to expose TSV 134 and 136. Accordingly, conductive vias 134 and 136 pass through silicon substrate 130. A passivation layer 160 is deposited and patterned on the backside of semiconductor wafer 170. Passivation layer 160 can be made with SiO2, SixNy, SiON, PI, BCB, PBO, epoxy, or other insulating material. A UBM 162 is deposited and patterned to electrically contact Cu layer 154 in TSV 134 and 136. UBMs 162 can be made with Ti, Ni, NiV, Cu, or Cu alloy. UBMs 162 can be a multiple metal stack with adhesion layer, barrier layer, and wetting layer. The adhesion layer is made with Ti, Cr, Al, TiW, or titanium nitride (TiN). The barrier layer can be made

with Ni, NiV, CrCu, or TiW. The wetting layer can be made with Cu, Au, or Ag. The exposed TSV 134 and 136 can be used for alignment of UBMs 162. Alternatively, a BSA/IR alignment can be used to form UBMs 162.

An electrically conductive solder material is deposited over UBMs 162 through an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The solder material can be any metal or metal alloy or electrically conductive material, e.g., Sn, Pb, Ni, Au, Ag, Cu, Bi, and alloys thereof. The solder material is reflowed by heating the conductive material above its melting point to form spherical balls or bumps 166. In some applications, solder bumps 166 are reflowed a second time to improve electrical contact to UBMs 162. UBMs 162 and solder bumps 166 represent one type of interconnect structure.

The passive circuit elements, such as resistors, inductors, and capacitors, occupy a significant portion of the limited space on the surface of substrate 130. The interconnect structures like UBMs 162 and solder bumps 166 are disposed on the backside of the die. Semiconductor package 170 uses many TSVs like 134 and 136 to electrically connect the passive circuit elements on the topside of the die through UBMs 162 to solder bumps 166 on the backside of the die to provide for greater use of the die area and improve reliability.

The semiconductor device in FIG. 6e has a number of passive circuit elements. Cu layer 154a represents a cross-sectional view of an inductor coiled on the surface of substrate 130. The inductor is formed as coiled or wound metal layers on the surface of the substrate. The conductive layers 140 and Cu layers 154 can be electrically common or electrically isolated to connect the passive circuit elements

according to the desired circuit function. For example, the portion of CU layer 154 overlying TSVs 134 and 136 can electrically contact Cu layer 154a to connect both ends of the inductor formed by Cu layer 154a through UBMs 162 to solder bumps 166 under TSVs 134 and 136, respectively.

In a similar manner, the resistive layer 142a also provides a passive circuit element, i.e., a resistor connected between conductive layers 140. The portion of Cu layers 154 overlying conductive layers 140 between resistive layer 142a can electrically contact Cu layers 154 overlying TSVs 134 and 136 to connect both ends of the resistor formed by resistive layer 142a through UBMs 162 to solder bumps 166 under TSV 134 and 136, respectively.

In another example, the combination of conductive layer 140, resistive layer 142b, insulating layer 146, conductive layer 150, and Cu layer 154 constitute a passive circuit, i.e., a resistor in series with a MIM capacitor. The portion of Cu layer 154 in contact with conductive layer 140 under resistive layer 142b electrically contacts Cu layer 154 overlying TSV 134. The portion of Cu layer 154 overlying insulating layer 146 electrically contacts Cu layer 154 overlying TSV 136.

Accordingly, TSVs 134 and 136 allows the passive circuit elements to be placed on the topside of the die to be electrically connected to the interconnect structures, which are disposed on the backside of the die. The placement of passive circuit elements on the topside of substrate 130 and the interconnect structures on the backside of substrate 130 provides for greater use of die area and improves reliability. The TSVs provide for electrical connection between the topside passive circuit elements and the backside interconnect

structures. The inductor and MIM capacitor allow the semiconductor device to perform reactive circuit functions without using external circuit components.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims

Claims

What is claimed:

1. A semiconductor device, comprising:

a substrate;

a via formed through the substrate;

a first insulating layer formed over a first surface of the substrate;

a first conductive layer formed over the first insulating layer;

a resistive layer formed over the first conductive layer;

a second insulating layer formed over the resistive layer;

a third insulating layer formed over the first insulating layer and first conductive layer;

a second conductive layer formed over the second and third insulating layers and first conductive layer, the first and second conductive layers extending into the via to form a conductive via;

a fourth insulating layer formed over a second surface of the substrate opposite the first surface of the substrate; and

an under bump metallization (UBM) formed over the second surface of the substrate and electrically connected to the conductive via.

2. The semiconductor device of claim 1, further including a third conductive layer formed over the fourth insulating layer between the conductive via and UBM.

3. The semiconductor device of claim 1, wherein the first conductive layer, resistive layer, second insulating layer, and

second conductive layer constitute a metal-insulator-metal capacitor.

4. The semiconductor device of claim 1, wherein a portion of the second conductive layer is wound to operate as an inductor.

5. The semiconductor device of claim 1, further including:

a fifth insulating layer formed over the third insulating layer and second conductive layer; and

an encapsulant deposited over the fifth insulating layer and substrate.

6. The semiconductor device of claim 5, further including a semiconductor die mounted over the fifth insulating layer and covered by the encapsulant and electrically connected to the second conductive layer.

7. A semiconductor device, comprising:

a substrate;

a via formed partially through the substrate to a depth less than a thickness of the substrate;

a conductive material deposited into the via to form a conductive via;

a first conductive layer formed over a first surface of the substrate, the first conductive layer extending into the via and electrically connected to the conductive via;

an integrated passive device (IPD) formed over the first surface of the substrate and electrically connected through the first conductive layer to the conductive via;

an under bump metallization (UBM) layer formed over a second surface of the substrate and electrically connected to the conductive via; and

a bump formed over the UBM layer.

8. The semiconductor device of claim 7, further including:

a first insulating layer formed over the first surface of the substrate and extending into the via;

a second conductive layer formed over the first insulating layers; and

a second insulating layer formed over the second conductive layer.

9. The semiconductor device of claim 7, further including a second conductive layer formed over the first conductive layer, wherein a portion of the second conductive layer is wound to operate as an inductor.

10. The semiconductor device of claim 7, further including an encapsulant deposited over the substrate.

11. The semiconductor device of claim 7, further including a semiconductor die mounted over the substrate.

12. The semiconductor device of claim 7, wherein the bumps are laterally offset with respect to the conductive via.

13. A semiconductor device, comprising:

a substrate;

a first conductive layer formed over a first surface of the substrate;

a conductive via formed through the substrate and electrically common with the first conductive layer;

a first insulating layer formed over the first conductive layer;

a second insulating layer formed over the substrate and first conductive layer;

a second conductive layer formed over the first and second insulating layers and first conductive layer;

an under bump metallization (UBM) formed over a second surface of the substrate and electrically connected to the conductive via;

a third insulating layer formed over the second insulating layer and second conductive layer; and

an encapsulant deposited over the third insulating layer and substrate.

14. The semiconductor device of claim 13, further including a semiconductor die mounted over the third insulating layer and covered by the encapsulant and electrically connected to the second conductive layer.

15. A semiconductor device, comprising:

a substrate;

an interconnect structure formed partially through a first surface of the substrate to a depth less than a thickness of the substrate;

an integrated passive device (IPD) formed over the substrate and electrically connected to the interconnect structure; and

an under bump metallization (UBM) layer formed over a second surface of the substrate and electrically connected to the interconnect structure.

16. The semiconductor device of claim 15, wherein the IPD includes:

a first conductive layer formed over the first surface of the substrate;

an insulating layer formed over the first conductive layer; and

a second conductive layer formed over the insulating layer.

17. The semiconductor device of claim 15, further including:

an insulating layer formed over the second surface of the substrate; and

a redistribution layer formed over the insulating layer between the interconnect structure and UBM.

18. The semiconductor device of claim 15, wherein the IPD includes a resistor, capacitor, or inductor.

19. The semiconductor device of claim 15, further including a bump formed over the UBM.

20. A semiconductor device, comprising:

a substrate having first and second surfaces;

a conductive via formed partially through the substrate to a depth less than a thickness of the substrate;

a first conductive layer formed over the first surface of the substrate and electrically connected to the conductive via; and

an electronic component mounted over the first surface of the substrate and electrically connected to the first conductive layer.

21. The semiconductor device of claim 20, further including:

an under bump metallization (UBM) layer formed over the second surface of the substrate and electrically connected to the conductive via; and

a bump formed over the UBM layer.

22. The semiconductor device of claim 20, further including:

a first insulating layer formed over the first surface of the substrate and extending into the via;

a second conductive layer formed over the first insulating layers; and

a second insulating layer formed over the second conductive layer.

23. The semiconductor device of claim 20, further including a second conductive layer formed over the first conductive layer, wherein a portion of the second conductive layer is wound to operate as an inductor.

24. The semiconductor device of claim 20, further including an encapsulant deposited over the substrate.

25. The semiconductor device of claim 20, further including a semiconductor die mounted over the substrate.

26. The semiconductor device of claim 20, wherein the bumps are laterally offset with respect to the conductive via.