A Circuit and Method for Reducing the Effects Of Parasitic Capacitances In Integrated Resistors

Field of the Invention

This invention relates to an electronic circuit having a resistor integrated therein and to a method of reducing the effects of parasitic capacitances in such a circuit, particularly, though not exclusively to such circuits for high frequency and precision applications.

Background of the Invention

In advanced or high-end monitors, there exists a need for amplifying high frequency video signals (up to 200MHz). However, the video bandwidth in such situations is limited by the parasitic capacitance that develops between the conductive (or semiconductive) layer forming the integrated resistor (hereinafter referred to as "resistance layer") and a lower conductive, or semiconductive, layer that is separated from the resistance layer by an insulating layer. This parasitic capacitance together with the integrated resistor forms a low pass filter in which the low frequency component can pass through while the high frequency component is attenuated. In addition, the linearity of the high frequency signal is also degraded due to the attenuation of the high frequency component. Hence, there exists a need to reduce the effects of parasitic capacitance of integrated resistors, especially for high frequency applications.

Brief Summary of the Invention

The present invention therefore seeks to provide a circuit and method for reducing the effects of parasitic capacitances in integrated resistors which overcome, or at least reduce the above-mentioned problems of the prior art.

Accordingly, in a first aspect, the invention provides an electronic circuit on a semiconductor chip having a resistor integrated therein, the resistor being formed by a resistance layer formed over an insulating layer formed over a first cancellation layer, wherein the circuit has an input for receiving an ac signal, the resistor being coupled between the input and a reference voltage potential, and a duplicating circuit coupled to the input for duplicating the ac signal and for applying the duplicated signal to

the first cancellation layer below the resistor so as to reduce parasitic capacitance between the resistance layer and the first cancellation layer.

In one embodiment, there is at least one further cancellation layer below the first cancellation layer, wherein the duplicating circuit is arranged for applying the duplicated signal to the further cancellation layer(s) to further reduce the parasitic capacitance.

The first and/or further cancellation layers can be either conductive or semiconductive layers.

In a preferred embodiment, the electronic circuit includes an amplifying circuit having a transistor coupled to the resistor and the duplicating circuit is similar to the amplifying circuit and has a transistor coupled to the cancellation layer.

According to a second aspect, the invention provides a method of reducing the effects of parasitic capacitance of a resistor integrated in an electronic circuit on a semiconductor chip, the method comprising the steps of:

i) applying a signal across the resistor;

ii) duplicating the signal; and

iii) applying the duplicated signal to a cancellation layer formed in the semiconductor chip below the resistor so as to reduce the effects of parasitic capacitance between a layer of the semiconductor chip forming the resistor and the cancellation layer.

Preferably, step (iii) comprises applying a voltage representing the signal to the cancellation layer below the resistor such that the voltage tracks the signal so that the potential difference between them is minimised.

Brief Description of the Drawings

Various embodiments of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a cross sectional view of part of a known integrated electronic circuit showing the parasitic capacitance;

FIG. 2 shows an equivalent circuit illustrating the cross sectional diagram of FIG. 1;

FIG. 3 shows a cross sectional view of part of an integrated electronic circuit, similar to that of FIG. 1, but showing the structure of one embodiment of the present invention;

FIG. 4 shows an equivalent circuit illustrating the cross sectional diagram of FIG. 3;

FIG. 5 is a circuit schematic diagram of a preferred embodiment of the present invention;

FIG. 6 is a circuit schematic diagram of a known amplifier used for simulation;

FIG. 7 is a circuit schematic diagram, similar to that of FIG. 6, of an amplifier according to a further embodiment of the present invention;

FIG. 8 is a graphical diagram illustrating the rise times of the circuits shown in FIGS. 6 and 7;

FIG. 9 is a graphical diagram illustrating the fall times of the circuits shown in FIGS. 6 and 7; and

FIG. 10 is a graphical diagram illustrating the bandwidths of the circuits shown in FIGS. 6 and 7.

Detailed Description of the Drawings

Thus, as shown in FIG. 1, part of a known electronic integrated circuit 10 includes a resistor 11 formed by a resistance layer of polycrystalline silicon. The poly resistor 11 is formed above an n-epitaxial layer 12 formed in a p-type substrate 13. An insulating layer 14 of oxide is provided between the resistance layer 11 and the epitaxial layer 12. An input signal V_{IN} (shown as a step voltage) is connected to one end of the resistor 11, while the other end is coupled to a ground reference potential GND. Since the epitaxial layer 12 is semiconductive, a parasitic capacitance, schematically shown as 15, is formed between the resistance layer 11 and the epitaxial layer 12. Similarly, a further parasitic capacitance, shown as 16, is formed across the p-n junction between the epitaxial layer 12 and the substrate 13, which is usually connected to an a.c. ground.

The circuit shown in the cross-sectional diagram of FIG. 1 can be represented by an equivalent circuit 20, as shown in FIG. 2. The poly resistor 11 (of FIG.1) is represented by distributed resistors 21, 22, 23 and 24, and the parasitic capacitances 15 and 16 are

represented by distributed capacitors 25, 26 and 27. When a step voltage V_{IN} is applied to one end of the distributed resistor at resistor 21, part of the high frequency current I of the signal is shunted to ground reference potential GND through capacitors 25, 26 and 27, as shown by arrow 28, thereby degrading both the bandwidth and linearity of the signal at high frequencies.

In accordance with one embodiment of the present invention, an electronic integrated circuit 30, as shown in FIG. 3, includes a resistor 31, formed by a resistance layer of polycrystalline silicon. As in the circuit described above with reference to FIG. 1, the poly resistor 31 is formed above an n- epitaxial layer 32 formed in a p-type substrate 33. As before, an insulating layer 34 of oxide is provided between the resistance layer 31 and the epitaxial layer 32. A first parasitic capacitance 35 is thus formed between the resistance layer 31 and the epitaxial layer 32 and a second parasitic capacitance is formed across the p-n junction between the epitaxial layer 32 and the substrate 33. It will, of course, be appreciated that further parasitic capacitances may well exist if further p-n junctions are formed if there are are further semiconductive layers forming the circuit. In this case, only one p-n junction parasitic capacitance is shown for simplicity.

In this embodiment, the insulating layer 34 is broken, by etching or in any other way, in order to allow areas of conductive material forming contacts 37 and 38 to contact the epitaxial layer 34 close to each end of the resistor 31. A cancellation signal V'_{IN} is applied via the contact 37 to the epitaxial layer close to the end of the resistor 31 where the input signal V_{IN} is applied to one end and contact 38 connects the epitaxial layer close to the other end of resistor 31 to ground reference potential GND. The cancellation signal V'_{IN} is duplicated from the input signal V_{IN} so that cancellation signal V'_{IN} is as similar to input signal V_{IN} as possible. Thus, when input signal V_{IN} is applied to resistor 31 and cancellation signal V'_{IN} is applied to the epitaxial layer 32, essentially similar voltages are on both sides of the parasitic capacitance 35, hence reducing the potential difference between them.

An equivalent circuit 40 to the above described integrated circuit 30 is shown in FIG. 4, where the poly resistor 31 is

represented by distributed resistors 41, 42, 43 and 44, the epitaxial layer 32 is represented by distributed resistors 48, 49, 50 and 51, the resistance-epitaxial parasitic capacitance 35 is represented by distributed capacitors 45, 46 and 47, and the p-n junction parasitic capacitance 36 is represented by distributed capacitors 52, 53 and 54. As a step voltage input signal V_{IN} is applied to one end of the first distributed resistor 41, the duplicated cancellation signal V'_{IN} is injected into the epitaxial layer 32 represented by distributed resistor 48 so that the signal underneath the poly resistor 31 in the epitaxial layer 32 tracks with the signal in the poly resistor 31, hence reducing the potential difference (dV) across the parasitic capacitance 35. Thus, as can be seen in FIG. 4, since the current is governed by the equation:

$$I = C\ (dV/dT)$$

for the same parasitic capacitance C, the current I, shunted to ground reference potential GND from the input signal V_{IN}, is reduced, as compared to the current I', due to a reduction in the voltage difference dV. The input signal V_{IN} is therefore not attenuated as much as the cancellation signal V'_{IN}, which is, of course, shunted by the parasitic capacitance 36 to ground reference potential GND. Alternatively, if the current I is maintained constant, for the same parasitic capacitance C, the difference in time dT is reduced due to a reduction in the voltage difference dV.

FIG. 5 shows a preferred embodiment of an amplifier 60 having an amplifying circuit 61 and an active cancellation circuit 62. The amplifying circuit 61 consists of an input stage formed by two NPN transistors 63 and 64 coupled between a pair of resistors 65 and 66 between a supply voltage rail V_{CC} and a ground reference rail GND, respectively. The input signal V_{IN} is input to the base of transistor 63 whose emitter is connected to the ground reference rail GND via the resistor 65, and whose collector is connected to the emitter of the common base transistor 64. The base of the transistor 64 is connected to a DC reference voltage V_{DC} and the collector is connected to the supply voltage rail V_{CC} via the resistor 66, which is the poly resistor 31 of FIG. 3. The collector of transistor 64 is further coupled to an emitter follower output stage formed by NPN transistor 67 and resistor 68 coupled between the emitter of the

transistor 67 and the ground reference rail GND. The collector of the transistor 67 is coupled to the supply voltage rail V_{CC} and the base of the transistor 67 is coupled to the collector of transistor 64, the junction between them being the dominant pole of the circuit, as shown by arrow 73. The output of the amplifier V_{OUT} is taken at the junction between the transistor 67 and the resistor 68.

The active cancellation circuit 62 consists of a duplication of the input stage of the amplifying circuit 61 and is formed by a pair of NPN transistors 69 and 70 and a resistor 71. Thus, the bases of transistors 69 and 70 are coupled to the bases of transistors 63 and 64, respectively, the emitter of transistor 69 is coupled via resistor 71 to the ground reference rail GND and the collector of transistor 69 is coupled to the emitter of transistor 70, The only difference between the active cancellation circuit 62 and the input stage of the amplifying circuit 61 is that the collector of transistor 70 is connected to the epitaxial layer (32 in FIG. 3) underneath resistor 66. Thus, the input signal at V_{IN} is duplicated using the active cancellation circuit 62 and the resulting signal is injected, as shown by arrow 72, into the epitaxial layer underneath the poly resistor 66 to achieve the results described above with reference to FIGS. 3 and 4.

Turning now to FIGS. 6 and 7, the benefits of using the active cancellation circuit can be demonstrated by comparing the results from two simulation circuits. Simulation circuit 74, shown in FIG. 6, is provided by an amplifier circuit without active cancellation, while simulation circuit 85, shown in FIG 7, is provided by an amplifier circuit with active cancellation. The simulation circuit 74 thus comprises an NPN transistor 75 having its emitter coupled via a current source 76 to a ground reference rail GND, to which the substrate 77 of the integrated resistor is also coupled, and its base coupled to a bias voltage source 78. The collector of transistor 75 is coupled to a supply voltage source 79 via a poly resistor represented, as before, by distributed resistors 80, 81 and 82 having a parasitic capacitance represented by distributed capacitors 83 and 84.

Simulation circuit 85 comprises the same elements as simulation circuit 74, which are labelled with the same reference

numbers, but also includes an active cancellation circuit formed by NPN transistor 86 having its emitter coupled via current source 87 to ground reference rail GND, its base coupled to the base of transistor 75 and its collector coupled to the epitaxial layer below the poly resistor. Again, the epitaxial layer is represented by distributed resistors 88, 89 and 90 having a parasitic capacitance represented by distributed capacitors 91 and 92.

The results of small and large signal analysis performed on the two simulation circuits 74 and 85 are shown in FIGS 8, 9 and 10. As can be seen in FIG. 8, there is a 28% improvement in rise times, from 360pSec to 259pS. A similar improvement can be seen in FIG. 9 for fall times, from 422pSec to 300pS for large signal step responses. Furthermore, there is a 33% improvement, from 900MHz to 1197MHz at -3dB bandwidth for small signal frequency responses, as is shown in FIG. 10.

It will be appreciated that although only a few particular embodiments of the invention have been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention. For example, it will be appreciated that, although the duplicated signal has been described as being injected only into the first epitaxial layer below the poly resistor, further injections of duplicated signals could be injected into further lower layers, if desired, in order to still further reduce the effects of parasitic capacitances.

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Claims

1. An electronic circuit on a semiconductor chip having a resistor integrated therein, the resistor being formed by a resistance layer formed over an insulating layer formed over a first cancellation layer, wherein the circuit has an input for receiving an ac signal, the resistor being coupled between the input and a reference voltage potential, and a duplicating circuit coupled to the input for duplicating the ac signal and for applying the duplicated signal to the first cancellation layer below the resistor so as to reduce parasitic capacitance between the resistance layer and the first cancellation layer.

2. An electronic circuit according to claim 1, further comprising at least one further cancellation layer below the first cancellation layer, wherein the duplicating circuit is arranged for applying the duplicated signal to the further cancellation layer(s) to further reduce the parasitic capacitance.

3. An electronic circuit according to either claim 1 or claim 2, wherein at least one of the first and/or further cancellation layers is a conductive layer.

4. An electronic circuit according to any one of claims 1, 2 or 3, wherein at least one of the first and/or further cancellation layers is a semiconductive layer.

5. An electronic circuit according to claim 4, wherein the semiconductive layer is formed of epitaxial material.

6. An electronic circuit according to claim 5, wherein the resistance layer is formed of polycrystalline silicon material.

7. An electronic circuit according to any preceding claim, wherein the electronic circuit includes an amplifying circuit having a transistor coupled to the resistor.

* C L M S *

8. An electronic circuit according to claim 7, wherein the duplicating circuit is similar to the amplifying circuit and has a transistor coupled to the cancellation layer.

9. A method of reducing the effects of parasitic capacitance of a resistor integrated in an electronic circuit on a semiconductor chip, the method comprising the steps of:

i) applying a signal across the resistor;

ii) duplicating the signal; and

iii) applying the duplicated signal to a cancellation layer formed in the semiconductor chip below the resistor so as to reduce the effects of parasitic capacitance between a layer of the semiconductor chip forming the resistor and the cancellation layer.

10. A method according to claim 9, wherein step (iii) comprises applying a voltage representing the signal to the cancellation layer below the resistor such that the voltage tracks the signal so that the potential difference between them is minimised.