

IMPROVEMENTS IN OR RELATING TO RANGEFINDERS
AND IMAGE SENSORS THEREFOR

5 The present invention relates to automatic
rangefinders and image sensors for use therein, and
more particularly to such rangefinders of the type
wherein a beam of light is projected on a scene to
form a spot of light on an object, and an array of
photosensors sense the location of the light spot in
10 an image of the scene to determine the distance to
the object in the scene.

Automatic rangefinders are known in which a
beam of light is projected upon an object in a scene
to form a spot of light on the object. An image of
the scene including the light spot, is formed on a
15 linear array of photosensors. The location of the
image of the light spot along the linear array is
determined and used as a function of the distance to
the object in the scene. Such ranging devices
are used, for example, in automatic focusing cameras.

20 The general arrangement of elements and mode
of operation of such a known ranging device will
be described with reference to FIG. 1. Means for
projecting a beam of light is shown, by way of
example, as a light emitting diode (LED) 10 and a
25 lens 12. The beam is projected along a path 14 to
form a spot of light on an object O_1 in a scene.
The scene is imaged by a second lens 16 onto a linear
array 17 of photosensors. The signals produced by
the photosensors are analyzed by control electronics
30 20 to determine the position of the light spot in the
scene and produce a signal 21 representing the distance
to the object.

As shown in FIG. 1, the apparent position of
the light spot in the scene is a function of distance
35 along light path 14 to the object. For an object
 O_1 located at a distance D_1 from the

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rangefinding device, the image of the light spot will fall on the array at a location S_1 . For an object O_2 at a further distance D_2 , the image of the spot will fall on the array at a location S_2 . By examining the output of the array 17, the control electronics 20 determines (for example, by comparing the outputs of the elements to determine that output which is a maximum) the location of the light spot in the scene and thereby the distance to the object.

When the ambient illumination is relatively bright, the scene itself, regardless of the light spot, will produce substantial modulation of the photosensor array. Under such circumstances, it may not be possible to determine the location of the light spot merely by examining the outputs of the photosensors. The effects of ambient scene light can be removed however by operating the sensor with the beam off and again with the beam on, and subtracting the signals produced thereby. The information in the difference signal is solely from the light spot. One way of accomplishing this subtraction is described in US-A-4274735. In US-A-4274735 there is described a device having a pair of memory capacitors associated with each photosensor in the array. The capacitors are selectively connectable to the photosensors by field effect transistor (FET) switches, and each pair is further connectable to an associated differential amplifier. In operation, a photosensor is first connected to one of the capacitors while the light beam is off. The photosensor is then connected to the other capacitor while the light beam is on. Both the capacitors are then connected to the differential amplifier to produce a signal free from background information. The signals are compared in an array of comparators to determine the location of the light

spot by sensing the largest difference signal produced by the array of differential amplifiers.

To effectively remove the relatively large background signal from the relatively small signal due to the light spot, each of the differential amplifiers must have very good common mode rejection. Furthermore, so that the amplifiers themselves do not introduce overwhelming pattern noise into the signals, they must be very closely matched. The need for a plurality of closely matched differential amplifiers exacts a high price on any attempt to increase the signal-to-noise ratio of the device. Furthermore, the use of an array of comparators to determine the maximum difference signal from the differential amplifiers complicates the signal processing circuitry.

There was a need, therefore, to simplify the signal processing electronics of the rangefinder while improving the signal-to-noise ratio achievable therein.

It is an object of the present invention to overcome the above problems.

According to the present invention there is provided a rangefinder having means for projecting a beam of light to form a spot of light on an object in a scene, an image sensor for sensing the light from a scene and producing signals representative thereof, and means responsive to the signals for detecting the position of the spot of light in the scene to

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determine the distance to the object, said
rangefinder including means for removing from the
signals produced by the image sensor components other
than those derived from the light in the beam, by
5 sensing the scene with the light beam turned on and
again with the light beam turned off, and forming
difference signals from the photosignals produced
thereby, said image sensor including 1) an array of
photosensors for producing signals related to the
10 amplitude of light on them, respectively, 2) first
and second analog shift registers, adjacent the array
of photosensors, for receiving a plurality of signals
in parallel and shifting the signals serially to an
output location, 3) first and second transfer gates
15 located respectively between the array of
photosensors and the first and second analog shift
registers, for selectively transferring the
photosignals produced by the photosensors into the
respective shift registers, whereby, the signals
20 produced with the light beam turned on are
transferred to the first shift register, and the
signals produced with the light beam turned off are
transferred to the second shift register, and the
shift registers are read out simultaneously to
25 deliver the signals to a differencing circuit.

The present invention will now be described,
by way of example, with reference to Figs. 2 to 9 of
the accompanying drawings, in which:-

FIG. 2 is a schematic diagram of an image

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sensor, including a photosensor array and a pair of analog shift registers, according to one aspect of the present invention;

5 FIG. 3 is a partial plan view showing the electrode and channel structure of the image sensor shown in FIG. 2;

10 FIG. 4 is a schematic cross-sectional view and potential diagram of the image sensor showing the photosensor array and readout shift registers taken along line IV-IV in FIG. 3;

15 FIG. 5 is a schematic block diagram showing the signal processing and control electronics of a rangefinder according to another aspect of the present invention;

20 FIG. 6 is an electrical circuit schematic diagram showing the signal processing electronics for differencing and peak detecting;

 FIG. 7 is a flow chart showing the general operation of the rangefinder of Fig. 5; and

25 FIGS. 8 and 9 are timing diagrams useful in explaining the operation of the rangefinder of Fig. 5.

 FIG. 2 shows a solid state image sensor 18 according to the present invention. The image sensor 18 includes a linear array of photosensors, in the present embodiment photodiodes 22, and a pair of charge coupled device (CCD) shift registers 24 and 24'. Corresponding elements of the two CCD shift registers are given the same reference numerals and the elements of register 24' will be distinguished by the use of primes ('). A transfer gate 26 between the array of photodiodes 22 and CCD shift register 24 is actuatable for transferring charge (in the direction of arrows X) from the photodiodes 22 into the shift register 24. A second transfer gate 26' between the array of photodiodes 22 and the second shift register 24' is actuatable for transferring charge (in the

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direction of arrows X') from the photodiodes 22 to the second shift register 24'. In this embodiment, the CCD shift registers are of the buried channel variety to maximize their transfer efficiency and hence the signal-to-noise ratio of the device, and the transfer channels created by the transfer gates 26 and 26' are surface channels thereby enabling a single low voltage power supply (e.g. 5 Volts) to be employed to power the device.

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10 The signals in the CCD shift register 24 are shifted serially in the direction of arrow Y to an output diode 28 by applying four-phase clock signals ϕ_{1-4} to the transfer electrodes of the CCD shift register. The signals are detected at the output diode 28 by a preamplifier 30 which is specially configured, as described below, to operate from the single low voltage power supply.

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20 FIG. 3 is a partial plan view illustrating the electrode and channel structures of the linear photodiode array and associated CCD readout shift registers 24, 24'. The buried channels for the CCD shift registers 24, 24', comprising for example n-type regions 32, 32' respectively in a p-type silicon substrate, are shown by dotted lines. Channel stopping regions 34, 34' confining the respective outer edges of the CCD shift registers 24, 24' and comprising, for example, (p+)-type regions under a thickened field oxide, are shown by chain lines. The photodiodes 22 are formed by (n+)-type diffusions in the areas defined between dumbbell-shaped channel stopping regions 36 in the centre of the device.

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35 Two levels of polysilicon overlying the channels define the electrode structure of the device. A first level of polysilicon respectively defines the phase-2 electrodes (38, 38') and phase-4 electrodes (40, 40') of the CCD shift registers 24 and 24'.

A second level of polysilicon respectively defines the phase-1 electrodes (42, 42') and phase-3 electrodes (44, 44') of the CCD shift registers 24 and 24' and the transfer gates 26 and 26'. The phase-2 electrodes 38, 38' and the transfer gates 26, 26' form surface channels that couple the photodiodes 22 to the CCD shift registers 24, 24'.

FIG. 4 is a partial, cross-sectional view of the image sensor 18 taken along line IV-IV in FIG. 3, showing the channel structure of the image sensor 18.

Image sensor 18 is formed in a p-type silicon substrate 46. The CCD buried channels are defined by n-type regions 32. The photodiodes 22 are formed by (n⁺)-type regions. A layer 48 of silicon dioxide overlies the doped regions of the device. Chain line 50 depicts the potential profile across the device when 0 volts is applied to the transfer gates 26 and 26' and 5 volts is applied to the phase-2 electrodes 38 and 38'. Potential barriers 52 and 52' keep charge generated in the photodiode from flowing into either of the CCD shift registers. If 5 volts is applied to either transfer gate 26 or 26', the potential barrier 52 or 52' thereunder is lowered to the position shown by dotted lines 54 or 54' respectively and allows the charge in the photodiode to flow into the respective CCD shift register beneath the phase-2 electrode via the surface channel created thereunder. When the 5-volt potential is removed from the transfer gate and the phase-2 electrode 38 or 38', the potential well thereunder collapses as shown by broken lines 56 and 56'. Charge in the shift register is moved in a direction perpendicular to the plane of the drawing by pulsing the four-phase transfer electrodes in the conventional manner for moving charge in a CCD shift

register. The use of a surface channel to couple the photodiode 22 with the buried channel CCD shift register enables the sensor to operate at a single low voltage (e.g. 5 volts), thereby simplifying the power supply requirements for the device.

Referring now to FIG. 5, overall control of the rangefinder is provided by a programmed microprocessor 100 via conventional driver circuits 102. The microprocessor 100 is supplied with timing signals from a clock circuit 104 and with power via a main power switch 106 from a battery 108. Four-phase clock signals ϕ_1 -.4. and transfer signals T_1 and T_2 are supplied to the image sensor 18 from the driver circuits 102 under control of microprocessor 100 to produce output signals from the CCD shift registers of the sensor 18. The signals from the CCD shift registers are supplied to a differencing circuit 110. Difference signals produced by the differencing circuit 110 are supplied to a peak detector circuit 114. The output of the peak detector circuit is supplied to a latch circuit 116. Latch circuit 116 is connected to the outputs of a digital counter 118. Counter 118 receives a reset signal R and a timing signal ϕ_T having the same frequency as the four-phase clock signals ϕ_1 -.4.. The output of the latch circuit 116 is supplied to an input port of microprocessor 100.

The driver circuits 102 also power LED 119 and an output device 120 such as a range display or a range servo. LED 119 preferably emits infrared light.

FIG. 6 is a more detailed circuit schematic of the signal processing electronics shown in FIG. 5. A portion of the CCD shift registers 24 and 24' including output gates 122 and 122' and output diodes 28 and 28' is shown.

The preamplifier 30 is an on-chip, sense and

reset amplifier including a sense FET 124 and a reset FET 126. The sense FET 124 is a surface channel device and the reset FET 126 is a buried channel device, so that a single low voltage power supply can be used to power the apparatus. A buried channel FET 128 is connected between the drain of the FET 124 and earth in a constant current configuration for converting the sensed charge on diode 28 to a voltage at node A.

The differencing circuit 110, comprises multiplexing FETs 130 and 132 for sampling the outputs at nodes A and A', a detection capacitor 134, a clamping FET switch 136, and an amplifier 138. Differencing circuit 110 includes a sample and hold portion comprising a sampling FET 140, a storage capacitor 142 and an amplifier 144.

The peak detector circuit 114 comprises a differential amplifier 146, a reference capacitor 148, a sampling FET switch 150, and a timing FET switch 152. The peak detector circuit 114 contains a threshold setting portion comprising a preset FET switch 154 connecting capacitor 148 to earth, and a threshold setting FET switch 156 connecting the 5 volt power supply to capacitor 148 through a resistor 158.

The operation of the rangefinder will now be described with reference to FIGS. 7, 8 and 9. FIG. 7 is a flow chart showing a control program for the microprocessor 100 (see FIG. 5). To begin, for example upon closure of main power switch 106 at time t_0 , (see FIG. 8) the microprocessor 100 initializes the photosensor array by transferring any accumulated charge from photodiodes 22 into shift register 24 by applying a T_1 transfer pulse to transfer gate 26, (FIG. 8a) while phase two (Φ_2) of the four-phase clock signals is held high, and then applying the

four-phase clock signals ϕ_{1-4} to both CCD shift registers to empty any residual charge therein (FIG. 8c). Meanwhile, at time t_1 the microprocessor 100 executes a time delay τ_1 to accumulate background charge, due to ambient scene illumination, in the photosensor array. After time delay τ_1 , at time t_2 , the background charge is transferred to the first CCD shift register 24 by holding ϕ_2 high and again pulsing transfer gate 26 (see FIGS. 8a and c).

Next, at time t_3 , the microprocessor 100 turns on LED 119, while ϕ_2 is held high (see FIGS. 8c and 8d). LED 119 is kept on for a period τ_1 , during which the signal processing circuitry is initialized to set the threshold of the peak detector circuit 114. FET switch 154 (see FIG. 6) is turned on momentarily by generating a ϕ_{preset} pulse (see FIG. 8e) to earth capacitor 148. Then, FET switch 156 is turned on by a pulse ϕ_{TH} for a period τ_2 (See FIG. 8f) to charge capacitor 148 to a value determined by the time constant of resistor 158 and capacitor 148. At time t_4 , the LED 10 is turned off. The background plus LED photosignals generated by the sensor array are transferred to the second CCD shift register 24' by applying a pulse T_2 to transfer gate 26' (see FIG. 8b). Both CCD shift registers 24, 24' are then read out simultaneously to generate the range signal by applying the four-phase clock signals ϕ_{1-4} to the four-phase transfer electrodes 38, 38', 40, 40', 42, 42', 44, and 44' (see FIG. 8c).

Processing of the signals from the CCD's will now be described with reference to FIG. 9. The four-phase clock signals ϕ_{1-4} are shown in FIGS. 9a-d. While the signal charge resides under the phase-3 and phase-4 electrodes, 44, 44' and 40, 40' respectively, (ϕ_3 and ϕ_4 simultaneously high)

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a reset pulse ϕ_R is applied to reset FETs 126 and 126' to prepare the output diodes 28, 28' to receive the signal charge. At this point, the outputs A and A' of the CCD shift registers go to a high level (200 in FIGS. 9f and 9g). When the phase-3 transfer gate goes low, some of the signal charge spills over the output gates onto the output diode, and the outputs go to the intermediate level 202 in FIGS. 9f and 9g. Finally, when the voltage on the phase-4 transfer gate goes low, all the signal charge is moved to the output diodes 28 and 28' and the output signal at A and A' go to their final signal levels 204 as shown in FIGS. 9f and 9g.

During an initial portion of the period that the final signal levels are present at nodes A and A', a pulse ϕ_{E1} is applied to the sampling, multiplexing FET 130, thereby storing the background level present at node A on capacitor 134 (see FIG. 9h). During the ϕ_{E1} pulse, a pulse ϕ_{CL} is applied to clamping FET switch 136 to establish the voltage present at node A as a reference on capacitor 134. During a later portion of the period that the final signal level is present, a pulse ϕ_{E2} is applied to sampling, multiplexing FET 132. The resulting voltage on the capacitor 134 is the difference between the "background" signal and the "background plus the LED" signal. The output at node C of amplifier 138 follows this difference as shown in FIG. 9k. The difference level 206 is sampled and held on the output of amplifier 144 at node D by pulsing FET 140 with a sampling pulse $\phi_{S/H}$ (see FIG. 9l).

The voltage at node D is a step-wise smooth curve representing the successive values of the difference signal (see FIG. 9m). Differential amplifier 146 compares the first sample with a threshold value V_{TH} (see FIG. 9m) stored on

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-12-

capacitor 148. If the sampled value is less than the threshold value, the output of amplifier 146 at node E remains low, however if the sampled value exceeds the threshold value, the output at node E goes high. At a point during the sample period, a sampling signal ϕ_s (see FIG. 9n) is applied to timing FET switch 152. If the voltage at node E is low at this time, the low value will be applied to the gate of sampling FET 150 and will have no effect upon the state of the circuit. If, however, the voltage at node E is high, the high value will be applied to the gate of FET switch 150, thereby applying the new higher reference voltage to capacitor 148. The new reference value is equal to the input at node D thereby causing the output at node E of differential amplifier 146 to go low (see FIG. 9o). This process continues, producing a pulse at node E each time a new greater difference signal is received from the difference circuit 110.

At the start of the sequence, counter 118 is initialized. Each time a new charge packet is read from the CCD shift registers, counter 118 is advanced (see FIG. 5). The pulse train produced by the peak detector at node E is applied to latch circuit 116 which latches the output of counter 118 whenever a new pulse is produced by the peak detector. After all the charge packets in the CCD shift registers have been read out, the count held by latch circuit 116 is indicative of the location of the sensor element having the greatest illumination from the LED above the threshold level. At this point, the microprocessor 100 retrieves the range data from the latch circuit 116 by interrogating its input port.

The range data are then used in known manner to drive an output device such as a range display or a range servo.



Thus a rangefinding device has been disclosed having an improved image sensor and simplified signal processing electronics affording improved signal-to-noise ratio and capable of being
5 operated from a single low voltage power supply, thereby simplifying the power supply requirements of the device.

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CLAIMS:

1. A rangefinder having means for projecting a beam of light to form a spot of light on an object in a scene, an image sensor for sensing the light from a scene and producing signals representative thereof, and means responsive to the signals for detecting the position of the spot of light in the scene to determine the distance to the object, said rangefinder including means for removing from the signals produced by the image sensor components other than those derived from the light in the beam, by sensing the scene with the light beam turned on and again with the light beam turned off, and forming difference signals from the photosignals produced thereby, said image sensor including 1) an array of photosensors for producing signals related to the amplitude of light on them, respectively, 2) first and second analog shift registers, adjacent the array of photosensors, for receiving a plurality of signals in parallel and shifting the signals serially to an output location, 3) first and second transfer gates located respectively between the array of photosensors and the first and second analog shift registers, for selectively transferring the photosignals produced by the photosensors into the respective shift registers, whereby, the signals produced with the light beam turned on are transferred to the first shift register, and the signals produced with the light beam turned off are transferred to the second shift register, and the shift registers are read out simultaneously to deliver the signals to a differencing circuit.

2. A rangefinder as claimed in Claim 1, wherein the photosensors are photodiodes, said analog shift registers are buried channel charge coupled device shift registers, and said transfer gates are actuatable for forming surface channels between said



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photodiodes and said buried channel CCD shift registers, whereby the image sensor may be operated by a single low voltage power supply.

3. A rangefinder as claimed in Claim 2,
5 further comprising sense and reset FET preamplifiers associated with each of said CCD shift registers, wherein the reset FET of said preamplifier is a buried channel FET and the sense FET is a surface
10 channel FET, whereby said sense and reset preamplifiers are operated by the single low voltage power supply.

4. A rangefinder as claimed in Claim 1
substantially as hereinbefore described with
reference to Figs. 2 to 9 of the accompanying
15 drawings.

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