

PROCESS FOR FABRICATING TWO DIFFERENT GATE DIELECTRIC
THICKNESSES USING A POLYSILICON MASK AND CHEMICAL MECHANICAL
POLISHING (CMP) PLANARIZATION

ABSTRACT

A method of forming a semiconductor device, including forming a substrate with a memory array region (201) and a logic device region (101), growing a thick gate dielectric (102) over the substrate, forming a gate stack, including a first polysilicon layer (103), over the thick gate dielectric (102) for the memory array region (201), forming a thin gate dielectric (200) on the substrate over the logic device region (101), wherein layers of the gate stack in the memory array region (201) protect the thick gate oxide (102) during the forming of the thin gate dielectric (200), forming a second polysilicon layer (300) for the gate stack in the logic device region (101), to produce a resulting structure, wherein a thickness of the second polysilicon layer (300) is at least as thick as the gate stack in the memory array region (201), planarizing the structure using chemical mechanical polishing (CMP), and patterning the gate stacks in said memory array region (201) and the logic device region (101).

FIG 4

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