

1113.211



PATENT SPECIFICATION

DRAWINGS ATTACHED

1113.211

Date of Application and filing Complete Specification: 14 May, 1965.
No. 20563/65.

Application made in United States of America (No. 371674) on 1 June, 1964.
Complete Specification Published: 8 May, 1968.

© Crown Copyright 1968.

Index at acceptance: —H1 K(1C1, 1CX, 2S2P, 2S5, 2S19, 2S20, 2S21, 2S23, 3E1D, 3E1M, 3J, 3P2, 4C9A, 4C14, 4C21, 4C23, 4F17, 4F20, 5C5, 9M)

Int. Cl.: —H 01 11/14

COMPLETE SPECIFICATION

Field Effect Transistor with Insulated-gate

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be performed, to be particularly described in and by the following statement:—

This invention relates to insulated-gate field effect transistors.

Previous insulated-gate field effect transistors comprise generally a channel, a source and a drain connected to the channel and defining the ends of a drain current path through the channel, and a gate overlying and closely spaced from the channel by a thin insulator layer. Such devices are used as active elements in electronic circuits; for example, in amplifying, switching, or oscillating circuits.

An important characteristic of this device is its gain characteristic which is a plot of the transconductance, g_m , as a function of the gate voltage, V_g . The transconductance, g_m , is defined as the ratio of the differential change of drain current δI_D through the channel (between source and drain) to the differential change of gate voltage δV_g at constant drain voltage V_D . The pinch off voltage V_{po} of the device is the gate voltage at which the drain current approaches zero.

Previous insulated-gate field effect transistors exhibit a gain characteristic with a sharp cutoff. By sharp cut-off is meant that the transconductance drops sharply as the gate voltage changes in the proper sense to reduce the drain current. A gain characteristic with a sharp cutoff is desirable in some applications; for example, in switching circuits. However, in other applications, for example, in

automatic gain controlled amplifying circuits, a more desirable gain characteristic is one having a remote cutoff.

By remote cutoff is meant that there are progressively smaller reductions in transconductance (and drain current) for fixed changes in gate voltage which drive the device to conduct smaller drain currents. Ideally, a gain characteristic having a remote cutoff is asymptotic with the value $g_m=0$ and the gate voltage never completely pinches off the drain current. But, in practice, this is only approximated. As used herein, therefore, a gain characteristic having a remote cutoff may either be asymptotic or approximately asymptotic with the value $g_m=0$.

An object of this invention is to provide a new and improved insulated-gate field effect transistor.

According to the invention we provide an insulator-gate field effect transistor having drain current flow in a plurality of parts which have different pinch off voltages transversely across the gate, thereby obtaining a remote cut-off characteristic, said remote cut-off being obtained by a lateral charge in one or more of: the thickness of the insulator, the thickness of the channel under the gate of the transistor, the dielectric constant of the insulator, the dielectric constant of the channel, or the charge carrier density in the channel. The transistor has a remote cutoff gain characteristic. In the accompanying drawings:

FIGURES 1 and 2 are respectively perspective and sectional views of a first embodiment of the invention having an insulator which is stepped laterally;

FIGURE 3 is a curve illustrating a typical gain characteristic of the embodiment of FIGURE 1;

FIGURES 4 and 5 are respectively perspective and sectional views of a second em-

[Price 4s. 6d.]

SEE ERRATA SHEET ATTACHED



bodiment of the invention having an insulator with a laterally tapered thickness,

FIGURES 6 and 7 are respectively perspective and sectional views of a third embodiment of the invention having an insulator with a laterally stepped dielectric constant,

FIGURE 8 is a sectional view through the channel of the fourth embodiment of the invention having an insulator with a laterally tapered dielectric constant,

FIGURES 9 and 10 are sectional views of a fifth embodiment of the invention having a channel with a laterally stepped dielectric constant,

FIGURE 11 is a sectional view through the channel of a sixth embodiment of the invention having a channel with a laterally tapered dielectric constant,

FIGURE 12 is a sectional view through the channel of a seventh embodiment of the invention having a channel whose conductivity is tapered laterally, and

FIGURE 13 is a sectional view through the channel of an eighth embodiment of the invention illustrating that several lateral variations in structure may be used in combination.

Similar reference numerals are used for similar structures throughout the drawings.

Previous insulated-gate field effect transistors are substantially uniform in structure in the lateral direction, i.e., transversely and along the gate and, as a result, exhibit a gain characteristic with a sharp cutoff. Consequently, the prior art considers the drain current to flow in a single path; or to flow in a plurality of parallel paths all of which have substantially the same pinch off voltage. The invention, however, provides a unitary structure in which the drain current flows in a plurality of paths which have different pinch off voltages. Thus, in some respects, the structure behaves as several field effect transistors, or sometimes as a continuous spectrum of field effect transistors, with different pinch off voltages all connected in parallel; that is, with their sources connected together and their drains connected together, and in the embodiments herein described, with the gates connected together.

The invention will be described for devices having an N-type channel. However, devices having a P-type channel are also part of the invention. Generally, the same analysis and circuits apply to devices having a P-type channel, except that all polarities are reversed.

FIGURES 1 and 2 illustrate a first embodiment 21 of the invention having an insulator with a stepped thickness in the lateral direction. The device 21 includes a semiconductor body 23 of resistive P-type silicon, and a source 25 and a drain 27 of conducting N-type silicon in spaced locations in the body 23. An insulator 29 overlies the region of the body 23 between the source 25 and the

drain 27, which region is referred to as the channel 31.

The channel 31 is considered to be N-type because the drain currents are electron currents. The channel may have an excess of electrons with no gate voltage applied, or the excess of electrons may be induced in the channel by applying a positive gate voltage. The insulator 29 is preferably of silicon oxide although other insulators may be used.

The insulator 29 has three different thicknesses or steps 29a, 29b and 29c. The insulator 29 is thinnest (portion 29a) over one side of the channel 31 from source 25 to drain 27, thickest (portion 29c) over the other side of the channel 31 from source 25 to drain 27, and of intermediate thickness (portion 29b) over the central portion of the channel 31 from source 25 to drain 27.

A gate 33, preferably of metal, rests on the insulator 29 which spaces the gate 33 from the channel 31. The gate may lie over the entire surface of the insulator 29 extending between the source 25 and the drain 27. It is preferred, as shown in FIGURE 1, that the gate 33 extend over only part of the insulator 29, from opposite the source 25 over about two-thirds of the distance toward the drain 27. A low resistance source electrode 35, preferably of metal, contacts the source 25 and a low resistance drain electrode 37, preferably of metal, contacts the drain 27.

The first embodiment 21 may be operated with a circuit 39 which comprises a conductor 41 connecting the source electrode 35 to ground or reference potential 43. Connected between the gate 33 and the source electrode 35 by means of a gate conductor 45 is a gate bias source 47 and a signal source 49 connected in series. A drain conductor 51 connects the drain electrode 37 to ground through a source 53 and a load resistor 55 connected in series. The output signal of the device may be monitored across the load resistor 55 at terminals 57. An amplified replica of a signal applied to the gate 33 from the signal source 49 appears across the terminals 57. The polarity of the biases shown in FIGURE 1 are for operating a device 21 having an N-type channel.

FIGURE 3 illustrates a gain curve 59 for the embodiment illustrated in FIGURE 1. The right side of curve 59 is linear as viewed in FIGURE 3 and at the left side, the curve exhibits a remote cutoff. Upon analysis, the curve 59 appears to be approximately the sum of the three curves 59a, 59b and 59c, which appear to approximate the gain curves of three devices of identical structure except for the three steps 29a, 29b and 29c, respectively of the insulator thickness, and having channels one-third the total width of the channel of the transistor illustrated in FIGURES 1 and 2.

Thus, by this analysis, the embodiment 21



has a single channel with effectively three drain current paths; each path having a different pinch off voltage and consequently a different gain characteristic. The additive effect of the three drain current paths is to provide a remote cutoff portion to the gain composite curve.

As shown in FIGURE 3, the component gain curves 59a, 59b and 59c all intersect at $V_g=0$. This special case holds where the component paths are identical except for the respective insulator thicknesses. However, the component gain curves may have differing slopes and intersection point which result from physical differences in the component paths. The transconductance g_m of each component path may be described qualitatively by the following relationship:

$$g_m = n_0 e \mu \left(\frac{W\lambda}{L} \right) + \left(\frac{\epsilon_{ox}}{s} \right) \left(\frac{W}{L} \right) \mu V_g$$

where:

n_0 is the initial free carrier density in the channel

e is a unit electronic charge

μ is the mobility of majority carriers in the channel

ϵ_{ox} is the dielectric constant of the insulator

s is the thickness of the insulator

L is the length of the channel under the gate in the direction from source to drain

W is the width of the channel

λ is the thickness of the channel

It follows that different component gain curves can be provided with changes in one or more of the parameters that appear in only one of the two terms on the right side of the equation. It also follows that changes in any of the parameters that appear in only one of these two terms may be used to impart a remote cutoff to the gain characteristic. Thus, the device may have lateral changes in thickness s , or dielectric constant ϵ_{ox} of the insulator, carrier density n_0 , or thickness λ of the channel.

Although not shown in the equation, lateral changes in the dielectric constant of the channel ϵ_{ch} may also be used to produce the remote cutoff. In the usual case, where the insulator is much thicker than the channel, this effect is relatively small. However, a greater effect is produced when the insulator thickness s is smaller relative to the channel thickness λ , or where the dielectric constant of the insulator ϵ_{ox} is much greater than the dielectric constants ϵ_{ch} of the channel.

The lateral direction, or laterally, as used herein, is the direction transverse to the drain current paths and along the gate. The transistor has a plurality of drain current paths with differing predetermined pinch off voltages along the gate transversely to the path, thus

enabling the gain characteristic of the device to have a remote cutoff.

The circuit 39 illustrated in FIGURE 1 is illustrative of circuits generally that are useful. Other circuits may be used to operate one or more embodiments of the invention. The circuit may be an amplifier of controllable gain in a radio frequency receiver wherein automatic gain control voltage derived as a function of received signal strength is applied to the gate of the transistor. As shown in FIGURE 1, the signal source 49 may provide a radio frequency signal, and the bias source 47 may provide an automatic gain control voltage. Generally, the sources 47 and 49 each may provide a signal d.c., low frequency a.c., or high frequency a.c. Thus, the device and circuit illustrated in FIGURE 1 may function as a mixer.

As shown in FIGURE 1, the body of semiconductor material 23 is floating (not connected to the circuit). Although not shown, the body 23 may also be biased, either with a d.c. or with an a.c. signal to provide an auxiliary signal input to the device. Also, if the body 23 is thin and relatively resistive, an auxiliary gate electrode (not shown) may be positioned adjacent the body 23 opposite the gate 33 to provide an auxiliary signal input or output.

FIGURES 4 and 5 illustrate a second embodiment 61 of the invention similar to the first embodiment except that the insulator 29 is wedge-shaped or tapered, instead of stepped. The wedge shape provides a continuous change in thickness from one side of the channel to the other, that is, transverse to the direction of drain current flow. This structure may be considered to have an infinite number of steps, which control an infinite number (a continuous spectrum) of drain current paths which vary smoothly over a finite range of pinch-off voltages.

FIGURES 6 and 7 illustrate a third embodiment 63 which is similar to the first embodiment illustrated in FIGURE 1 except that the insulator 29 is replaced with an insulator 65 of uniform thickness. Insulator 65 includes three different laterally-positioned regions 65a, 65b and 65c, having different dielectric constants. That is, the dielectric constant of the composite insulator 65 is stepped in a direction transverse to the direction of drain current flow in the channel 31.

The insulator 65a over one side of the channel 31 (the left side as viewed in FIGURE 7) has the lowest dielectric constant. The insulator 65c over the other side of the channel 31 from source 25 to drain 27 (the right side as viewed in FIGURE 7) has the highest dielectric constant. The insulator 65b over the central portion of the channel from source to drain has an intermediate dielectric constant between that of insulators 65a and 65c.

When a gate voltage is applied to the gate 33, the portion of the transistor having the insulator portion 65c will pinch off first. The portion 65a having the insulator of lowest dielectric constant will pinch off last. The difference in dielectric constants in the insulator 65 may be obtained by successively depositing different insulator materials upon the channel 31.

FIGURE 8 illustrates a fourth embodiment which is similar to the third embodiment illustrated in FIGURE 6 except that the dielectric constant of the insulator is tapered in a direction transverse to the direction of drain current flow, instead of being stepped. In this embodiment, the dielectric constant of the insulator 65 changes continuously from one side of the channel 31 to the other providing a continuously changing pinch off voltage across the channel over a finite voltage range.

FIGURES 9 and 10 illustrate a fifth embodiment which is similar to the first embodiment of FIGURE 1 except that the insulator 29 has a uniform thickness and dielectric constant, and the channel 31 is comprised of three different regions 31a, 31b and 31c, each having different dielectric constants. The dielectric constant of the channel therefore is stepped in the sense that the dielectric constant transverse to the direction of drain current flow changes discontinuously by discrete amounts for each of the channel portions.

One side of the channel 31a (the left side as viewed in FIGURE 10) has the lowest dielectric constant. The other side of the channel 31c (the right side as viewed in FIGURE 10) has the highest dielectric constant. The central portion 31b has an intermediate dielectric constant.

When an increasing gate voltage is applied to the gate electrode 33, the portion of the transistor having the channel 31c with the highest dielectric constant pinches off first, and the portion having the channel 31a of lowest dielectric constant, pinches off last. The difference in dielectric constants in the channel 31 may be provided by using different semiconductor materials, for example, deposited epitaxially in successive steps upon a common semiconductor support.

FIGURE 11 illustrates a sixth embodiment which is similar to the fifth embodiment shown in FIGURE 9, except that the dielectric constant of the channel 29 is tapered instead of being stepped in a direction transverse to the direction of drain current flow. In this embodiment, the dielectric constant of the channel changes continuously from one side of the channel to the other providing a continuous change in pinch-off voltage across the channel 31 over a finite voltage range. The variable dielectric constant channel may be provided as hereinafter described.

FIGURE 12 illustrates a seventh embodiment which is similar to the fifth embodiment

illustrated in FIGURE 9 except that the conductivity, instead of the dielectric constant of the channel 31 is either stepped or tapered from side to side laterally across the channel. That is, the conductivity of the channel varies either in a step-wise or in a continuous manner. The higher the conductivity of the channel, the higher is the transconductance at $V_g=0$.

The conductivity in the channel may be modified by changing the impurity concentration laterally across the channel in a manner known in the art. One method applicable to thin film evaporated transistors is to use a mask protecting part of the channel during a gas discharge step. This increases the conductivity of the unmasked portion of the channel.

Another method applicable to silicon transistors is to cover the entire channel with doped oxide deposited from silane, and then to remove it over part of the channel. The entire channel is then covered with another doped oxide of different doping concentration and the structure is heated to diffuse impurities from the doped oxide into the channel.

Combinations of the foregoing techniques may be used to provide other embodiments of the invention. FIGURE 13 illustrates an eighth embodiment of the invention which has a structure similar to that of the first embodiment illustrated in FIGURE 1 except that the insulator 29 has two steps in thickness. Each step further has two portions with different dielectric constants. Thus, the insulator 29 comprises four portions 29a, 29b, 29c and 29d, each having different thicknesses and/or different dielectric constants.

In addition, the channel is divided into five portions 31a, 31b, 31d, 31f and 31h, each having different conductivities. The channel portions are offset physically from the portions of different dielectric constant in the insulator. Such a structure comprises effectively eight current paths having different pinch-off voltages. That is, channel 31b has a portion 31c which is adjacent insulator 29b. Channel 31d is not only adjacent insulator 29b but it also has a portion 31c adjacent insulator 29c. Similarly channel 31f has a portion adjacent insulator 29d.

The devices incorporating the invention include structures having channels constituted of a single crystal such as silicon produced directly in a single crystal body or produced epitaxially on a single crystal body. For such single crystal structures, the insulator may be deposited as from a vapor phase, or, in some materials such as silicon, may be grown in situ as by thermal oxidation.

The embodiments of the invention include also structures having a channel of polycrystalline material, such as cadmium sulfide, cadmium selenide, or tellurium, preferably produced by deposition from a vapor. For such polycrystalline structures, the insulator

is preferably produced by deposition from a vapor. Also, in devices with polycrystalline channels, the channel material may be deposited upon the insulator or the insulator may be deposited upon the channel.

The fabrication techniques for insulated-gate field effect transistors are similar to those used to produce planar bipolar transistors and integrated monolithic devices. Impurity diffusion techniques may be used, and geometry may be controlled by precision masking and photolithographic techniques.

A fabrication schedule for a stepped oxide remote cutoff channel device may be as follows: A lightly doped P-type silicon wafer, about one inch in diameter and 0.007 inch thick, is polished on one side and the surface heavily oxidized in a furnace at about 900° C. containing a steam atmosphere to produce an oxide surface coating. The oxide surface coating is then etched away in selected areas defined by masking, using photolithographic techniques.

Next, the wafer is heated at about 1050° C. for 10 minutes in an atmosphere containing an N-type dopant, such as phosphorus, thereby forming source and drain regions which are not covered by the oxide. The entire remaining oxide layer is then removed. Then, the wafer is heated at about 900° C. in dry oxygen gas for about five hours until another, second oxide layer about 4000 Å thick is formed on the surface of the wafer. The wafer is cooled to room temperature and then reheated at about 400° C. in dry hydrogen gas for about 5 minutes to produce a desired channel characteristic. The second oxide layer is selectively removed over the source and drain regions as by etching.

The oxide layer over the channel is now stepped by using a series of photolithographic and partial etching operations designed to reduce the oxide thickness. The number of these operations depends upon the requisite number of oxide steps. In this example, four steps are produced having thicknesses of about 1000, 2000, 3000 and 4000 Å. Metal is evaporated over the entire wafer, and then selectively etched from all areas of the wafer except over the source region, the drain region and the stepped oxide. The metal over the stepped oxide between the source region and the drain region constitutes the gate of the device. The wafer is then diced into separate units or arrays. The units or arrays are mounted on a suitable support and leads are bonded thereto, as by thermal compression. After bonding, the units are encapsulated.

Another method for obtaining the stepped oxide employs photolithographic techniques to fully, instead of partially, remove the oxide. The oxide growth is then reheated. The areas with oxide already present grow thicker and the stripped regions grow to a thinner layer.

A method for obtaining a continuously

tapered oxide is to selectively deposit the insulator as by vapor deposition. By this technique, an aperture mask is moved slowly during the deposition laterally along the channel. The tapering of the oxide is controlled by the movement of the aperture mask and the rate of deposition. The thickness may be profiled by adjusting the rate of movement of the mask.

The fabrication of gate structures with a tapered or stepped dielectric constant in the insulator may be done by vapor deposition using more than one source, depositing different materials in sequence through a repositioned mask. One may, for example, use three sources with three different insulators with three dielectric constants corresponding to 65a, 65b, and 65c in FIGURE 7. After depositing the insulator corresponding to 65a through a suitable mask, the mask is moved laterally to the position corresponding to 65b and the insulator corresponding to 65b is deposited. By repeating the procedure the third insulator corresponding to 65c is laid down. By gradually moving the mask while gradually shifting from one insulator to the other, an insulator layer with tapered dielectric constant can be obtained.

For fabrication of structures with a tapered or stepped dielectric constant in the semiconductor, the same procedure may be used with three sources of three different semiconductors in combination with a movable mask.

WHAT WE CLAIM IS:—

1. An insulated-gate field effect transistor having drain current flow in a plurality of paths which have different pinch off voltages transversely across the gate, thereby obtaining a remote cut-off characteristic, said remote cut-off being obtained by a lateral change in one or more of the thickness of the insulator, the thickness of the channel under the gate of the transistor, the dielectric constant of the insulator, the dielectric constant of the channel, and the charge carrier density in the channel.

2. An insulated-gate field-effect transistor comprising a channel of a semiconductor material; a source and a drain connected to said channel and defining the ends of a plurality of drain current paths in said channel, a metallic electrode across and spaced from said channel by an insulator which varies continuously or discontinuously as to some physical characteristic in a direction transverse to said current paths and along said gate whereby the field applied to the channel is varied in the direction transverse to the direction of current flow so as to provide the effect of a plurality of devices with different pinch off voltages connected in parallel and thereby obtain a remote cut-off characteristic.

3. An insulated-gate field-effect transistor



is preferably produced by deposition from a vapor. Also, in devices with polycrystalline channels, the channel material may be deposited upon the insulator or the insulator may be deposited upon the channel.

The fabrication techniques for insulated-gate field effect transistors are similar to those used to produce planar bipolar transistors and integrated monolithic devices. Impurity diffusion techniques may be used, and geometry may be controlled by precision masking and photolithographic techniques.

A fabrication schedule for a stepped oxide remote cutoff channel device may be as follows: A lightly doped P-type silicon wafer, about one inch in diameter and 0.007 inch thick, is polished on one side and the surface heavily oxidized in a furnace at about 900° C. containing a steam atmosphere to produce an oxide surface coating. The oxide surface coating is then etched away in selected areas defined by masking, using photolithographic techniques.

Next, the wafer is heated at about 1050° C. for 10 minutes in an atmosphere containing an N-type dopant, such as phosphorus, thereby forming source and drain regions which are not covered by the oxide. The entire remaining oxide layer is then removed. Then, the wafer is heated at about 900° C. in dry oxygen gas for about five hours until another, second oxide layer about 4000 Å thick is formed on the surface of the wafer. The wafer is cooled to room temperature and then reheated at about 400° C. in dry hydrogen gas for about 5 minutes to produce a desired channel characteristic. The second oxide layer is selectively removed over the source and drain regions as by etching.

The oxide layer over the channel is now stepped by using a series of photolithographic and partial etching operations designed to reduce the oxide thickness. The number of these operations depends upon the requisite number of oxide steps. In this example, four steps are produced having thicknesses of about 1000, 2000, 3000 and 4000 Å. Metal is evaporated over the entire wafer, and then selectively etched from all areas of the wafer except over the source region, the drain region and the stepped oxide. The metal over the stepped oxide between the source region and the drain region constitutes the gate of the device. The wafer is then diced into separate units or arrays. The units or arrays are mounted on a suitable support and leads are bonded thereto, as by thermal compression. After bonding, the units are encapsulated.

Another method for obtaining the stepped oxide employs photolithographic techniques to fully, instead of partially, remove the oxide. The oxide growth is then reheated. The areas with oxide already present grow thicker and the stripped regions grow to a thinner layer.

A method for obtaining a continuously

tapered oxide is to selectively deposit the insulator as by vapor deposition. By this technique, an aperture mask is moved slowly during the deposition laterally along the channel. The tapering of the oxide is controlled by the movement of the aperture mask and the rate of deposition. The thickness may be profiled by adjusting the rate of movement of the mask.

The fabrication of gate structures with a tapered or stepped dielectric constant in the insulator may be done by vapor deposition using more than one source, depositing different materials in sequence through a repositioned mask. One may, for example, use three sources with three different insulators with three dielectric constants corresponding to 65a, 65b, and 65c in FIGURE 7. After depositing the insulator corresponding to 65a through a suitable mask, the mask is moved laterally to the position corresponding to 65b and the insulator corresponding to 65b is deposited. By repeating the procedure the third insulator corresponding to 65c is laid down. By gradually moving the mask while gradually shifting from one insulator to the other, an insulator layer with tapered dielectric constant can be obtained.

For fabrication of structures with a tapered or stepped dielectric constant in the semiconductor, the same procedure may be used with three sources of three different semiconductors in combination with a movable mask.

WHAT WE CLAIM IS:—

1. An insulated-gate field effect transistor having drain current flow in a plurality of paths which have different pinch off voltages transversely across the gate, thereby obtaining a remote cut-off characteristic, said remote cut-off being obtained by a lateral change in one or more of the thickness of the insulator, the thickness of the channel under the gate of the transistor, the dielectric constant of the insulator, the dielectric constant of the channel, and the charge carrier density in the channel.

2. An insulated-gate field-effect transistor comprising a channel of a semiconductor material; a source and a drain connected to said channel and defining the ends of a plurality of drain current paths in said channel, a metallic electrode across and spaced from said channel by an insulator which varies continuously or discontinuously as to some physical characteristic in a direction transverse to said current paths and along said gate whereby the field applied to the channel is varied in the direction transverse to the direction of current flow so as to provide the effect of a plurality of devices with different pinch off voltages connected in parallel and thereby obtain a remote cut-off characteristic.

3. An insulated-gate field-effect transistor





- according to claim 1 or 2 wherein the thickness of said insulator varies continuously or discontinuously in said direction.
- 5 4. An insulated-gate field-effect transistor according to claim 1 or 2, wherein the composition or dielectric constant of said insulator varies continuously or discontinuously in said direction.
- 10 5. An insulated-gate field effect transistor according to claim 1 comprising a channel, a source and a drain connected to said channel and defining the ends of a plurality of drain current paths in said channel, and a gate spaced from said channel by an insulator, wherein it is a physical characteristic of said channel which varies laterally.
- 15 6. An insulated-gate field effect transistor according to claim 1 or 5, wherein it is the dielectric constant of said channel which varies laterally.
- 20 7. An insulated-gate field effect transistor according to claim 5 or 6 in which the channel is thicker than the insulator.
8. An insulated-gate field effect transistor according to claim 6 in which the dielectric constant of the insulator is greater than the dielectric constants of the channel.
- 25 9. An insulated-gate field-effect transistor substantially as hereindescribed with reference to the Figures 1—3, or 4 & 5, or 6 & 7, or 8, or 9 & 10, or 11, or 12 or 13 of the accompanying drawings.
- 30

For the Applicants
MATTHEWS, HADDAN & CO.
Chartered Patent Agents
31—32, Bedford Street,
London W.C.2.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1968.

Published by the Patent Office, 25, Southampton Buildings, London, W.C.2, from which copies may be obtained.

