

Isolating Substrate Noise by Forming Semi-Insulating Regions

[0001] This application claims the benefit of U.S. Provisional Application No. 60/611,186, filed on September 17, 2004, entitled "Method and Structure for Isolating Substrate Noise," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] This invention relates generally to integrated circuit isolation, and particularly relates to noise isolation using guard ring and proton bombardment.

BACKGROUND

[0003] Recent advances in IC design and fabrication make possible the integration of digital and analog circuits on the same IC chip. This technology is widely used in mobile communication systems where a digital core is combined with analog RF circuits. The digital and analog circuits are typically formed as a variety of components near one surface of a wafer. These components may be at several levels separated by inter-metal dielectric layers. Usually, the topmost layer is made of a dielectric material and serves as a passivation layer for the entire structure.

[0004] The integration of the digital and analog circuits causes noise coupling between the digital and analog circuits. The analog circuit is especially affected by the noise generated in the digital circuit. This significantly limits the performance achieved in analog signal processing and data conversion circuits, such as differential amplifiers that are extremely sensitive to the noise at the differential inputs. Figure 1 illustrates the noise path between the digital and analog circuits.

Region 4 is a digital circuit. Region 6 is an analog circuit. Arrows 8, 10 and 12 symbolize one of the noise paths in the substrate 2.

[0005] Besides the noise interference between the digital circuit and analog circuit, noise interference also exists between the digital circuit components.

[0006] There is a significant dependence of the noise coupling through the substrate on the constitution of the silicon substrate. Therefore, various methods have been developed to break the noise path in the silicon substrate. One commonly used method is forming isolation layers in the substrate. As shown in Figure 1, an isolation layer 14 breaks the noise path between circuit regions 4 and 6. Isolation layer 14 is typically formed of dielectric materials. One example of the isolation layer 14 is a trench isolation between the circuits to be isolated. To form deep trench isolation, trenches with near vertical sides are etched between the circuits and then filled with dielectric materials.

[0007] However, even deep trench isolation is not fully satisfactory when full isolation between the circuits is required. This is particularly true when high-speed analog circuits are involved.

[0008] Another known method is placing a guard ring in the substrate and between the circuits to be isolated. As illustrated in Figure 2, a p⁺ guard ring 20 is formed in a p⁻ substrate 2. The guard ring 20 is grounded as shown at 22; therefore, it creates a low resistivity path for the substrate noise. The noise is more likely to take the low resistivity path to the guard ring 20 than a higher resistivity path to another circuit region.

[0009] Yet another method has been developed. Figure 3 illustrates a proton bombardment approach. Semi-insulating region 24 is created by proton bombardment from the topside of the

substrate 2 between the circuits 4 and 6 to be isolated. The semi-insulating region 24 has resistivity of higher than about $10^5 \Omega\text{-cm}$. Therefore, a high resistivity path is created between the circuits to isolate the noise. To further isolate the circuits, the substrate 2 is also bombarded from the backside, creating a semi-insulating region 26. When the semi-insulating region 24 created from the topside and the semi-insulating region 26 created from the backside of the circuit are connected, the noise path in the substrate is effectively isolated by high resistivity isolations.

[0010] The guard ring and proton bombardment are effective methods for noise isolation. However, when the size of the integrated circuit drops to $0.13\mu\text{m}$ or lower, and the frequency increases to over about 1GHz, the noise interference becomes more severe and better isolation techniques are needed.

SUMMARY OF THE INVENTION

[0011] The preferred embodiments of the present invention provide an integrated circuit structure for isolating substrate noise and a method of forming the same.

[0012] In accordance with one aspect of the present invention, a semi-insulating region is formed in a substrate between a first circuit region and a second circuit region by proton bombardment. Two guard-rings are formed along the semi-insulating regions. A backside semi-insulating region is formed using proton bombardment from the back surface of the substrate. The backside semi-insulating region is preferably connected with the semi-insulating region created from topside. A grounded guard layer is then formed on the backside semi-insulating region.

[0013] The preferred embodiments of the present invention effectively isolate the substrate noise.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0015] Figure 1 illustrates a noise path in a substrate between a digital circuit region and an analog circuit region;

[0016] Figure 2 illustrates a conventional method of forming a guard ring in a substrate to isolate the noise between a digital circuit region and an analog circuit region;

[0017] Figure 3 illustrates a conventional method of using semi-insulating regions created by proton bombardment to isolate the noise between a digital circuit region and an analog circuit region;

[0018] Figure 4 illustrates the formation of a digital region, an analog region, and guard rings;

[0019] Figure 5 illustrates the formation of a proton mask for a topside semi-insulating region;

[0020] Figure 6 illustrates proton bombardment to the topside of the substrate creating a semi-insulating region;

[0021] Figure 7 illustrates a proton bombardment from the backside of the substrate;

[0022] Figure 8 illustrates a back side grounded guard layer formed on the backside of the substrate;

[0023] Figure 9 illustrates a top view of a digital region, an analog region and the insulation regions;

[0024] Figure 10 illustrates a top view of a digital region and analog regions with only the digital region insulated; and

[0025] Figure 11 illustrates noise levels as functions of frequency.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0026] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0027] The preferred embodiments are illustrated in Figures 4 through 11 wherein like reference numbers are used to designate like elements throughout the various views and illustrative embodiments of the present invention. Figure 4 illustrates a silicon substrate 2 having two circuit regions 4 and 6. Throughout the description of the preferred embodiments, region 4 is referred to as a digital circuit region and region 6 is referred to as an analog circuit region. However, in other embodiments, regions 4 and 6 can also be two digital regions, two analog regions or two compound regions that include both analog and digital circuits.

[0028] Topside guard rings 32 and 34 are formed in substrate 2. A space 36 is left between the topside guard rings 32 and 34 in order to form a topside semi-insulating region. In the preferred embodiment, there are two topside guard rings formed. The first guard ring 32 is formed along the topside semi-insulating region 36 on the first circuit region 4 side. The second guard ring 34 is formed along the topside semi-insulating region 36 on the second circuit region 6 side. The second guard ring 34 is substantially similar to the first guard ring 32. In other embodiments, only one guard ring 32 that is closer to the digital region 4 is formed. In yet other embodiments, a single guard ring may be formed closer to analog region 6. Preferably, the guard rings 32 and 34 are formed by implanting a p type impurity into a p- type substrate to form a p+

region, or implanting an n type impurity into an n- type substrate to form an n+ region.

Preferably, the guard rings 32 and 34 are formed simultaneously with the source and drain region implantation and/or silicidation in the integrated circuit. The topside guard rings 32 and 34 may also be formed by methods such as forming recesses and growing highly doped silicon in the recesses, providing the source and drain regions are formed the same way. It is preferred that the guard rings 32 and 34 are formed using the same method used for forming other parts of the circuit so that there are fewer forming steps involved.

[0029] The guard rings 32 and 34 substantially extend from the top surface of the substrate 2 into the substrate. The guard rings 32 and 34 have a preferred depth of about 0.2 μ m to about 0.4 μ m and a width of greater than about 0.5 μ m. They are preferably connected to the substrate 2. In the preferred embodiment, the guard rings 32 and 34 connect to a circuit ground pad through a metal/contact/substrate structure, which is known in the art.

[0030] Figure 5 illustrates the formation of a proton mask 41 for forming the topside semi-insulating region 36. The proton mask 41 is formed over the digital region 4, the analog region 6 and the topside guard rings 32 and 34. It is to be noted that a semi-insulating region produced by proton bombardment is unstable over long periods if maintained at temperatures in excess of about 400°C, so it is preferable that the proton bombardment not be performed until the manufacture of the integrated circuit is substantially complete. Therefore, an inter-layer 40 typically exists between the proton mask 41 and the digital region 4 and circuit region 6 since the proton mask 41 is preferably formed at a point after the formation of the digital and analog regions and before packaging. The packaging temperature after forming the semi-insulating regions produced by proton bombardment is preferably less than 350°C. The inter-layer 40

represents multiple device layers that are not necessary for understanding the invention and may comprise PMD, CESL and/or other layers.

[0031] The proton mask 41 is preferably formed of a proton mask layer 44, which preferably comprises silicon or metal, on an adhesive layer 42. The adhesive layer 42 is used to bond the inter-layer 40 and the proton mask layer 44. In the preferred embodiment, the adhesion layer 42 is a photo resist. Although conventionally the proton mask layer 44 is formed of heavy metals, in the preferred embodiment of the present invention, silicon is preferred over metals since metals affect the characteristics of the underlying layers when metals are diffused. The adhesive layer 42 is preferably formed through a traditional lithography coating approach to a thickness of about 15 μ m to about 30 μ m. The proton mask layer 44 is preferably formed by depositing raw wafer material to a thickness of about 200 μ m to about 600 μ m, and more preferably about 300 μ m to about 400 μ m. The thickness of the proton mask layer 44 is related to the energy and proton current of the proton bombardment and it is desired that its thickness be enough to prevent the protons from penetrating and reaching the underlying layers. An opening 50 is formed in the proton mask layer 44, preferably by using dry etch, to expose the region 36 to proton bombardment. Photo resist 42 acts as an etching stop layer.

[0032] Figure 6 illustrates a proton bombardment, which is symbolized by arrows 52, performed from the topside of substrate 2. Without the protection of the silicon proton mask layer 44, protons penetrate the photo resist 42 and inter-layer 40 and bombard region 36. The proton bombardment to the silicon region 36 destroys the lattice structure of the silicon substrate and forms amorphous silicon; therefore, the resistivity is increased. In a typical case, the resistivity of the region 36 is increased from about 10 Ω -cm before proton bombardment to about 10⁵ Ω -cm after.

[0033] To prevent the protons from penetrating the proton mask layer 44 and destroying the underlying layers in regions not intended to be bombarded, the topside proton bombardment uses lower energy, preferably about 1MeV to about 3MeV. The topside semi-insulating region 36 substantially extends from the top surface of the substrate into the substrate. The depth of the resulting semi-insulating region 36 is preferably less than about 50 μ m, and more preferably about 10 μ m to about 50 μ m. The width of the semi-insulating region 36 is preferably greater than 10 μ m, and more preferably between about 30 μ m to about 50 μ m. The proton current is also preferably low, more preferably between about 5E14 protons/cm² and about 5E15 protons/cm². The proton mask 41 is then removed through a traditional photo resist stripping approach.

[0034] A backside semi-insulating layer 51 is then formed at the backside of the substrate 2, as illustrated in Figure 7. The backside of the substrate is blanket bombarded by protons. Arrows 53 symbolize the proton bombardment. The energy of the proton bombardment is preferably between about 10MeV and about 20MeV. The preferred proton current is about 5E15 protons/cm² to about 5E16 protons/cm². The backside semi-insulating region 51 substantially extends from the back surface of the substrate 2 into the substrate. Using these bombardment parameters, the thickness of the resulting semi-insulating region 51 is typically between about 200 μ m to about 400 μ m.

[0035] Better isolation is provided if the semi-insulating region 36 is connected to semi-insulating layer 51. Therefore, the depth of the semi-insulating layer 51 may be adjusted by adjusting the bombardment energy and the optimal energy can be determined according to the thickness of the wafer.

[0036] In one preferred embodiment, a backside guard layer 54 is formed on the semi-insulating layer 51, as illustrated in Figure 8. The guard layer 54 is preferably grounded. The guard layer 54 preferably comprises a metal such as aluminum, aluminum-copper alloy, copper, copper alloy, gold, silver, iron, tin, and the like. In the preferred embodiment, the backside guard layer 54 is blanket sputtered to a desired thickness of about 200 μ m to about 1000 μ m, and more preferably about 200 μ m to about 400 μ m. In other embodiments, physical vapor deposition (PVD), plating, and plasma enhanced CVD (PECVD) can also be used. The backside guard layer 54 is preferably grounded for electrical isolation. In other embodiments, there is no backside guard layer 54 formed.

[0037] Topside guard rings 32, 34 and semi-insulating region 36 are preferably formed surrounding the region to be isolated, although they can be formed as strips or other configurations. Figure 9 illustrates a top view of a digital region 4 and an analog region 6 being isolated. Topside guard rings 62, 64 and semi-insulating region 36 enclose both digital region 4 and analog region 6. Considering that there is a semi-insulating region underneath the digital region 4 and analog region 6, digital region 4 and analog region 6 are each isolated in a well constructed of semi-insulating materials and guard rings.

[0038] The insulating scheme in Figure 9 protects digital and analog circuits from both inside and outside noise sources. However, to have an insulating scheme like this, more space is needed. In a typical IC circuit with both digital and analog circuits, there may be one digital region and multiple analog regions. Figure 10 illustrates another scheme protecting the analog circuits from the digital circuit noise. Digital circuit 4 is enclosed in a well formed of guard rings 32, 34 and semi-insulating region 36 and a semi-insulating layer (not shown) on the backside of

the substrate 2, while the analog circuits 6 are placed outside of the well. The noise generated by the digital circuit is thus isolated inside.

[0039] The preferred embodiments of the present invention provide effective noise isolation, particularly when the size of the integrated circuit drops to about 0.13 μ m or lower, and the frequency increases to over about 1GHz, since the noise interference becomes more severe and better isolation techniques are needed. Figure 11 illustrates noise levels 70 and 72 as functions of frequency. Line 70 shows the noise level measured in a circuit with no noise isolation. A -10db noise level is measured. Line 72 illustrates the noise measured using the present embodiment. At 0.1GHz, the noise is about -70db, at 1GHz, the noise is about -50db, and at 10GHz, the noise is about -40db. Therefore, the present embodiment has a noise reduction of about 60db at 0.1GHz and about 40db at 1GHz. As a comparison, by using a guard ring only, the noise reduction is about 20db at 1GHz, and by using proton bombardment only, the noise reduction is about 25db at 1GHz. Therefore, the preferred embodiments of the present invention have greatly improved the noise isolation between digital and analog regions in the integrated circuit.

[0040] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding

embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. An integrated circuit structure comprising:
 - a first circuit region in a substrate;
 - a second circuit region in the substrate;
 - a first semi-insulating region between the first circuit region and the second circuit region wherein the first semi-insulating region substantially extends from a top surface of the substrate into the substrate;
 - a first guard ring along and adjoining the first semi-insulating region wherein the first guard ring substantially extends from the top surface of the substrate into the substrate;
 - a second semi-insulating region extending substantially from a surface of a backside of the substrate into the substrate, wherein the first semi-insulating region physically contacts the second semi-insulating region; and
 - a guard layer on the second semi-insulating region from the backside of the substrate, wherein the guard layer is grounded.
2. The integrated circuit structure of claim 1 wherein the first circuit region comprises a digital circuit region and wherein the first guard ring is on the first circuit region side of the semi-insulating region.
3. The integrated circuit structure of claim 2 wherein the second circuit region comprises an analog circuit region.
4. The integrated circuit structure of claim 1 wherein the first guard ring is along the first semi-insulating region and is on a same side of the first semi-insulating region as the first circuit region.

5. The integrated circuit structure of claim 4 further comprising a second guard ring adjoining the first semi-insulating region, wherein the second guard ring is on a same side of the semi-insulating region as the second circuit region.
6. The integrated circuit structure of claim 1 wherein the first guard ring is coupled to a circuit ground pad through a metal/contact/substrate structure.
7. The integrated circuit structure of claim 1 wherein the first guard ring has a depth of about $0.2\mu\text{m}$ to about $0.4\mu\text{m}$.
8. The integrated circuit structure of claim 1 wherein the first semi-insulating region has a depth of about $10\mu\text{m}$ to about $50\mu\text{m}$.
9. The integrated circuit structure of claim 1 wherein the second semi-insulating region has a thickness of about $200\mu\text{m}$ to about $400\mu\text{m}$.
10. The integrated circuit structure of claim 1 wherein the guard layer has a thickness of about $200\mu\text{m}$ to about $1000\mu\text{m}$.
11. The integrated circuit structure of claim 1 wherein the guard layer comprises aluminum, aluminum-copper alloy, and combinations thereof.

12. The integrated circuit structure of claim 1 wherein the semi-insulating region and the substrate are formed of a same material.

13. An integrated circuit structure comprising:

a semiconductor substrate;

a semi-insulating region extending substantially from a top surface of the semiconductor substrate into the semiconductor substrate; and

a first guard ring adjoining the semi-insulating region, wherein the first guard ring extends substantially from the top surface of the semiconductor substrate into the semiconductor substrate.

14. The integrated circuit structure of claim 13 further comprising a second guard ring adjoining the semi-insulating region and on an opposite side of the semi-insulating region than the first guard ring, wherein the second guard ring extends substantially from the top surface of the substrate into the substrate.

15. The integrated circuit structure of claim 13 further comprising a backside semi-insulating layer extending from a bottom surface of the semiconductor substrate into the semiconductor substrate, wherein the semi-insulating region physically contacts the backside semi-insulating layer.

16. The integrated circuit structure of claim 15 further comprising a metal layer adjoining the backside semi-insulating layer, wherein the metal layer is on an opposite side of the backside semi-insulating layer than the semi-insulating region.

17. The integrated circuit structure of claim 13 wherein the semi-insulating region comprises same materials as the semiconductor substrate, and has a resistivity of greater than about $10^5 \Omega\text{-cm}$.

18. The integrated circuit structure of claim 13 wherein the semi-insulating region forms a first ring, and the first guard ring forms a second ring, and wherein the first and the second rings are co-centroid and encircle an integrated circuit region.