

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO A COMPUTER EXECUTED TONE OR TONE SEQUENCE GENERATION SYSTEM

(71) I, ROBIN DAVID PALMER, a British subject, of Coachworks House, River Way, Harlow, Essex, do hereby declare the invention, for which I pray that a patent may be granted to me, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a computer executed tone generation system and particularly, but not exclusively, a system for generating or "playing" a tune under the command of instructions in a memory of a processor, the tune being stored in a memory in encoded form. Such system can be used with particular utility as a "door bell" system.

According to one aspect of the present invention there is provided a system for selecting a tone or tone sequence from a plurality of encoded tones or tone sequences and generating the tone or tone sequence as an electrical signal, the system comprising a first memory containing a plurality of tones or tone sequences stored in encoded form in respective locations in the memory, means, including a processor, for generating an electrical signal representing the required tone or tone sequence in response to data read out from a selected location, a second memory forming part of the generating means and having instructions determining the operation of the generating means, a plurality of input stages responsive to applied signals for feeding data to the processor; and a plurality of output stages individually controllable by the processor, the second memory being arranged to control the processor to apply a signal to each of the output stages in turn and to identify, when a selected one of the output stages is in use linked to a selected one of the input stages, the particular input stage at which a signal is received and the particular output stage then supplying the signal to the input stage, each of said respective locations being uniquely associated with a different linking between the input stages and the output stages, and the second memory controlling the read out of data from that

location in the first memory corresponding to the identified input stage/output stage linking. The memories are preferably in the form of read only memories.

Such a system has utility in, for example, doorbells where a tone sequence can be a recognisable tune and the linking selects the tune to be generated. In this case a bell push switch can be used to initiate the application of the signals to the output stages. In an alternative use, the generation of the tone or tone sequence can be triggered by an event such as the detection of the presence of an intruder, and furthermore, this detection can be employed to set a particular linking so that the generated tone or tone sequence becomes indicative of the whereabouts of the detected intruder. The generated electrical signal can be transmitted to a monitoring station, or used for example to initiate automatic dialling of a pre-selected telephone number for example that of the local police station.

It will be appreciated that the frequency of the tones will be selected according to the intended use of system, for example if the generated electrical signals are to be fed to loudspeakers they will be in the audio range, and if they are to be used to actuate electrical equipment they will be compatible with the requirements of the particular equipment and may be at infra-sonic or ultra-sonic frequencies.

In order to save energy, the system can be arranged to be unenergized in its inoperative or quiescent state, and can include a controllable switch responsive to a signal from the processor and arranged to complete a circuit path between power supply terminals of the system. An external switch, for example a bell push switch, can be connected in parallel with the controllable switch and when operated will energize the system, the second memory being arranged to cause activation of the controllable switch thus maintaining the system energized, and being arranged in some embodiments to cause deactivation of the controllable switch

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at the end of a generated tone sequence, and in other embodiments to cause deactivation at the end of a preselected number of bars (i.e. a first segment) of the musical tune provided that the bell push switch had been released and to continue with successive segments (eventually playing the whole of the tune) should the bell push switch be continually closed.

In embodiments for generating tunes, if more than one tune is required to be generated each time the system is energized, a second memory can be arranged to generate a pre-selected number of tunes starting with the tune corresponding to the link between the input stages and the output stages before deactivating the switch. However, if only the selected tune is desired the deactivation will be effected at the end of this tune.

The processor is preferably arranged to generate by the following method a selected one of the predetermined sequential set of tones, the selected tone to be generated being indicated by a word representing its sequential position, the method comprising entering in a store a predetermined number representative of the number of timing pulses to be counted for establishing half the period of the first tone of the set, performing a number of steps of incrementing (or decrementing, depending upon whether the tones of the set are in descending or ascending order, respectively) the contents of the store by respective predetermined numbers representing the respective differences between adjacent ones of the predetermined numbers representing the number of timing pulses to be counted for generating the tones of the set, the number of steps being performed being equal to one less than the sequential position of the selected tone to be generated, and proceeding to generate the desired note in accordance with the current contents of the store upon completion of said number of steps.

By arranging the processor to operate in this manner, the store does not contain all the respective numbers to be counted, but instead contains the first of these (corresponding to the first tone of the set) and a set of respective difference values enabling the calculation of the remaining numbers to be counted by successive modification in accordance with these difference values.

For determining the number of steps, preferably the first position is coded zero, and there is employed a technique of successive decrementing by one and stopping when zero is reached. It will be appreciated that if the tone selected is the first in the set, then the code for the selected tone will be zero and the tone will be generated without any modification by a difference value. If desired, the number of steps can be determined by other techniques, for example a successive incrementing technique, but these may involve the use of a greater number of stores and/or more com-

plicated instructions.

Conveniently, the tones in the sequence can be in ascending order, as in the embodiment described later. However, it will be appreciated that if the sequence is in descending order the predetermined number of timing pulses for the first tone will be the smallest, and under certain conditions this arrangement may be desired for enabling a reduction in the size of the store allocated in the processor for storing this number.

This tone generation technique is of particular utility in microcomputers to avoid wasteful storage utilization by "look-up" procedures. Although the smaller the microcomputer the greater the advantage obtained from the point of view of storage space released for other purposes, it will be appreciated that this aspect is not limited to microcomputers and can be employed in larger computers, the released storage being used for other purposes, possibly for storing a further tone sequence in encoded form.

In generating the tone the contents of the store are read and entered into a further store which is counted down to zero to produce a pulse for toggling a flip-flop, at which the contents of the store are again read into the further store. This sequence continues for as long as it is intended, in other words, until an instruction derived from, say, another part of a tone sequence generating programme causes the computer to return to the beginning of the generation procedure and read in the next word representing a tone to be generated. If this count down is based on timing pulses at or in the region of the master clock rate, the numbers may be relatively large in a tone generating system, for example for the note G below middle C the half period in microseconds is approximately 2600 and this would require a 12 bit store not only in the memory but in the CPU for performing the count down if pulses from, for example a 1 MHz clock were counted. Thus preferably timing pulses at a lower repetition rate are employed, and conveniently the period of "machine cycles" of the CPU is approximately 2^3 times that of the above-mentioned 1 MHz master clock. Therefore by counting machine cycles the approximate number requires an 8 bit store in the memory and in the CPU. Typically the machine cycle has a period of 15 μ seconds and thus the corresponding number of machine cycles to be counted for G is approximately 173. Alternatively, but not preferred, an external oscillator having a frequency of about 66KHz can be used.

A consequence of the abovementioned enter/count down technique is that the CPU cannot instantaneously re-enter the number upon the count reaching zero, and it takes a certain number of machine cycles to accomplish re-entering of the number to be counted. Thus, the actual number entered is smaller

by this certain number than the number of machine pulses corresponding to the desired half period. As an example, for a minimum of 33 machine cycles for achieving this re-entry and for the note G (assuming the half period = 173 machine cycles) the actual number stored in the memory will be 140, and for the note A, one tone above G, the corresponding number is 121.

If the second note of the set is A (121) then it will be understood that the contents of the second store will need to be reduced by 19, this being the first preselected number, referred to as a difference number. It will be appreciated that if the notes progress by semitones then the first difference number will be 10 to produce the note G# (130). However, such a latter sequence will not be desirable in practice since only just over one octave can be encoded by the use of a 4-bit store, and it is therefore preferred to omit certain notes. This means that some difference numbers will correspond to semitones while others correspond to full tones. Furthermore it will be understood that the higher the notes the smaller the values of these difference numbers, and therefore the largest difference number will be that for a full tone between the lowest note of the set and the adjacent note. The difference numbers are generally frequency dependent, as will be understood by reference to the mathematical relationship of notes in an equally tempered scale, becoming halved for each octave rise (i.e. a doubling in frequency). Thus for a difference number of 10 in respect of a semitone at the bottom of the sequence starting at G, the difference number for a note approximately two octaves above will be approximately 3.

One can store the difference numbers without modification but this will require stores larger than 4 bits in length. Thus, preferably, to reduce the amount of storage space required for the difference numbers a technique is adopted to reduce the largest difference number to 15, i.e. the largest number storable in a 4-bit store. To do this the aforementioned value of 19 has to be reduced by 4 and similarly all other difference numbers will be reduced by 4. Conveniently the difference numbers at the high end of the set are approximately equal to four, and should one or more be equal to three then a slight modification can be made to the number of machine pulses to be counted so as to raise the minimum difference number to four. In this manner the range of difference numbers is from 0 to 15. The reduction of the number stored in the second store will thus be a two stage process of reduction by the modified difference number and reduction by the constant 4.

If the difference between the largest and smallest difference numbers obtained when first deriving the predetermined sequence is greater than fifteen, then one can, as mentioned

above, make slight adjustments to the "frequency" selected for certain notes, i.e. the number of timing pulses to be counted for determining the half period. However, if the lowest note of the sequence is approximately C below middle C then the difference number for a tone interval to D will be approximately 28 and the above technique of subtracting a single constant to obtain a range of fifteen cannot be adopted because the changes in the "frequencies" of the notes will no longer be insignificant and the notes generated will be obviously incorrectly pitched. In such a case, a further constant can be introduced to be subtracted in the same manner but only for, say, a maximum of two consecutive subtractions in generating the note, where the intervals are full tones, i.e. C to D, and D to E.

It will be appreciated that the above mentioned technique involving one or more subtractions of constants to enable the maximum difference number to be not greater than fifteen and thus storable in a four-bit store, may not always be required. The sequence of notes may be so selected that the first full tone interval gives a difference number less than fifteen, for example where the first note of the sequence is the abovementioned G and the second note is A the difference number is 19, but if A was the first in the sequence with B as the second then the difference number on this basis would be 16 and a slight modification to the "frequency" of A would give a difference of 15 and no constant subtraction would be needed. Furthermore, it would be possible to use a lower frequency timing pulse to reduce the absolute values of the numbers to be counted down and, hence, of the difference numbers. In this connection it may be possible to use a simple flip-flop to half the frequency of the machine pulses. However, this approach of lowering the timing pulse frequency cannot be pursued too far because at the high end of the sequence the errors will eventually become too large.

The invention will now be particularly described by way of example with reference to a preferred embodiment of an electronic door bell system which upon actuation by, for example, a conventional bell push switch associated with a door, generates and reproduces via a loudspeaker a preselected tune.

The system comprises an audio amplifier and loudspeaker, together with a microcomputer for generating an audio signal representing the desired tune.

The microcomputer may be in the form of a single proprietary integrated circuit chip, or separate central processor unit and memory devices. In either form the basic components will be as follows:—

(a) a central processor unit (CPU) capable of decoding and executing instructions stored in a read only memory (ROM);

(b) a ROM having permanently stored instructions for the control of the CPU;

(c) a ROM having permanently stored data representing a number of digitally encoded tunes;

(d) an input register having inputs K1 to K4 and being arranged to accept externally applied data;

(e) an output register having outputs O1 to O8, each bit of the register being separately controllable by the CPU;

(f) a set of addressable random access registers (RAMs) for temporary data storage; and

(g) a clock pulse generator.

The ROMs of (b) and (c) may be separate memories, or may be separate portions of a single memory.

Conveniently the system is powered by a battery and is unenergized in its inoperative condition. The bell push switch is arranged to connect the battery to the system and energization is maintained by means of a semiconductor switch controlled by, for example, the O8 bit of the output register.

To select the tune to be "played" by the system, one of the output bits O1 to O5 of the output register is connected to one of the inputs K1 to K3 of the input register. Thus in this particular arrangement there are fifteen different ways of making this external link between the output register and the input register.

The manner of operation of the system can readily be understood from the following statements indicating the steps preprogrammed into the ROM of (a).

(1) Reset all RAMs upon energization of system.

(2) Monitor the inputs K1 to K3 whilst stepping along the output bits O1 to O5 to test for and identify the location of an external link K—O.

(3) Read out the stored musical data in the location in the ROM of (c) corresponding to the identified link K—O.

(4) Interpret, by means of a sub-routine, the musical data read out in step (3). This may involve storage of translated data in the RAM.

(5) Generate, by means of a sub-routine involving counting pulses, representing machine cycles, timing pulses corresponding to the desired pitch of the notes and cause the output bit O7 to toggle in response to the timing pulses. (The term toggle means to change state for each pulse applied to a trigger input.)

(6) Maintain the note generation of step (5) while the state of the K4 input is low, and upon change of state of the K4 input generate a resetting pulse on the output bit O6.

(7) If the particular note being generated is to have a duration of two or more times a basic time interval determined by a resettable, adjustable RC timing circuit connected to the

input K4, repeat step (6) the required number of times as determined by the data.

(8) When a musical rest is encountered in the tune, cease the note generation of step (5) (i.e. inhibit the output bit O7) but continue steps (6) and (7) reading "rest" for "note".

(9) When a special code in the read-out data is encountered signifying the end of the tune, activate the output bit O8 to cause the semiconductor switch to become non-conductive and thus de-energize the system. In the event that the system remains energized, the programme can loop back to generate the same selected tune or another tune stored in the ROM.

As mentioned, the tune to be "played" is selected by establishing a K—O link. The selection can be made at the manufacturing stage where the link will be pre-set, there being no external selector means for use by a customer. Alternatively, the customer can be provided with means to select any of the possible K—O links. Such means can be a mechanical multi-position switch, or can involve electronic switching.

It will be understood that the tempo of the tune can be changed by altering the time constant of the RC circuit coupled to the input K4, and that this will not affect the pitch of the notes since these are determined by the counting of the clock pulses.

In an alternative arrangement the tempo of a generated tune can be determined by an interrupt technique. The cyclic note generation routine could be interrupted by an external trigger pulse of adjustable periodicity to determine the duration of the basic note value by means of a counting sub-routine.

In computer executed note generation, the simplest determination of the note period from a note value code is by means of a "look-up" table. In other words, for each note value the computer store contains a number representing the number of timing pulses to be counted to obtain the desired toggle rate of the output bit at which the audio output signal is supplied.

In practice, each separate count-down corresponds to a half period of the note to be generated.

If the computer has a large store then the routine for determination and generation of the note can be simple, incorporating e.g. the above "look-up" technique. There is no need for economy of storage utilization and typically each stored number will be in the form of an 8 bit word or even longer, especially where the timing pulses are master clock pulses.

Where the computer is that of, or intended for, for example a tune-playing door bell system, it is desirable to make the computer small to obtain good battery life and low cost. However, the smaller the computer store becomes, the more difficult it is to employ the simple "look-up" technique mentioned above.

In practical terms, if a computer is based on an 8 bit organization CPU there will be sufficient storage for this, but if it is based on only a 4 bit chip, there will not be sufficient storage, and the instruction repertoire may be severely limited.

The preferred embodiment of an electronic door bell system includes a routine for the determination of the note period, which routine enables efficient use of a small memory such as that available on the single chip. The routine is based on the storing of a number representing the lowest note period and of numbers representing the respective differences

between adjacent notes of the system. Furthermore, for reducing the value of these numbers, the routine is based on the counting of machine cycles, as opposed to pulses at or in the region of master clock rate. Typically, the machine cycle time for a microcomputer based on a single chip is approximately 15 μ s, and thus a convenient encoded form for A is 77 machine cycles giving a frequency of 452 Hz.

As can be seen by reference to table 1 given below, the system stores 15 note values and a rest. The notes span nearly two octaves and permit chromatic sequences corresponding to the keys of C, G and F.

TABLE 1

X	Designation	Half-period in machine cycles	Y (Half-period less 33 machine cycles)	Actual differences	Value of Dif n for C=4
15	Rest				
14	E	52	19	6	2 (Dif 14)
13	D	58	25	7	3 (Dif 13)
12	C	65	32	4	0 (Dif 12)
11	B	69	36	4	0 (Dif 11)
10	B ^b	73	40	4	0 (Dif 10)
9	A	77	44	10	6 (Dif 9)
8	G	87	54	5	1 (Dif 8)
7	F [#]	92	59	5	1 (Dif 7)
6	F	97	64	6	2 (Dif 6)
5	E	103	70	13	9 (Dif 5)
4	D	116	83	14	10 (Dif 4)
3	Middle C	130	97	8	4 (Dif 3)
2	B	138	105	16	12 (Dif 2)
1	A	154	121	19	15 (Dif 1)
0	G	173	140		

In practice, the microcomputer of the system has a minimum period of 33 machine cycles for the operations of recognizing that the count-down has reached zero, and re-entering from a store the number to be counted down. This re-enter and count-down to zero

sequence occurs for each successive half period of the note being generated, and the signal at zero is used to toggle the output bit 07. The consequences of this minimum period are that the highest note that the system can generate is approximately C two octaves above

middle C, and that the actual number Y entered for count down will be smaller by 33 than that corresponding to the required half period, for example the number Y to be entered and counted down for A is 44.

5 The lowest note of the system having the note value code 0 is G below middle C and the number Y to be entered and counted down to obtain this G is 140. This number 140 is
10 stored in the ROM as the basic number from which all other values of Y are obtained by subtraction of difference values. It will be noted that the denary number 140 can be contained in an 8 bit store in the binary form
15 10001100, and also that, for the particular digitized form of the notes, the largest difference is 19 which cannot be contained in a 4 bit store. However, the numbers representing the half period have been so selected that
20 the range of the actual differences is from 4 to 19, that is a range of 15 and this can be contained in a 4 bit store. Accordingly, the constant value 4 is subtracted and the Dif values then range from 0 to 15 as shown in
25 table 1.

Thus the ROM contains the values of Dif 1 to Dif 14, the constant 4, and the constant 140.

30 The determination of the note period for the note to be generated is by means of a routine the steps of which are set out in table 2 below.

The routine requires the entering of X the note value code and the successive modification of the number in store 2 X times. A conventional technique being used for determining
35 when the number of successive modifications equals X, whereupon the resultant number in the store then represents the half period of the note to be generated and can be used in a
40 following execution routine.

TABLE 2.

Routine for determination of note period from a note value code.

Step	Description
1.	Read out note value code X from ROM and enter in temporary store 1.
2.	Is store 1 = 15? If YES go to step 3, if NO go to step 4.
3.	Set latch to inhibit toggling of output bit O7.
4.	Read out binary number 10001100 (denary 140) from ROM and enter in temporary store 2.
5.	Is store 1 = 0? If YES go to step 13, if NO go to step 6.
6.	Enter constant 4 from ROM in temporary store 3.
7.	Enter value of Dif n from ROM in temporary store 4 (Dif n = 1 + number of previous executions of step 7).
8.	Is store 1 = 0? If YES go to step 5, if NO go to step 9.
9.	Reduce number in store 1 by one.
10.	Reduce number in store 2 by number in store 4 (i.e. Y minus Dif value).
11.	Reduce number in store 2 by number in store 3 (i.e. subtract constant 4).
12.	Go to step 5.
13.	Execute note generation in accordance with number in store 2.

Whereas the abovedescribed embodiment plays the selected tune until the end and then switches off, in an alternative embodiment this automatic switch-off takes place after a pre-selected number of notes of the tune have been generated, say those notes corresponding to the

first two or three bars of the music, provided that by that time the bell push switch has been released. If the caller keeps the bell push switch closed then succeeding notes of the tune are generated. If desired, there may be more than one such break-point in the tune at which the system can automatically switch itself off.

WHAT I CLAIM IS:—

1. A system for selecting a tone or tone sequence from a plurality of encoded tones or tone sequences and generating the tone or tone sequence as an electrical signal, the system comprising: a first memory containing a plurality of tones or tone sequences stored in encoded form in respective locations in the memory; means, including a processor, for generating an electrical signal representing the required tone or tone sequence in response to data read out from a selected one of the locations in the first memory; a second memory forming part of the generating means and having instructions determining the operation of the generating means; a plurality of input stages responsive to applied signals for feeding data to the processor; and a plurality of output stages individually controllable by the processor; the second memory being arranged to control the processor to apply a signal to each of the output stages in turn and to identify, when a selected one of the output stages is in use linked to a selected one of the input stages, the particular input stage at which a signal is received and the particular output stage then supplying the signal to the input stage, each of said respective locations being uniquely associated with a different linking between the input stages and the output stages, and the second memory controlling the read out of data from that location in the first memory corresponding to the identified input stage/output stage linking.

2. A system as claimed in claim 1 wherein the memories are in the form of read only memories.

3. A system as claimed in either claim 1 or claim 2, comprising an external switch arranged to complete the power supply circuit of the system, and a controllable switch responsive to a signal from the processor and arranged to electrically in parallel with the external switch to complete said power supply circuit while the system is operative.

4. A system as claimed in claim 3 wherein said second memory is arranged to provide said signal to the controllable switch and is arranged to cause deactivation of the controllable switch at the end of the selected tone sequence.

5. A system as claimed in claim 3 wherein said second memory is arranged to provide said signal to the controllable switch and is arranged to cause deactivation of the con-

trollable switch at the end of a predetermined succession of tone sequences starting with that tone sequence corresponding to the identified input stage/output stage linking.

6. A system as claimed in claim 3 wherein each tone sequence comprises a plurality of successive segments and wherein said second memory is arranged to provide said signal to the controllable switch and is arranged to cause deactivation of the controllable switch at the end of a segment provided that the external switch is open at that time, the respective last segments of the sequences being disregarded if successive sequences are to be generated and being taken into account if the system is to stop at the end of the selected sequence.

7. A system as claimed in any one of the preceding claims wherein the processor is arranged to generate by the following method the selected tone or a tone of a sequence, the tone to be generated being indicated by a word representing its sequential position with respect to the set of different encoded tones, the method comprising entering in a store a predetermined number representative of the number of timing pulses to be counted for establishing half the period of the first tone of the set, performing a number of steps of incrementing (or decrementing, depending upon whether the tones of the set are in descending or ascending order, respectively) the contents of the store by respective predetermined numbers representing the respective differences between adjacent ones of the predetermined numbers representing the number of timing pulses to be counted for generating the tones of the set, the number of steps being performed being equal to one less than the sequential position of the selected tone to be generated, and proceeding to generate the desired tone in accordance with the current contents of the store upon completion of said number of steps.

8. A system as claimed in claim 7 wherein the timing pulses are derived from the machine cycles of the processor.

9. A system as claimed in any one of the preceding claims including a timer for determining the basic duration of a tone, and wherein the secondary memory is arranged to generate a tone continuously for one or more times this basic duration as determined by the data for that tone stored in the first memory.

10. A system as claimed in claim 9 wherein said timer is adjustable so as to alter the tempo of generated tone sequences.

11. A system for selecting a tune from a plurality of encoded tunes stored in a memory and generating the tune as an audio signal, substantially as hereinbefore described.



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first two or three bars of the music, provided that by that time the bell push switch has been released. If the caller keeps the bell push switch closed then succeeding notes of the tune are generated. If desired, there may be more than one such break-point in the tune at which the system can automatically switch itself off.

WHAT I CLAIM IS:—

1. A system for selecting a tone or tone sequence from a plurality of encoded tones or tone sequences and generating the tone or tone sequence as an electrical signal, the system comprising: a first memory containing a plurality of tones or tone sequences stored in encoded form in respective locations in the memory; means, including a processor, for generating an electrical signal representing the required tone or tone sequence in response to data read out from a selected one of the locations in the first memory; a second memory forming part of the generating means and having instructions determining the operation of the generating means; a plurality of input stages responsive to applied signals for feeding data to the processor; and a plurality of output stages individually controllable by the processor; the second memory being arranged to control the processor to apply a signal to each of the output stages in turn and to identify, when a selected one of the output stages is in use linked to a selected one of the input stages, the particular input stage at which a signal is received and the particular output stage then supplying the signal to the input stage, each of said respective locations being uniquely associated with a different linking between the input stages and the output stages, and the second memory controlling the read out of data from that location in the first memory corresponding to the identified input stage/output stage linking.

2. A system as claimed in claim 1 wherein the memories are in the form of read only memories.

3. A system as claimed in either claim 1 or claim 2, comprising an external switch arranged to complete the power supply circuit of the system, and a controllable switch responsive to a signal from the processor and arranged to electrically in parallel with the external switch to complete said power supply circuit while the system is operative.

4. A system as claimed in claim 3 wherein said second memory is arranged to provide said signal to the controllable switch and is arranged to cause deactivation of the controllable switch at the end of the selected tone sequence.

5. A system as claimed in claim 3 wherein said second memory is arranged to provide said signal to the controllable switch and is arranged to cause deactivation of the con-

trollable switch at the end of a predetermined succession of tone sequences starting with that tone sequence corresponding to the identified input stage/output stage linking.

6. A system as claimed in claim 3 wherein each tone sequence comprises a plurality of successive segments and wherein said second memory is arranged to provide said signal to cause deactivation of the controllable switch at the end of a segment provided that the external switch is open at that time, the respective last segments of the sequences being disregarded if successive sequences are to be generated and being taken into account if the system is to stop at the end of the selected sequence.

7. A system as claimed in any one of the preceding claims wherein the processor is arranged to generate by the following method the selected tone or a tone of a sequence, the tone to be generated being indicated by a word representing its sequential position with respect to the set of different encoded tones, the method comprising entering in a store a predetermined number representative of the number of timing pulses to be counted for establishing half the period of the first tone of the set, performing a number of steps of incrementing (or decrementing, depending upon whether the tones of the set are in descending or ascending order, respectively) the contents of the store by respective predetermined numbers representing the respective differences between adjacent ones of the predetermined numbers representing the number of timing pulses to be counted for generating the tones of the set, the number of steps being performed being equal to one less than the sequential position of the selected tone to be generated, and proceeding to generate the desired tone in accordance with the current contents of the store upon completion of said number of steps.

8. A system as claimed in claim 7 wherein the timing pulses are derived from the machine cycles of the processor.

9. A system as claimed in any one of the preceding claims including a timer for determining the basic duration of a tone, and wherein the secondary memory is arranged to generate a tone continuously for one or more times this basic duration as determined by the data for that tone stored in the first memory.

10. A system as claimed in claim 9 wherein said timer is adjustable so as to alter the tempo of generated tone sequences.

11. A system for selecting a tune from a plurality of encoded tunes stored in a memory and generating the tune as an audio signal, substantially as hereinbefore described.



* C L M S *

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