

# **SPECIFICATION** **Switching circuit**

This invention relates to semiconductor devices and, in particular, to switching circuits.

Many applications require relays and other types of switches which operate at high voltage and current levels. There have been many attempts to use photoactivated opto-isolators comprising bipolar transistors as substitutes for mechanical relays. It has been generally found that adapting bipolar transistors to the very high voltage and current requirements needed is economically unfeasible, because of the limited voltage-handling capabilities of such transistors.

In an article entitled "A Field Terminated Diode" by Douglas E. Houston et al., published in *IEEE Transactions on Electron Devices*, Vol. ED-23, No. 8 August 1976, there is described a discrete solid-state high voltage switch which includes a region which can be pinched off to provide an "OFF" state or which can be made highly conductive with dual carrier injection to provide an "ON" State. Dual carrier injection refers to the injection of both holes and electrons to form a conductive plasma in the semiconductor.

Gated diode switches can be made with high voltage and current handling capability where as conventional switching amplifiers, whilst they can be made with high current handling capability, generally have only limited voltage handling capability.

In a switching circuit as claimed the capability of the gated diode switch to block a high voltage is combined with the amplification provided by a switching amplifier.

The expression "amplifier/switch" is used in the following description to denote a switching amplifier.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings, of which:—

FIGS. 1 and 2 illustrate a switching circuit in accordance with the invention;

FIGS. 3, 4 and 5 illustrates other switching circuits in accordance with the invention; and

FIG. 6 illustrates a bidirectional switching circuit in accordance with the invention.

Referring now to FIGS. 1 and 2, there is illustrated circuitry 10 coupled between terminals X and Y comprising an amplifier A comprising transistors Q1 and Q2 (which are illustrated connected in a Darlington configuration), a level shifting circuit LS comprising diodes D1 and D2, and a gated diode switch (GDS), illustrated in a semiconductor cross-sectional view in FIG. 1 and by an electrical symbol in FIG. 2. Amplifier A may be denoted as an amplifier/switch. Q1 is a phototransistor whose base region is photosensitive. The emitter of Q1 is coupled to the base of Q2.

Semiconductor substrate 12 and body 16 and regions 18, 20, 22 and 24 are illustrated as  $n$ ,  $p$ -,  $p$ +,  $n$ +,  $p$ , and  $n$ + type conductivity regions,

respectively. Regions 18 and 24 serve as the anode and cathode, respectively, and regions 20 and 12 serve as gate (control terminal) of the GDS. Region 22 serves as a punch-through shield. Electrode regions 28, 30 and 32 are typically aluminium and provide low resistance contact to regions 18, 20 and 24, respectively.

The GDS has a relatively low resistance path between anode region 18 and cathode region 24 when in the ON (conducting) state and a substantially higher impedance when in the OFF (blocking) state. In the ON state the potential of the gate electrode 30 is at or below the potential of the anode 28. Holes are injected into body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. These holes and electrons can be in sufficient numbers to form a plasma which increase the conductivity of body 16 so that the resistance between anode region 18 and cathode region 24 is relatively low when the GDS is operating in the ON state. This type of operation, in which both holes and electrons act as current carriers, is denoted as dual carrier injection.

Region 22 helps limit the punch-through of a depletion layer formed during operation between region 20 and substrate 12 and cathode region 24. Region 22 also helps inhibit formation of a surface inversion layer between regions 24 and 20. In addition, it allows anode region 18 and cathode region 24 to be relatively closely spaced. This results in relatively low resistance between anode region 18 and cathode region 24 during the ON state.

Conduction between anode region 18 and cathode region 24 is inhibited or cut off if the potential of gate electrode 30 is sufficiently more positive than that of anode electrode 28 and cathode electrode 32. The amount of excess positive potential needed to inhibit or cut off conduction is a function of the geometry and impurity concentration levels of structure 10. This positive gate potential causes a sufficient part of body 16 to be depleted so that the potential of this portion of body 16 is more positive than that of the anode 18 and cathode 24 regions. This positive potential barrier cuts off the conductive plasma and inhibits the conduction of holes from anode region 18 to cathode region 24. It also serves to collect electrons emitted at cathode region 24 before they can reach anode region 18. The switch GDS has been fabricated on an  $n$  type substrate having a thickness of 457 to 559 microns and an impurity concentration of  $10^{15}$  to  $10^{16}$  impurities/cm<sup>3</sup>. Body 16 is of  $p$ - type conductivity with a thickness of 30 to 40 microns, a width of 720 microns, a length of 910 microns, and an impurity concentration in the range of  $5 \times 10^{13}$  to  $9 \times 10^{13}$  impurities/cm<sup>3</sup>. The anode region 18 is of  $p$ + type conductivity with a thickness of 2 to 4 microns, and an impurity concentration of  $10^{19}$  impurities/cm<sup>3</sup>. The cathode region 24 is of  $n$ + type conductivity with a thickness of 2 to 4 microns and an impurity

concentration of  $10^{18}$  impurities/cm<sup>3</sup>. The spacing between anode and cathode is typically 120 microns.

Circuitry 10 is useful as an opto-isolator which provides a low or high impedance path between terminals X and Y. The current gain and high current capability of the amplifier A and the high voltage and high current capability of the GDS are combined to provide a high voltage, high current switch. In addition, circuitry 10 provides relatively high electrical isolation between the source of input light (not illustrated) and the X and Y terminals.

The collectors of Q1 and Q2 and the anode of D1 are all coupled together to terminal X. The emitter of Q2 is coupled to the anode of the GDS at a terminal B. The cathode of D2 is coupled to the gate of the GDS at a terminal C. The cathode of the GDS is coupled to terminal Y. The cathode of D1 is coupled to the anode of D2. Transistor Q1 is a phototransistor having a photosensitive base area which serves as an input for circuitry 10. Conduction can occur between the collector and emitter of Q1 if there is sufficient light incident on the photosensitive base of Q1.

As will become clear from the description below, when sufficient light is incident upon the photosensitive base of Q1 there is established a relatively low impedance path between terminals X and Y and conduction from terminal X to terminal Y occurs if terminal X is more positive than terminal Y by a preselected amount. If there is sufficient light signal incident upon the photosensitive base of Q1 then there is essentially an open circuit (a high impedance path) between terminals X and Y.

During an ON (conducting) state of the GDS the potential of anode region 18 is more positive than that of gate regions 12 and 20 and cathode region 24, and there is current flow from anode region 18 through regions 16 and 22 and into cathode region 24. Conduction between anode region 18 and cathode region 24 is inhibited or cut off if the potential of the gate regions 12 and 20 is sufficiently more positive than that of anode region 18 and cathode region 24. The amount of excess positive potential needed to inhibit or cut off conduction is a function of the geometry and impurity concentration levels of the semiconductor regions of the GDS.

Circuitry 10 can be operated to perform a switch function and to serve as an opto-isolator amplifier circuit. If a light signal impinges on the photosensitive base of Q1, then Q1 and Q2 are biased so as to support conduction therethrough. Substrate 12 (the gate of the GDS) and region 24 (the cathode of the GDS) also serve as the collector and emitter, respectively, of a vertical n-p-n transistor with body 16 and region 22 serving as the base. Conduction from anode region 18 to cathode region 24 serves as base current which supports conduction from substrate 12 to cathode region 24. A first conduction path from terminal X through Q1, Q2, region 18 (anode of the GDS) body 16, and regions 22 and 24 (cathode of the

GDS) to terminal Y is established. A second conduction path from terminal X through D1, D2, region 20, substrate 12, body 16, and regions 22 and 24 to terminal X is also established.

The above-described operating condition is achieved by selecting the collector-emitter voltage of Q2 to be less than the combined forward-bias potentials of D1 and D2. This insures that the potential of terminal C (the potential of the gate of the GDS) is less positive than that of terminal B (the potential of the anode of the GDS) during conduction. This insures that conduction can occur between the anode region 18 and cathode region 24.

If the light illuminating the photosensitive base of Q1 is removed, then Q1 and Q2 are biased off and the flow of current therethrough ceases. The potential of terminal B now falls below that of terminal C such that the GDS is switched to the OFF state. This cuts off all conduction between terminals X and Y. Thus there is a relatively high impedance between terminals X and Y at this time. Most of the voltage drop between terminals X and Y is across the anode region 18 (terminal B) and the cathode region 24 (terminal Y) and only a relatively modest amount exists across the collector-emitter of Q2. The voltage across the collector-emitter of Q2 is such that the potential of terminal B is sufficiently less positive than that of terminal C to insure that the GDS is biased to the OFF state.

From the foregoing it can be appreciated that level shifting circuit LS provides self-biasing for the GDS gate without the need for a separate bias source. It further provides an alternate current path during the ON state which reduces high current flow through the amplifier A.

Referring now to FIG. 3, there is illustrated circuitry 100 coupled between terminals X1 and Y1 which is very similar to that of circuitry 10. Circuitry 100 comprises an amplifier A1, a gated diode switch (GDS1), and a level shifting circuit means LS1. A1 comprises a p-n-p transistor Q3 and an n-p-n transistor Q4 and may be denoted as an amplifier/switch. The emitter of Q3 is coupled to the collector of Q4 and the collector of Q3 is coupled to the base of Q4. LS1 comprises serially connected p-n diodes D3 and D4. The base of transistor Q3 (input terminal D1) is not photosensitive as is transistor Q1 of FIG. 1. The operation of circuitry 100 is very similar to that of circuitry 10 except that the input signal is coupled to the base of Q3 via an electrical connection and not via a light path and the gain of amplifier A1 may be different from the gain of amplifier A.

Referring now to FIG. 4, there is illustrated circuitry 102 coupled between terminals X2 and Y2 which is very similar to circuitry 100. Circuitry 102 comprises amplifier A2 which comprises a junction field effect transistor Q5 whose gate is coupled to an input terminal 12. A2 may be denoted as an amplifier/switch. It further comprises a level shifting circuit means LS2 which comprises a p-n diode D5 and further comprises a gated diode switch (GDS 2). The basic difference

between circuitry 102 and 100 is that junction field effect transistor Q5 is substituted for Q3 and Q4 and a single diode D5 is used instead of diodes D3 and D4. The operation of circuitry 102 is very similar to that of circuitry 100 of FIG. 3 except the gain of amplifier A3 may be somewhat different from the gain of A2 of FIG. 3.

Referring now to FIG. 5, there is illustrated circuitry 104 coupled between terminals X5 and Y5 comprising amplifier A5, level shifting circuit means LS5, and a gated diode switch (GDS5). A5 comprises a p-n-p transistor Q5 and LS5 comprises a p-n diode D10. A5 may be denoted as an amplifier/switch. Circuitry 104 is very similar to circuitry 102 of FIG. 4 except that p-n-p transistor Q8 is used instead of junction field effect transistor Q5 and diode D10 is used instead of diode D5. The operation of circuitry 104 is very similar to that of circuitry 102 but the gain of A5 may be different from the gain of A2.

Referring now to FIG. 6, there is illustrated circuitry 106 coupled between terminals X3 and Y3 comprising amplifiers A3 and A4, gated diode switches GDS3 and GDS4, level shifting circuit means LS3 and LS4 comprising diodes D6 and D8, respectively, and first and second unidirectional circuit means comprising diodes D7 and D9. A3 and A4 may each be denoted as an amplifier/switch. Circuitry 106 is capable of being operated as a bilateral switch which couples terminals X3 and Y3. Current flow can be achieved from terminal X3 to Y3 or in the reverse direction.

In one illustrative embodiment of circuitry 106, amplifier A3 comprises an n-p-n transistor Q6 whose base region is photosensitive and amplifier A4 comprises an n-p-n transistor Q7 whose base is also photosensitive. The combination of A3, GDS3, and D6 and the combination of A4, GDS4 and D8 are both configured in essentially the same manner as A, GDS and LS of FIGS. 1 and 2, and function in essentially the same manner. The collector of Q6 is coupled to the anode of D6, the cathode of D7, and to terminal X3. The emitter of Q6 is coupled to the anode of GDS3, the cathode of GDS4, and to a terminal U. The collector of Q7 is coupled to the anode of D8, the cathode of D9, and to terminal Y3. The emitter of Q7 is coupled to the anode of GDS4, the cathode of GDS3, and to a terminal V. The cathodes of D6 and D8 and the gates of GDS3 and GDS4 are all coupled together to a terminal W.

If the terminal X3 is more positive in potential than Y3 and there is a light signal incident upon the photosensitive base of Q6, there is conduction from terminal X3 through Q6 and D6 and through GDS3 into the cathodes of GDS3 and then through D9 and into terminal Y3. The impedance between terminals X3 and Y3 with a light signal applied to the photosensitive base of Q6 is relatively low.

If terminal Y3 is more positive in potential than X3 and there is a light signal applied to the photosensitive base of Q7, there is conduction from terminal Y3 through Q7 and D8, and into

GDS4 and then through D7 and into terminal X3. The impedance between terminals Y3 and X3 with a light signal applied to the photosensitive base of Q7 is relatively low.

It is thus clear that circuitry 106 provides a bilateral switching function which also introduces gain.

The embodiments described herein are intended to be illustrative of the general principles of the invention. Various modifications are possible. For example, the amplifier(s) can be a single n-channel or p-channel MOS transistor and the level shifting circuit means can be an MOS-type diode equivalent. Still further, the amplifier(s) can be a pair of n-p-n transistors coupled together in a Darlington configuration. Still further, the amplifier/switch(es) can be considerably more complex than just one or two transistors and the level shifting circuit means can likewise be more complex than just one or two diodes. Still further, the amplifier/switch(es) and level shifting circuit means can be formed from components other than junction or field effect transistors or diodes.

#### CLAIMS

1. A switching circuit including: a gated diode switch comprising a semiconductor body having a bulk portion of a first conductivity type, a first region of the first conductivity type, a second region of a second conductivity type opposite to the first conductivity type and constituting a first output point of the circuit and a gate region of the second conductivity type, the first second and gate regions being mutually disjoint regions within the body and having resistivities lower than the resistivity of the bulk portion; a switching amplifier connected between a second output point of the circuit and the first region; and level shifting means connected between the second output point and the gate region; whereby in operation, with suitable voltages applied to the output points of the circuit, when the amplifier is in the "OFF" state a depletion region is formed in the bulk portion of the body substantially preventing current flow between the first and second regions, and when the amplifier is in the "ON" state current flow between the first and second regions is facilitated by injection into the bulk portion of majority carriers from the first region and minority carriers from the second region.

2. A circuit as claimed in claim 1 wherein the level shifting means comprises one or more semiconductor diodes connected in series.

3. A circuit as claimed in claim 1 or claim 2 wherein the amplifier comprises transistors connected as a Darlington pair.

4. A circuit as claimed in claim 1 or claim 2 wherein the amplifier is responsive to an optical signal.

5. A circuit as claimed in claim 4 wherein the amplifier comprises transistors connected as a Darlington pair, the first transistor of the pair being a phototransistor.

6. A switching circuit substantially as herein described with reference to any of FIGS. 2 to 5 of



between circuitry 102 and 100 is that junction field effect transistor Q5 is substituted for Q3 and Q4 and a single diode D5 is used instead of diodes D3 and D4. The operation of circuitry 102 is very similar to that of circuitry 100 of FIG. 3 except the gain of amplifier A3 may be somewhat different from the gain of A2 of FIG. 3.

Referring now to FIG. 5, there is illustrated circuitry 104 coupled between terminals X5 and Y5 comprising amplifier A5, level shifting circuit means LS5, and a gated diode switch (GDS5). A5 comprises a p-n-p transistor Q5 and LS5 comprises a p-n diode D10. A5 may be denoted as an amplifier/switch. Circuitry 104 is very similar to circuitry 102 of FIG. 4 except that p-n-p transistor Q8 is used instead of junction field effect transistor Q5 and diode D10 is used instead of diode D5. The operation of circuitry 104 is very similar to that of circuitry 102 but the gain of A5 may be different from the gain of A2.

Referring now to FIG. 6, there is illustrated circuitry 106 coupled between terminals X3 and Y3 comprising amplifiers A3 and A4, gated diode switches GDS3 and GDS4, level shifting circuit means LS3 and LS4 comprising diodes D6 and D8, respectively, and first and second unidirectional circuit means comprising diodes D7 and D9. A3 and A4 may each be denoted as an amplifier/switch. Circuitry 106 is capable of being operated as a bilateral switch which couples terminals X3 and Y3. Current flow can be achieved from terminal X3 to Y3 or in the reverse direction.

In one illustrative embodiment of circuitry 106, amplifier A3 comprises an n-p-n transistor Q6 whose base region is photosensitive and amplifier A4 comprises an n-p-n transistor Q7 whose base is also photosensitive. The combination of A3, GDS3, and D6 and the combination of A4, GDS4 and D8 are both configured in essentially the same manner as A, GDS and LS of FIGS. 1 and 2, and function in essentially the same manner. The collector of Q6 is coupled to the anode of D6, the cathode of D7, and to terminal X3. The emitter of Q6 is coupled to the anode of GDS3, the cathode of GDS4, and to a terminal U. The collector of Q7 is coupled to the anode of D8, the cathode of D9, and to terminal Y3. The emitter of Q7 is coupled to the anode of GDS4, the cathode of GDS3, and to a terminal V. The cathodes of D6 and D8 and the gates of GDS3 and GDS4 are all coupled together to a terminal W.

If the terminal X3 is more positive in potential than Y3 and there is a light signal incident upon the photosensitive base of Q6, there is conduction from terminal X3 through Q6 and D6 and through GDS3 into the cathodes of GDS3 and then through D9 and into terminal Y3. The impedance between terminals X3 and Y3 with a light signal applied to the photosensitive base of Q6 is relatively low.

If terminal Y3 is more positive in potential than X3 and there is a light signal applied to the photosensitive base of Q7, there is conduction from terminal Y3 through Q7 and D8, and into

GDS4 and then through D7 and into terminal X3. The impedance between terminals Y3 and X3 with a light signal applied to the photosensitive base of Q7 is relatively low.

It is thus clear that circuitry 106 provides a bilateral switching function which also introduces gain.

The embodiments described herein are intended to be illustrative of the general principles of the invention. Various modifications are possible. For example, the amplifier(s) can be a single n-channel or p-channel MOS transistor and the level shifting circuit means can be an MOS-type diode equivalent. Still further, the amplifier(s) can be a pair of n-p-n transistors coupled together in a Darlington configuration. Still further, the amplifier/switch(es) can be considerably more complex than just one or two transistors and the level shifting circuit means can likewise be more complex than just one or two diodes. Still further, the amplifier/switch(es) and level shifting circuit means can be formed from components other than junction or field effect transistors or diodes.

#### CLAIMS

1. A switching circuit including: a gated diode switch comprising a semiconductor body having a bulk portion of a first conductivity type, a first region of the first conductivity type, a second region of a second conductivity type opposite to the first conductivity type and constituting a first output point of the circuit and a gate region of the second conductivity type, the first second and gate regions being mutually disjoint regions within the body and having resistivities lower than the resistivity of the bulk portion; a switching amplifier connected between a second output point of the circuit and the first region; and level shifting means connected between the second output point and the gate region; whereby in operation, with suitable voltages applied to the output points of the circuit, when the amplifier is in the "OFF" state a depletion region is formed in the bulk portion of the body substantially preventing current flow between the first and second regions, and when the amplifier is in the "ON" state current flow between the first and second regions is facilitated by injection into the bulk portion of majority carriers from the first region and minority carriers from the second region.

2. A circuit as claimed in claim 1 wherein the level shifting means comprises one or more semiconductor diodes connected in series.

3. A circuit as claimed in claim 1 or claim 2 wherein the amplifier comprises transistors connected as a Darlington pair.

4. A circuit as claimed in claim 1 or claim 2 wherein the amplifier is responsive to an optical signal.

5. A circuit as claimed in claim 4 wherein the amplifier comprises transistors connected as a Darlington pair, the first transistor of the pair being a phototransistor.

6. A switching circuit substantially as herein described with reference to any of FIGS. 2 to 5 of

the accompanying drawings.

7. A circuit as claimed in any of the preceding claims wherein the gated diode switch is substantially as herein described with reference to

5 FIG. 1 of the accompanying drawings.

8. A bidirectional switching circuit comprising a pair of circuits as claimed in any of the preceding claims, the first output point of each circuit of the pair being connected to the second output point of

10 the other circuit of the pair.

9. A bidirectional switching circuit as claimed in claim 8 wherein the first output point of each circuit of the pair is connected to the second

output point of the other circuit of the pair via

15 unidirectional conducting means.

10. A bidirectional switching circuit as claimed in claim 9 wherein the first region of each circuit of the pair is connected to the second region of the other circuit of the pair.

20 11. A bidirectional switching circuit as claimed in any of the claims 8 to 10 wherein the gate regions of the circuits of the pair are connected together.

12. A bidirectional switching circuit

25 substantially as herein described with reference to FIG. 6 of the accompanying drawings.

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