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WAFER LEVEL PACKAGE FOR SEMICONDUCTOR DEVICES

BACKGROUND

[0001] This invention relates generally to an integrated circuit (IC) device and a method of manufacturing the IC device. More particularly, this invention relates to an IC device including one die or two or more dies arranged in a matrix array package configuration so as to achieve very high pin counts and multiple functionality with in the defined device geometry, and to a method of manufacturing such an IC device.

[0002] With the miniaturization of electronic products, there is a need to also reduce the size of IC packaged devices and to add more functionality so that more of these IC devices can be packed into a given area of a substrate. Two approaches have been taken to meet such a need. A first approach is to reduce the size of packaging of existing IC device packages. The second approach is focused on increasing the functionalities provided by each IC device, for example to form system-on-a-chip (SOC) and system-in-package (SIP) devices.

[0003] Figures 1A- 1F show prior art IC devices fabricated in a wafer level configuration. Each individual device is packaged while they are still available in wafer form, prior to the wafer dicing process to obtain chip sized package. Many packaging process steps are added directly on a wafer to realize these chip sized packages, which are of small form factor and reduced weight. However, the IC device obtained in this method are limited to the IO density as the chip size determines the package IO density

[0004] U.S. Patent No. 6,040,235 discloses an IC device having a footprint approximately the size of a die of the IC device. The steps for manufacturing the IC device includes: (1) providing a wafer that includes multiple dies wherein each die includes multiple connection pads, (2) sandwiching the wafer between two protective layers, (3) cutting notches through one of the protective layers along outlines of the dies to expose portions of the connection pads, (4) forming metal contacts on the surface of the notched protective layer that are electrically connected to the exposed portions of the connection pads, and (5) separating the dies to form individual dies. Such a manufacturing process suffers from a number of disadvantages. The step of cutting notches is sequential and therefore is time-consuming. That step also requires an accurate fixed angular shaped cutting blade for cutting the notches. As cutting produces debris, the cutting step has to be performed outside of a clean room. A cut wafer is then transported into the clean room for further processing, making handling of the wafer cumbersome. The two protective layers on a resultant die also make it costly.

[0005] U.S. Patent No. 6,117,707 discloses another IC device having multiple dies similar to that disclosed in U.S. Patent No. 6,040,235. The dies are arranged in a stacked configuration. Interconnections between the dies of such an IC device are formed only after

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the stacks of dies are separated to form individualized IC devices. That is, the process of interconnecting the dies in a device is performed on a device level and is thus slow.

SUMMARY

[0006] According to an aspect of the present invention, there is provided a method of manufacturing an integrated circuit (IC) device. According to the method, a first wafer including multiple dies separated by separation zones is first provided. Each die includes connection pads on a first active side of the wafer. High aspect ratio micro structures are provided at the die peripheral lines, adjacent to each bond pads formed along the separation zones. Routers are also formed for electrically connecting with the connection pads to route the connection pads to an interior of the corresponding micro structures. Wafer material is then removed from a second side of the wafer, opposite the first side, to expose the routers in the micro structures. Contacts are formed on the second side of the wafer. These contacts are electrically connected to the routers in the interior of the micro structures to thereby electrically connect with the bond pads on the first side. The dies are separated along the separation zones to produce individualized dies, each of which serves as an IC device.

[0007] Preferably, the method may further include forming a passivation layer prior to forming the routers so that the routers are separated from the dies by the passivation layer.

[0008] Preferably, removing wafer material includes removing wafer material from a second side of the wafer, opposite the first side, to expose the passivation layer in the interior of the micro structures. A second passivation layer is then formed on the second side of the wafer to contact the passivation layer in the interior of the micro structures. Thereafter, portions of the passivation layers are removed from the second side of the wafer to expose the routers in the micro structures.

[0009] The method may further include forming terminals electrically connected to the contacts. Preferably, forming terminals includes forming a solder mask over the passivation layer and contacts on the second side of the wafer, removing portions of the solder mask over the contacts to expose the contacts and forming solder bumps over the exposed contacts.

[0010] Preferably, the method may further include attaching a packaging layer to the first side of the wafer after forming the routers. In such a case, separating the dies includes separating the packaging layer.

[0011] The method may further include providing a second wafer of dies processed in a manner similar to the first wafer to include routers that route connection pads on a first side of the second wafer to corresponding contacts on the second side of the second wafer. The second wafer is then attached to the first wafer by aligning and attaching the first side of the second wafer to the second side of the first wafer to thereby electrically connect connection pads on the dies of the second wafer to the contacts on the second side of corresponding dies of the first wafer to define stacks of dies. The second side of the second wafer is

processed in a similar manner to the first wafer to produce contacts thereon. In such a case, separating the dies includes separating the stacks of dies to produce individualized integrated circuit devices, each of which includes a stack of dies.

[0012] Preferably, the method further includes providing at least one intermediate wafer interconnected between the first wafer and the second wafer.

[0013] According to another aspect of the present invention, there is provided an integrated circuit (IC) device manufactured according to the method described above. This IC device includes a first die having multiple connection pads on a first active side of the first die and multiple contacts on a second side of the first die, opposite the first side. The IC device also includes multiple routers, each of which electrically connects a connection pad to a corresponding contact, wherein the routers run along recesses formed on at least one sidewall of the first die.

[0014] Preferably, the recesses are formed on an upper portion of the sidewall adjacent to the first side of the die, leaving a lower portion of the sidewall adjacent to the second side of the die substantially planar.

[0015] Preferably, the IC device further includes a passivation layer on the first side of the first die between the die and the routers.

[0016] Preferably, the IC device further includes a second passivation layer on the second side of the first die between the die and the routers.

[0017] Preferably, the IC device further includes terminals electrically connected to the contacts. In such a case, the IC device may further include a solder mask on the second side of the first die covering areas on the second side exposed by the terminals.

[0018] Preferably, the IC device may further include a packaging layer attached to the first side of the die.

[0019] Preferably, the IC device may further include a second die having routers that route connection pads on a first side of the second die to contacts on a second side, opposite the first side, of the second die. The first side of the second die is attached to the second side of the first die to thereby electrically connect connection pads on the second die to the contacts on the second side of the first die to define a stack of dies. The IC device may further include at least one intermediate die interconnected between the first die and the second die.

BRIEF DESCRIPTION OF DRAWINGS

[0020] The invention will be better understood with reference to the drawings, in which:

Figure 1 is a sectioned drawing of a prior art IC device having two dies in a stacked configuration and connected to a substrate using wire bonding;

Figure 2 is a sectioned drawing of a prior art IC device having three dies, stacked and connected to a substrate in a similar manner as the IC device in Figure 1;

Figure 3 is a sectioned drawing of another prior art IC device having multiple dies in a stacked configuration and interconnected using metal-filled through holes;

Figure 4 is a flow diagram of a sequence of steps for manufacturing an IC device according to an embodiment of the present invention;

Figure 5 is a schematic drawing of a device showing its original bond pads and peripheral lines adjacent to the bond pads;

Figure 6 is a schematic drawing of a device cross section showing street lines between the active device peripheral, adjacent to the bond pads:

Figure 7 is a schematic drawing of a device cross section showing high aspect ratio micro structures at the device peripheral, adjacent to the bond pads. Each micro etched structure represents a corresponding bond pad:

Figure 8 is a schematic drawing of a device cross section showing 1st layer deposition of an insulation at the micro structures;

Figure 9 is a schematic drawing of a device cross section showing extension of original bond pads to the micro structures with the help of metal routing;

Figure 10 is a schematic drawing of a device cross section showing a second layer of insulation and or a polymer adhesive layer covering the exposed bond pads, routing lines and micro structures:

Figure 11 is a schematic drawing of a device cross section showing a second substrate attached over the 1st side of the 1st active device:

Figure 12 is a schematic drawing of a device cross section showing a thinned 1st active device wafer at the back or second side;

Figure 13 is a schematic drawing of a device cross section showing a deposited layer of insulation / passivation on the second side of the 1st active device wafer after thinning;

Figure 14 is a schematic drawing of a device cross section showing removed insulation / passivation layer at the micro structures to expose the routed metal traces;

Figure 15 is a schematic drawing of a device cross section showing a thin film metal deposition on the second side of the 1st active device wafer connecting the metal routers on the first side at the micro structures;

Figure 16 is a schematic drawing of a device cross section showing solder bump pads defined by patterning on the 2nd side metal film of the 1st active device wafers;

Figure 17 is a schematic drawing of a device cross section showing a deposited solder mask thin film with bump pad openings at the second side of the 1st active device wafer;

Figure 18 is a schematic drawing of a device cross section showing a UBM structures along with solder bumps at the bump pad locations;

Figure 19 is a schematic drawing of a device cross section showing a diced wafer level package separating each individual processed device;

Figure 20 is a schematic drawing of a device cross section showing a wafer level package with another embodiment body, where in the active portion of the device on the first side is kept clear of any contacts from 2nd substrate, or by any polymeric adhesives and or epoxy materials as desired by the product application.

DETAILED DESCRIPTION

[0021] Figure 4 is a flow diagram showing a sequence 2 of steps for manufacturing an integrated circuit (IC) device 4 (Figures 19) according to an embodiment of the present invention. The sequence 2 starts in a PROVIDE WAFER step 6, wherein a wafer 8 (Figure 5) including an array of finished dies 10 formed therein by conventional techniques is provided. The wafer 8 may be a six, eight or twelve-inch wafer. Separation zones, generally known as scribe lines 11 that are typically more than 50 microns wide, separate the dies 10. Each die 10 has multiple bond pads or connection pads 23 (Figure 6) on a first active surface 12 of the die 10. These connection pads 23 are electrically connected to an electronic circuitry (not shown) formed in each die 10. A side of the wafer 8, which defines the first active surfaces 12 of the dies 10, is referred herein as the first active side 21 of the wafer 8. The other side of the wafer 8, opposite the first side 21, is referred to herein as the second side 29 of the wafer 8. Figure 6 shows a cross sectional view of two adjacent dies 10 of the wafer 8 prior to processing.

[0022] The sequence 2 next proceeds to a FORM MICROSTRUCTURES step 20, wherein microstructures 31 and 33 are formed adjacent to corresponding connection pads 23 along the scribe lines 11 as shown in Figures 7. The microstructures 31 and 33 have a depth in the range of 20 -50 microns and preferably have a rectangular opening on a surface of the first side 21 of the wafer 8. Microstructures with a circular, square, hexagonal or any other shape may also be used. These microstructures can be formed using conventional techniques, such as photolithography followed by silicon removal processes. The microstructures 31 and 33 extend deeper into the first side 21 of the wafer 8 than the connection pads 23. In this embodiment, each connection pads 23 is connected with one microstructure on the scribe line area.

[0023] The sequence 2 next proceeds to a first FORM PROTECTIVE LAYER step 24, wherein an insulation / passivation layer 35 is formed only at the microstructure 31 and 33 of the dies 10. Such a localized INSULATION / passivation layer 35 is preferably formed by first depositing a layer of silicon dioxide according to a DEPOSIT LAYER step 28. Any appropriate passivation process having an operating temperature between Room Temperature to 450 degree Celsius may be used in this step 28, depending on the application of the IC device. Figure 8 shows the surface on the first side 21 of the wafer 8 covered by the localized passivation layer 35.

[0024] Next, a layer 37 of metal, such as aluminum, is deposited over the passivation layer covered surface of the wafer 8 in a FORM ROUTERS step 34. The metal layer 37 is

deposited using any conventional technique, such as sputter deposition, to cover the surface of the first side 21 of the wafer 8. The layer 37 of metal covers the exposed surfaces of the connection pads 23 and extends into the microstructures 31, 33. The metal layer 37 is then patterned, again, using any conventional technique, such as photolithography patterning to form mutually electrically insulated interconnections or routers 37 that route the connection pads 23 to the interior of their corresponding microstructures. Preferably, these routers 37 are treated, for example by plating with nickel or copper, to increase their thickness to about 3-5 microns. Depending on the application of the IC device, the metal layer 37 may also be of a metal alloy in the form of a paste that is screen printed as routers 37. An optional passivation layer 39 may be applied over the routers as another protective layer.

[0025] Preferably, the sequence 2 next proceeds to an APPLY EPOXY step 42, wherein an epoxy layer 41 is applied, for example by spin-coating or screen-printing, onto the router patterned surface of the wafer 8, as shown in Figure 10. After the epoxy layer 41 is applied, a packaging layer 43, such as of glass, alumina, beryllium, sapphire, ceramic, silicon, germanium or other suitable materials, is attached to the epoxy layer 41 in an ATTACH PACKAGING LAYER step 48. The epoxy layer may be required to be patterned using lithography when manufacturing optically sensitive devices. The epoxy layer 41 cures to rigidly bond the packaging layer 43 to the wafer 8 as shown in Figure 11.

[0026] After attachment of the packaging layer 43, wafer material on the second side 29 of the wafer 8 is removed in a REMOVE WAFER MATERIAL step 50. In this step 50, the wafer material on the second side 29 of the wafer 8 is preferably first ground, by backgrinding and / or polishing in a GRIND WAFER step 52, to reduce the thickness of the wafer 8 to leave about 40 – 70 microns thick of wafer material between the ground surface on the second side 29 of the wafer 8 and the bottom of the microstructures 31, 33. Thereafter, the 40 – 70 micron thick wafer material on the second side 29 of the wafer 8 is preferably etched, in a STRESS REMOVAL step 54, to further remove the remaining wafer material 45 until the passivation layer 47 at the microstructures is exposed as shown in Figure 12.

[0027] Next, the etched surface 45 at the second side 29 of the wafer 8 is coated with a second passivation layer 49 in a second FORM PROTECTION LAYER step 58 as shown in Figure 13. This second passivation layer 49 comes into contact with the exposed passivation layer 47 at the microstructures. Portions of the passivation layers 47, 49 on the second side of the wafer covering the metal layer 37 at the microstructures 31,33 are then removed in a second REMOVE PASSIVATION LAYER PORTIONS step 60 to expose the metal layer 51 at the microstructures as shown in Figure 14.

[0028] The sequence 2 next proceeds to a FORM CONTACTS step 62, wherein mutually electrically insulated contacts 53 (Figures 15) are formed on the processed second side 29 of the wafer 8. These contacts 53 are electrically connected to the metal layer 47 in the corresponding microstructures to thereby route the connection pads 23 on the first side 21

to the second side 29 of the wafer. Such a step 62 preferably includes first forming, such as by depositing, a second metal layer 53 over the passivation layer 49 at the second side 29 of the wafer in a FORM METAL LAYER step 66. Figure 15 shows the second metal layer 53 covering the surface of the second side 29 of the wafer 8. This second metal layer 53 comes into contact with the metal layer 47 at the microstructures to thereby electrically connect therewith. Thereafter, the second metal layer 53 is patterned in a PATTERNING METAL LAYER step 68 using any conventional technique to define mutually electrically insulated routers that functions as contacts 55 on the surface of the second side 29 of the wafer 8. In this manner, the connection pads 23 on the first side 21 of the wafer 8 are electrically routed to the contacts 55 on the second side 29 of the wafer 8 as shown in Figure 16.. Preferably, the contacts 55 are coated with a layer of nickel followed by a layer of gold using an under bump metallization (UBM) process.

[0029] The sequence 2 next proceeds to a FORM TERMINALS step 72, wherein the wafer 8 is further processed to include electrical terminals such as solder bumps 74 (Figure 7N). Preferably, this step 72 includes a FORM SOLDER MASK step 76, wherein the surface on the second side 29 of the wafer is coated with a layer of solder mask 59 or a third passivation layer, preferably 1 to 25 micron thick as shown in Figure 17. Portions 61 of the solder mask 59 or the third passivation layer covering the contacts 55 are next removed using any conventional technique in a REMOVE SOLDER MASK PORTIONS step 80 to expose the contacts 55. The solder bumps 65 are then formed in a FORM SOLDER BUMPS step 82 over the contacts 55 on the second side 29 of the wafer 8 to function as terminals for the dies 10, as shown in Figure 18. The sequence 2 finally ends in a SEPARATE DIES step 84, wherein the wafer 8 with the attached packaging layer 43 is diced along the scribe lines 11, in between the microstructures 31, 33 to produce individualized IC devices ready for mounting on a substrate (not shown). Figure 19 shows three resultant individualized IC devices.

[0030] It should be noted that the IC device produced according to the sequence 2 is only one possible embodiment of the present invention. IC devices, such as IC device shown in Figure 20, according to other embodiments can also be manufactured. Here in this embodiment, the active portion of the device area other than bond pads are kept away from the 2^{nd} substrate and or any polymeric materials contact.

CLAIMS

I claim:

1. A method of manufacturing an integrated circuit (IC) device comprising:

providing a first wafer including a plurality of dies separated by separation zones, each of the plurality of dies including connection pads on a first active side of the wafer;

forming a plurality of microstructures along the separation zones, the plurality of microstructures corresponding to the connection pads;

forming routers that electrically connect the connection pads to route the connection pads to corresponding microstructures;

removing wafer material from a second side, opposite the first side, to expose the routers at the microstructures;

forming contacts on the second side of the wafer, the contacts being electrically connected to the routers in the interior of the microstructures to thereby electrically connect with the connection pads on the first side; and

separating the dies along the separation zones to produce individualized dies, each of which serves as an IC device.

2. A method according to Claim 1, further comprising forming individual high aspect ratio microstructures that represent each connection pads on the active dies

3. A method according to Claim 2, further comprising forming an insulation / passivation layer prior to forming the routers so that the routers are separated from the dies by the passivation layer.

4. A method according to Claim 3, wherein removing wafer material includes:

removing wafer material from a second side of the wafer, opposite the first side, to expose the insulation / passivation layer under the routers at the microstructures;

forming a second insulation / passivation layer on the second side of the wafer to contact the passivation layer in the interior of the microstructures and

removing portions of the insulation / passivation layers from the second side of the wafer to expose the routers at the microstructures

5. A method according to Claim 4, further comprising forming terminals electrically connected to the contacts.

6. A method according to Claim 5, wherein forming terminals includes:

forming one of a solder mask and a third passivation layer over the second passivation layer and contacts on the second side of the wafer;

removing portions of the one of the solder mask and the third passivation layer over the contacts to expose the contacts; and

forming solder bumps over the exposed contacts.

7. A method according to Claim 1, further comprising attaching a packaging layer to the first side of the wafer after forming of the routers.

8. A method according to claim 7, wherein separating the dies includes separating the packaging layer.

9. A method according to Claim 1, further comprising:

providing a second wafer of dies processed in a manner similar to the first wafer to include routers that route connection pads on a first side of the second wafer to corresponding contacts on the second side of the second wafer;

aligning and attaching the first side of the second wafer to the second side of the first wafer to thereby electrically connect connection pads on the dies of the second wafer to the contacts on the second side of corresponding dies of the first wafer to define stacks of dies;

processing the second side of the second wafer in a similar manner to the first wafer to produce contacts thereon; and wherein separating the dies includes separating the stacks of dies to produce individualized integrated circuit devices, each of which includes a stack of dies.

10. A method according to Claim 9, further comprising providing at least one intermediate wafer interconnected between the first wafer and the second wafer.

11. A method according to claim 1, wherein the said invention method allows active wafers with 5 micron bond pads and 10 micron bond pitch that may be expected in the future device manufacturing.

12. A method according to claim 1, wherein the said invention method allows active wafers with less than 50 micron scribe line width as the microstructures can be as small as 5 micron in size.

13. A method according to claim 1, wherein the said invention method allows backside processing of wafers for passive components such as resistors, inductors and capacitors before the final solder bump contacts are made.

14. A method according to claim 1, wherein the said invention method allows very fine pitch bumping at the back side of the chip using organic build-up layer methods.