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- (71) Applicant: TELEFONAKTIEBOLAGET L M ERICSSON (PUBL) [SE/SE]; S-164 83 Stockholm (SE).
- (72) Inventors: KÄLLMAN, Stig; Olstorpögatan 3, S-692 71 Kumla (SE). BERGSTEN, Tomas; Bygatan 31, S-516 93 Rångedala (SE).
- (74) Agent: SJÖBERG, Mats; Ericsson AB, Patent Unit Kista, RAN Implementation & Core (PU-KRIC), S-164 80 Stockholm (SE).
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(54) Title: SELECTIVE PARTITIONING OF VIA STRUCTURES IN PRINTED CIRCUIT BOARDS

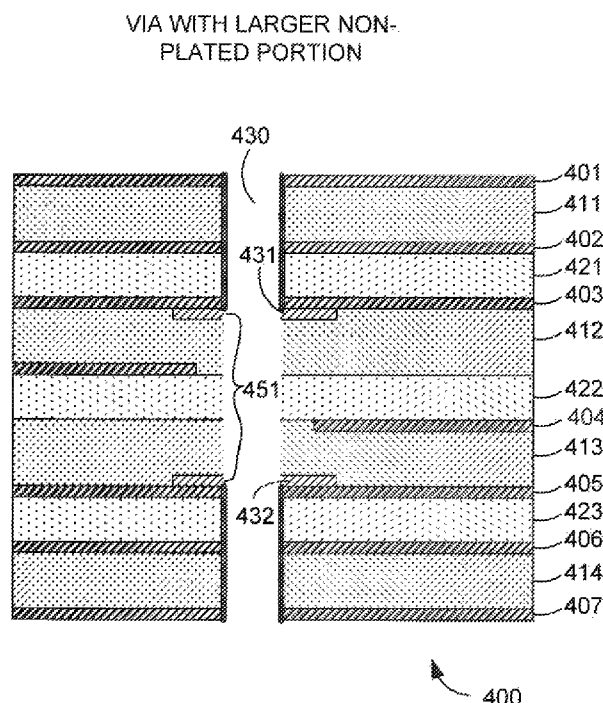


Figure 4

(57) Abstract: The embodiments herein relates to a method for selective partitioning of a via in a printed circuit board (200) as to produce an electrically isolating portion between two electrically conducting portions in said via. The method involves the step of prior to drilling the hole for the via (240), laminating plating resist layers (233,234) to the printed circuit board (200) at a distance from each other corresponding to the desired length of the electrically isolated portion of the via. After drilling, copper is added to selected portions of the interior of the via (240) in two different processing steps followed by a step of removing undesired copper as to produce the electrically isolating portion.



EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
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