EFFICIENT UTILIZATION OF MEMORY DIE AREA

CROSS REFERENCE

[0001] The present Application for Patent claims priority to U.S. Patent Application No. 15/434,395 by Laurent, entitled "Efficient Utilization of Memory Die Area," filed on February 16, 2017, assigned to the assignee hereof.

BACKGROUND

[0002] The following relates generally to memory devices and more specifically to efficient utilization of die area for three-dimensional cross-point architecture.

[0003] Memory devices are widely used to store information in various electronic devices such as computers, wireless communication devices, cameras, digital displays, and the like. Information is stored by programing different states of a memory device. For example, binary devices have two states, often denoted by a logic "1" or a logic "0." In other systems, more than two states may be stored. To access the stored information, the electronic device may read, or sense, the stored state in the memory device. To store information, the electronic device may write, or program, the state in the memory device.

[0004] Multiple types of memory devices exist, including magnetic hard disks, random access memory (RAM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), read only memory (ROM), flash memory, phase change memory (PCM), and others. Memory devices may be volatile or non-volatile. Non-volatile memory, e.g., FeRAM and PCM, may maintain their stored logic state for extended periods of time even in the absence of an external power source. Volatile memory devices, e.g., DRAM, may lose their stored state over time unless they are periodically refreshed by an external power source. Improving memory devices may include increasing memory cell density, increasing read/write speeds, increasing reliability, increasing data retention, reducing power consumption, or reducing manufacturing costs, among other metrics.

[0005] FeRAM may use similar device architectures as volatile memory but may have non-volatile properties due to the use of a ferroelectric capacitor as a storage device. FeRAM devices may thus have improved performance compared to other non-volatile and volatile memory devices. PCM or chalcogenide-material-based memories may be non-volatile and

may offer improved read/write speeds and endurance compared to other memory devices. PCM or chalcogenide-material-based memories may also offer increased memory cell density capabilities. For example, three-dimensional memory arrays employing FeRAM, PCM, or chalcogenide-material-based memories may be possible. However, in some three-dimensional architectures, regions of the memory device may be dedicated to support circuitry and may be exclusive of memory cells. Such areas may increase the physical dimensions of the memory device without increasing the capacity of the memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The disclosure herein refers to and includes the following figures:

[0007] FIG. 1 illustrates an example of a memory device that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0008] FIG. 2 illustrates an example of a memory device having a three-dimensional array of memory cells that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0009] FIG. 3 illustrates an example of a memory array that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0010] FIG. 4 illustrates an example of a memory device that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0011] FIG. 5 illustrates an example of a cross-section of the memory device of FIG. 4 along line 5-5.

[0012] FIG. 6 illustrates an example of memory tile configurations that support efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0013] FIG. 7 illustrates an example of a memory tile of a group of memory times that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0014] FIG. 8 illustrates examples of boundary tile configurations that support efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0015] FIG. 9 illustrates an example of a memory device that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0016] FIG. 10 illustrates an example of a cross-section of the memory device of FIG. 9 along line 10-10.

[0017] FIG. 11 illustrates an example of a boundary tile configuration that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0018] FIG. 12 illustrates an example of a memory portion that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0019] FIG. 13 illustrates an example of a memory portion that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0020] FIG. 14 illustrates an example of a memory portion that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0021] FIG. 15 illustrates an example of a memory portion that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0022] FIGs. 16 through 17 show block diagrams of a device that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0023] FIG. 18 illustrates a block diagram of a system including a memory controller that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

[0024] FIG. 19 illustrates a method that supports efficient utilization of die area for cross-point architecture in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

[0025] Some memory devices are built using a cross-point architecture having a "quilt" pattern. In some examples, the architecture may be a two-dimensional cross-point architecture. In some examples, the architecture may be a three-dimensional cross-point architecture. As is described with more detail below within quilt architectures, the memory device may be configured of modules called memory tiles. The memory device may be formed by arranging the memory tiles in an array. Each memory tile may include a similar configuration of components as the other memory tiles. Memory tiles may include a substrate layer that includes support components such as amplifiers and decoders and memory cells positioned above the substrate layer.

[0026] Because memory devices are configured to be assembled in an array of memory tiles, memory cells in a memory tile may be accessible using support components (*e.g.*, decoders) positioned in a neighboring memory tile. For instance, the cells of each tile within the quilt architecture may be accessed by decoders underlying adjacent tiles. So a given cell may be accessed from decoders that are outside of the footprint of the tile of which that cell is a party. Consequently, some memory cells positioned near the border of the array of memory tiles may not be accessible.

[0027] To ensure memory cells positioned above memory tiles are accessible, portions of the array near the border may have a different architecture. These portions may be referred to as boundary tiles and may be positioned adjacent to some memory tiles near the border of the array of memory tiles. For example, boundary tiles may be positioned on the first side of the array of memory tiles and positioned on a second side of the array of memory tiles opposite the first side. Boundary tiles may include support components for accessing memory cells of neighboring memory tiles. For example, boundary tiles may include decoders and amplifiers. In some examples, boundary tiles may not include memory cells positioned above the support components.

[0028] Techniques are described herein that support efficient utilization of die area for cross-point architecture, which may include reducing the size of the die area as compared to legacy configurations by reducing the area of boundary tiles and/or eliminating at least some

boundary tiles in a quilt architecture memory device. As used herein, a portion or cut of a substrate containing a memory array or circuit may be referred to as a die. Boundary tiles may be positioned on only one side of an array of memory tiles. Memory cells may be positioned above the boundary tiles. The boundary tiles may include support components to access both memory cells of neighboring memory tiles and memory cells of the boundary tiles. Column lines and column line decoders may be integrated as part of a boundary tile. Access lines, such as row lines may be truncated or omitted at or near borders of the memory portion of the memory device. By positioning boundary tiles on only one side of an array of memory tiles, area devoted to support components may be reduced. In addition, by positioning memory cells above the boundary tiles, the number of accessible memory cells in the memory device may be increased, in some cases.

[0029] Features of the disclosure introduced above are further described below in the context of a memory array. Specific examples are then described for memory devices and memory portions that relate to reducing the die area by removing boundaries in a quilt architecture. These and other features of the disclosure are further illustrated by and described with reference to apparatus diagrams, system diagrams, and flowcharts that relate to reducing the die area by removing boundaries in a quilt architecture.

[0030] **FIG. 1** illustrates an example of a memory device 100 that supports efficient utilization of die area for cross-point architecture. In the illustrative example of FIG. 1, the memory device 100 includes a two-dimensional memory array 102. Memory device 100 may also be referred to as an electronic memory apparatus. Memory device 100 includes memory cells 105 that are programmable to store different states. FIG. 1 is an illustrative schematic representation of various components and features of the memory device 100. As such, it should be appreciated that the components and feature of the memory device 100 are shown to illustrate functional interrelationships, not their actual physical positions within the memory device 100. FIG. 1 also shows an alternative schematic option of arranging sense component 126 (in a dashed box). An ordinary person skilled in the art would appreciate that sense component may be associated either with column decoder or row decoder without losing its functional purposes.

[0031] Each memory cell 105 may be programmable to store two states, denoted as a logic 0 and a logic 1. In some cases, memory cell 105 is configured to store more than two logic states. A memory cell 105 may include a capacitor or other memory storage component

to store a charge representative of the programmable states; for example, a charged and uncharged capacitor may represent two logic states, respectively, or a chalcogenide material may represent different states depending on its crystalline structure or other properties, for example.

[0032] The memory device 100 may be arranged using a quilt architecture. In a quilt architecture, tiles with similar configurations of components are arranged in an array. Memory devices built in such a manner may be expanded or contracted by adding or reducing tiles. The tiles may be building blocks for the memory device 100. Supporting circuitry (not shown) for the memory device may be positioned beneath the arrays of memory cells in a tile. As used herein a quilt architecture may refer to a memory array comprising a plurality of memory modules. For example, a memory device having a quilt architecture may comprise a repeating pattern of memory modules.

[0033] In some examples of quilt architecture, some memory cells positioned above a first tile may be accessed using support circuitry (not shown) positioned in a neighboring tile. Consequently, at the borders of the arrays of memory cells, some memory cells may not be accessible. To address these inaccessibility issues, boundary tiles may be positioned beyond the border of the array of memory cells to ensure all memory cells of the tiles are accessible. In some examples, memory cells may be positioned above the boundary tiles.

[0034] Operations such as reading and writing, which may be referred to as access operations, may be performed on memory cells 105 by activating or selecting the appropriate combination of common conductive lines, such as, for example, word line 110 and digit line 115. Word lines 110 may also be referred to as access lines or row lines and digit lines 115 may also be referred to as bit lines or column lines. In some examples, the sense component may be coupled to either the word lines or the row lines. Word lines 110 and bit lines 115 may be perpendicular (or nearly perpendicular) to one another to create an array. References to word lines and bit lines, or their analogues are interchangeable without loss of understanding or operation. Depending on the type of memory device (*e.g.*, FeRAM, RRAM, *etc.*) other access lines may be present (not shown), such as plate lines, for example. It should be appreciated that the exact operation of the memory device may be altered based on the type of memory device and/or the specific access lines used in the memory device.

[0035] Activating or selecting a word line 110 or a digit line 115 may include applying a voltage to the respective line. Word lines 110 and digit lines 115 are made of conductive

materials. For example, word lines 110 and digit lines 115 may be made of metals (such as copper, aluminum, gold, tungsten, *etc.*), metal alloys, other conductive materials, or the like. By activating one word line 110 and one digit line 115 (*e.g.*, applying a voltage to the word line 110 or digit line 115), a single memory cell 105 may be accessed at their intersection. Accessing the memory cell 105 may include reading or writing the memory cell 105.

[0036] In some architectures, the logic storing device of a cell, *e.g.*, a capacitor, may be electrically isolated from the digit line by a selection component. The word line 110 may be connected to and may control the selection component. For example, the selection component may be a transistor and the word line 110 may be connected to the gate of the transistor. Activating the word line 110 results in an electrical connection or closed circuit between the capacitor of a memory cell 105 and its corresponding digit line 115. The digit line may then be accessed to either read or write the memory cell 105.

[0037] Accessing memory cells 105 may be controlled through a row decoder 120 and a column decoder 130. Row decoder 120, sense component, 125, and column decoder 130 may be configured under memory cells 105. As discussed below, these components may occupy portions of a substrate region underlying the array. In some examples, a row decoder 120 receives a row address from the memory controller 140 and activates the appropriate word line 110 based on the received row address; the appropriate word line 110 may be the word line 110 associated with the deck that includes a target memory cell 105, as discussed below. Similarly, a column decoder 130 receives a column address from the memory controller 140 and activates the appropriate digit line 115. For example, memory device 100 may include multiple word lines 110, labeled WL_1 through WL_M for the illustrative array 102, and multiple digit lines 115, labeled DL_1 through DL_N, where M and N depend on the array size. Thus, by activating a word line 110 and a digit line 115, *e.g.*, WL_2 and DL_2, the memory cell 105 at their intersection may be accessed.

[0038] Upon accessing, a memory cell 105, may be read, or sensed, by sense component 125 to determine the stored logic state of the memory cell 105. For example, after accessing the memory cell 105, the memory component of memory cell 105 may discharge onto its corresponding digit line 115. The discharging may cause a change in the voltage of the digit line 115, which sense component 125 may compare to a reference voltage (not shown) in order to determine the stored state of the memory cell 105. For example, if digit line 115 has

a higher voltage than the reference voltage, then sense component 125 may determine that the stored state in memory cell 105 was a logic 1 and vice versa.

[0039] Sense component 125 may include various transistors or amplifiers in order to detect and amplify a difference in the signals, which may be referred to as latching. The detected logic state of memory cell 105 may then be output through column decoder 130 as input/output 135. Sense component 125 may operate at a lower voltage than other components of memory device 100. For example, sense component 125 may be or include a low voltage latch.

[0040] A memory cell 105 may be set, or written, by activating the relevant word line 110 and digit line 115. As discussed above, activating a word line 110 electrically connects the corresponding row of memory cells 105 to their respective digit lines 115. By controlling the relevant digit line 115 while the word line 110 is activated, a memory cell 105 may be written—*i.e.*, a logic value may be stored in the memory cell 105. Column decoder 130 may accept data, for example input/output 135, to be written to the memory cells 105. A ferroelectric memory cell 105 may be written by applying a voltage across the ferroelectric capacitor. This process is discussed in more detail below.

[0041] The memory controller 140 may control the operation (*e.g.*, read, write, re-write, refresh, *etc.*) of memory cells 105 through the various components, such as row decoder 120, column decoder 130, and sense component 125. Memory controller 140 may generate row and column address signals in order to activate the desired word line 110 and digit line 115. Memory controller 140 may also generate and control various voltage potentials used during the operation of memory device 100. In general, the amplitude, shape, or duration of an applied voltage discussed herein may be adjusted or varied and may be different for the various operations for operating the memory device 100. Furthermore, one, multiple, or all memory cells 105 within memory device 100 may be accessed simultaneously; for example, multiple or all cells of memory device 100 may be accessed simultaneously during a reset operation in which all memory cells 105, or a group of memory cells 105, are set to a single logic state. It should be appreciated that the exact operation of the memory device may be altered based on the type of memory device and/or the specific access lines used in the memory device.

[0042] **FIG. 2** illustrates an example memory device 200 that supports efficient utilization of die area for cross-point architecture. In the illustrative example of FIG. 2, the

memory device 200 includes a three-dimensional memory array 205. Memory device 200 may also be referred to as an electronic memory apparatus. The memory device 200 may be an example of the memory device 100 described with reference to FIG. 1. As such, descriptions of components with similar naming and numbering may not be fully described with reference to FIG. 2. The sense component 125-a may be an example of the sense component 125 described with reference to FIG. 1. The input/output 135-a may be an example of the input/output 135 described with reference to FIG. 1. The memory controller 140-a may be an example of the memory controller 140 described with reference to FIG. 1. FIG. 1 is an illustrative schematic representation of various components and features of the memory device 100. As such, it should be appreciated that the components and feature of the memory device 100 are shown to illustrate functional interrelationships, not their actual physical positions within the memory device 100. Also, FIG. 2 shows an alternative schematic option of arranging sense component 126-a (in a dashed box). An ordinary person skilled in the art would appreciate that sense component may be associated either with column decoder or row decoder without losing its functional purposes.

[0043] Memory device 200 may include a three-dimensional (3D) memory array 205, where two or more two-dimensional (2D) memory arrays (e.g., memory array 102) are formed on top of one another. In such a configuration, a 2D memory array may be referred to as a deck of memory cells. This may increase the number of memory cells that may formed on a single die or substrate as compared with 2D arrays, which in turn may reduce production costs or increase the performance of the memory device 200, or both. According to the example depicted in FIG. 2, memory device 200 includes two levels (or decks) of memory cells 105-a and may thus be considered a three-dimensional memory array; however, the number of levels is not limited to two. Each level may be aligned or positioned so that memory cells 105-a may be approximately aligned with one another across each level, forming a memory cell stack 210. In other embodiments (not shown), the memory device 200 may be a single level memory, *e.g.*, a two-dimensional memory array.

[0044] As shown in FIG. 2, the two memory cells 105-a in a memory cell stack 210 may share a common conductive line such as a digit line 115-a. That is, a digit line 115-a may be in electronic communication with the bottom electrode of the upper memory cell 105-a and the top electrode of the lower memory cell 105-a. The upper memory cells 105-a may be referred to as a top deck and the lower memory cells 105-a may be referred to as a bottom deck. Other configurations may be possible; for example, a third deck may share a word line 110-a with a lower deck. In general, one memory cell 105-a may be located at the intersection of two conductive lines, such as a word line 110-a and a digit line 115-a. This intersection may be referred to as a memory cell's address. A target memory cell 105-a may be a memory

cell 105-a located at the intersection of an energized word line 110-a and digit line 115-a; that is, a word line 110-a and digit line 115-a may be energized in order to read or write a memory cell 105-a at their intersection. Other memory cells 105 that are in electronic communication with (*e.g.*, connected to) the same word line 110-a or digit line 115-a may be referred to as untargeted memory cells. Also, depending on the memory cell (*e.g.*, FeRAM, RRAM, *etc.*), other access lines, *e.g.*, plate lines (not shown) may be involved in accessing the storage element of a cell.

[0045] Accessing memory cells 105-a may be controlled through a row decoder 120-a and a column decoder 130-a. For example, memory device 200 may include multiple word lines 110-a, labeled WL_T1 through WL_TM for the top deck of the illustrative array 205 and WL_B1 through WL_BM for the bottom deck of the illustrative array 205, and multiple digit lines 115-a, labeled DL_1 through DL_N, where M and N depend on the array size. Thus, by activating a word line 110-a and a digit line 115-a, *e.g.*, WL_T2 and DL_2, the memory cell 105-a of the top deck at their intersection may be accessed. By activating, for example, WL_B2 and DL_2, the memory cell 105-a of the bottom deck at their intersection may be accessed. In some examples, other access lines or polarization lines (not shown) may be present. As such, the operations of the memory device may be modified based on the type of memory device and/or the specific access/polarization lines used in the memory device.

[0046] **FIG. 3** illustrates an example of memory array 300 that supports efficient utilization of die area for cross-point architecture. Memory array 300 may be an example of memory arrays 102 and 205 described with reference to FIGs. 1 and 2. As depicted in FIG. 3, memory array 300 includes multiple materials to construct memory cells 105-b. Each memory cell 105-b is stacked in a vertical direction (*e.g.*, perpendicular to a substrate) to create memory cell stacks. Memory cells 105-b may be examples of a memory cell 105 as described with reference to FIG. 1. Memory array 300 may thus be referred to as a three-dimensional or 3D memory array.

[0047] Memory array 300 also includes word lines 110-b and bit lines 115-b, which may be examples of word line 110 and bit line 115, as described with reference to FIG. 1. Illustration of the materials 105-b between the word lines 110-b and the bit lines 115-b may represent memory cell 105-a on the lower deck in FIG. 2. Memory array 300 includes electrode 305 elements, logic storage component 310, substrate 315, and selection component 320. In some examples, a single component may act as both a logic storage component and a

selection component. Electrode 305-a may be in electronic communication with bit line 115-b and electrode 305-c may be in electronic communication with word line 110-b. Insulating materials depicted as empty spaces may be both electrically and thermally insulating. As described above, in PCM technology, various logic states may be stored by programming the electrical resistance of the logic storage component 310 in memory cells 105-b. In some cases, this includes passing a current through memory cell 105-b, heating the logic storage component 310 in memory cell 105-b, or melting the material of the logic storage component 310 in memory cells 105-b wholly or partially. Other storage mechanism, such as threshold voltage modulation, may be exploited in chalcogenide-based memories. The memory array 300 may be included as part of a quilt architecture such that the memory cells are positioned above a substrate layer that includes the support components.

[0048] Memory array 300 may include an array of memory cell stacks, and each memory cell stack may include multiple memory cells 105-b. Memory array 300 may be made by forming a stack of conductive materials, such as word lines 110-b, where each conductive material is separated from an adjacent conductive material by electrically insulating materials in between. The electrically insulating materials may include oxide or nitride materials, such as silicon oxide, silicon nitride, or other electrically insulating materials. These materials may be formed above a substrate 315, such as a silicon wafer, or any other semiconductor or oxide substrate. Subsequently, various process steps may be utilized to form materials in between the word lines 110-b and bit lines 115-b such that each memory cell 105-b may be coupled to a word line and a bit line.

[0049] The selection component 320 may be connected with the logic storage component 310 through electrode 305-b. In some examples, the positioning of the selection component 320 and the logic storage component 310 may be flipped. The stack comprising the selection component 320, the electrode 305-b, and the logic storage component 310 may be connected to a word line 110-b through the electrode 305-c and to a bit line 115-b through the electrode 305-a. The selection component may aid in selecting a particular memory cell 105-b or may help prevent stray currents from flowing through non-selected memory cells 105-b adjacent a selected memory cell 105-b. The selection component may include an electrically non-linear component (*e.g.*, a non-ohmic component) such as a metal-insulator-metal (MIM) junction, an ovonic threshold switch (OTS), or a metal-semiconductor-metal (MSM) switch, among other types of two-terminal select device such as a diode. In some cases, the selection

component includes a chalcogenide film. The selection component may, in some examples, include an alloy of selenium (Se), arsenic (As), and germanium (Ge).

[0050] Various techniques may be used to form materials or components on a substrate 315. These may include, for example, chemical vapor deposition (CVD), metal-organic vapor deposition (MOCVD), physical vapor deposition (PVD), sputter deposition, atomic layer deposition (ALD), or molecular beam epitaxy (MBE), among other thin film growth techniques. Material may be removed using a number of techniques, which may include, for example, chemical etching (also referred to as "wet etching"), plasma etching (also referred to as "dry etching"), or chemical-mechanical planarization.

[0051] As discussed above, memory cells 105-b of FIG. 3 may include a material with a variable resistance. Variable resistance materials may refer to various material systems, including, for example, metal oxides, chalcogenides, and the like. Chalcogenide materials are materials or alloys that include at least one of the elements sulfur (S), tellurium (Te), or Se. Many chalcogenide alloys may be possible—for example, a germanium-antimony (Sb)-tellurium alloy (Ge-Sb-Te) is a chalcogenide material. Other chalcogenide alloys not expressly recited here may also be employed.

[0052] Phase change memory exploits the large resistance contrast between crystalline and amorphous states in phase change materials, which may be chalcogenide materials. A material in a crystalline state may have atoms arranged in a periodic structure, which may result in a relatively low electrical resistance. By contrast, material in an amorphous state with no or relatively little periodic atomic structure may have a relatively high electrical resistance. The difference in resistance values between amorphous and crystalline states of a material may be significant; for example, a material in an amorphous state may have a resistance one or more orders of magnitude greater than the resistance of the material in its crystalline state. In some cases, the material may be partially amorphous and partially crystalline, and the resistance may be of some value between the resistances of the material in a wholly crystalline or wholly amorphous state. So a material may be used for other than binary logic applications—i.e., the number of possible states stored in a material may be more than two.

[0053] To set a low-resistance state, a memory cell 105-b may be heated by passing a current through the memory cell. Heating caused by electrical current flowing through a material that has a finite resistance may be referred to as Joule or Ohmic heating. Joule

heating may thus be related to the electrical resistance of the electrodes or the phase change material. Heating the phase change material to an elevated temperature (but below its melting temperature) may result in the phase change material crystallizing and forming the low-resistance state. In some cases, a memory cell 105-b may be heated by means other than Joule heating, for example, by using a laser. To set a high-resistance state, the phase change material may be heated above its melting temperature, for example, by Joule heating. The amorphous structure of the molten material may be quenched, or locked in, by abruptly removing the applied current to quickly cool the phase change material. The various components, including memory cells 105-b, access lines (*e.g.*, word lines 110-b and bit lines 115-b) may be configured over substrate 315 to efficiently use the area of a die that includes the components. As described below, each portion of the array may overlie decoders and/or other circuitry.

[0054] **FIG. 4** illustrates an example of a memory device 400 that supports efficient utilization of die area for cross-point architecture. As discussed above, the term quilt architecture may refer to a memory device formed of a plurality of memory tiles or memory modules having a common configuration of components. The memory tiles may be arranged in a repeating pattern. The memory device 400 may be an example of the memory device 100 described with reference to FIG. 1.

[0055] The memory device 400 may include a memory portion 410 and a control circuit portion 415. The memory portion 410 of the memory device 400 may include an array of memory cells and supporting circuitry for the array of memory cells, for example, decoders and sense amplifiers. In some instances, the memory portion 410 may refer to an area of the memory device 400 that includes decoders. The control circuit portion 415 may include other components related to the memory device 400. For example, the memory portion 410 may include a memory controller 140 or an input/output 135 system. In some instances, the control circuit portion 415 may refer to an area of the memory device 400 that does not include some types of decoders or is exclusive of decoders. For example, the control circuit portion 415 may be exclusive of row decoders, column decoders, sense amplifiers, or combinations thereof. In some examples, the control circuit portion 415 may include other types of decoders, for example, plate line decoders.

[0056] The memory portion 410 may include a core portion 420 and a boundary portion 425. The memory portion 410 may include a substrate layer and memory cells positioned

above the substrate layer. The core portion 420 may refer to an array of the memory device 400 formed using a plurality of memory tiles 430. In some examples, the core portion 420 may correspond to an area of the memory device 400 that includes an array of memory cells (*e.g.*, array of memory cells 510).

[0057] The memory tiles 430 may be memory modules having common components. Each memory tile 430 in the core portion 420 may have an identical configuration of components. In this manner, the memory tiles 430 may be used as building blocks to assembly the memory device 400. The size of a core portion 420 (and by extension the memory portion 410 and the memory device 400 as a whole) may be flexible using memory tiles 430. A core portion 420 may be enlarged during design or manufacturing by adding additional memory tiles 430. A size of the core portion 420 may be reduced during design or manufacturing by removing memory tiles 430.

[0058] The memory tiles 430 may be configured to couple to neighboring memory tiles to form the core portion 420. In some examples, circuitry (*e.g.*, decoders and amplifiers) positioned in neighboring memory tiles 430 may be configured to access memory cells positioned above the memory tile 430. For example, circuitry in memory tile 430-2 may be used to access memory cells positioned above memory tile 430-1. In this manner, a memory tile 430 may not be configured to be fully operational as a stand-alone unit. Rather, a memory tile 430 may rely on the circuitry of neighboring tiles to provide full functionality to the memory tile 430. For example, circuitry in neighboring tiles may be used to access memory cells positioned above the memory tile.

[0059] At the borders of the core portion 420, a memory tile 430 may not have a neighboring tile to provide additional circuitry for access memory cells. To ensure functionality of all memory cells associated with a memory tile 430 on the edge of the core portion 420, a boundary portion 425 may be disposed around the core portion 420. The boundary portion 425 may include a plurality of first boundary tiles 435 and a plurality of second boundary tiles 440. The first boundary tiles 435 may be positioned at core portion 420 edges crossed by row access lines or word lines. The second boundary tiles 440 may be positioned at core portion 420 edges crossed by column access lines or digit lines.

[0060] The various tiles in the memory device 400 may have certain relative dimensions. A memory tile 430 may have a first dimension 445 extending in a first direction and a second dimension 450 extending in a second direction orthogonal to the first direction. In some

examples, the first dimension 445 may be equal to the second dimension 450. In some examples, the first dimension 445 may be different from the second dimension 450. In some examples, the first dimension 445 may be equal to eight units and the second dimension 450 may be equal to eight units. A unit may be associated with the size of the decoders in the memory tile.

[0061] The first boundary tile 435 may have a first dimension 455 extending in the first direction and a second dimension 460 extending in the second direction. The second dimension 460 may be equal to the second dimension 450. The first dimension 455 may be different than the first dimension 445. In some examples, the first dimension 455 of the first boundary tile 435 is three-eighths the size of the first dimension 445 of the memory tile 430. In other examples, the first dimension 455 may be any relative size compared to the first dimension 445. The dimensions 455, 460 of the first boundary tile 435 may be determined based at least in part on the circuitry (*e.g.*, decoders and amplifiers) used to access memory cells positioned above neighboring memory tiles 430. In some examples, the first dimension 455 may be equal to the second dimension 460. In some examples, the first dimension 455 may be different from the second dimension 460.

[0062] The second boundary tile 440 may have a first dimension 465 extending in the first direction and a second dimension 470 extending in the second direction. The first dimension 465 may be equal to the first dimension 445. The second dimension 470 may be different than the second dimension 450 and the second dimension 460. In some examples, the second dimension 470 of the second boundary tile 440 is one-eighths the size of the second dimension 450 of the memory tile 430. In other examples, the second dimension 470 may be any relative size compared to the second dimension 450. The dimensions 465, 470 of the second boundary tile 440 may be determined based at least in part on the circuitry (*e.g.*, decoders and amplifiers) used to access memory cells positioned above neighboring memory tiles 430. For example, the second boundary tile 440 may include column decoders coupled to column lines to assist in accessing memory cells positioned above neighboring memory tiles 430. In some examples, the first dimension 465 may be equal to the second dimension 470. In some examples, the first dimension 465 may be different from the second dimension 470.

[0063] **FIG. 5** illustrates an example of a cross-section view 500 of the memory device 400 of FIG. 4 along the line 5-5. The cross-section view 500 shows the various layers and

decks that may be included in the memory device 400. The memory device 400 may include a substrate layer 505 and decks 515 of memory cells positioned above the substrate layer 505. In some examples, the substrate layer 505 may be referred to as a peripheral region.

[0064] The substrate layer 505 may include the portion of the memory device 400 that includes support circuitry such as decoders and amplifiers. The substrate layer 505 may include portions of the control circuit portion 415, portions of the core portion 420 (*e.g.*, the support circuitry but not the memory cells), and portion of the boundary portion 425. In some examples, the substrate layer 505 is positioned below the array of memory cells 510. The substrate layer of the memory portion 410 may be referred to as complementary metal-oxide-semiconductor (CMOS) under array (CuA). The core portion 420 and the boundary portion 425 may be referred to as CuA.

[0065] The array of memory cells 510 may be an example of the memory cells 105 described with reference to FIG. 1. The array of memory cells 510 may include a plurality of decks 515 of memory cells. The decks 515 of memory cells may each be a two-dimensional array of memory cells. The decks 515 of memory cells may be an example of the decks of memory cells described with reference to FIG. 1. The array of memory cells 510 may be positioned over the core portion 420 of the substrate layer 505. In the illustrative example, the array of memory cells is not positioned over the boundary portion 425 or the control circuit portion 415 of the substrate layer 505 such that the decks 515 do not overlap the portions 415, 425. The memory device 400 may include any number of decks 515 of memory cells. In some examples all of the memory cells positioned above the core portion 420 are accessible using support components positioned in the core portion 420 and the boundary portion 425.

[0066] **FIG. 6** illustrates an example of memory tile configurations 600 that supports efficient utilization of die area for cross-point architecture. FIG. 6 illustrates only a portion of a tile under a memory array for clarity purposes. The memory tile configurations 600 may include a first configuration 605 and a second configuration 610. The first configuration 605 and the second configuration 610 may be examples of memory tiles 430 described with reference to FIGs. 4 and 5. A core portion 420 of a memory device 400 may be formed as a repeating pattern of one of the configurations 605, 610.

[0067] The first configuration 605 and the second configuration 610 include similar components but different arrangements of components. Each configuration 605, 610 includes column line decoders 615, row line decoders 620 for a first deck 515-1 of memory cells, row

line decoders 625 for a second deck 515-2 of memory cells, sense amplifiers 630 for the first deck 515-1, and sense amplifiers 635 for the second deck 515-2. In some examples, the configuration 605, 610 may include components for any number of memory decks of memory cells. The memory tiles 430 may include additional circuitry and components not expressly described with regards to the configurations 605, 610.

[0068] The column line decoder 615 may be coupled to column line (see column lines 1405 in FIG. 14). The column line decoder 615 may be configured to access memory cells in multiple decks 515. A single column line may be configured to access multiple decks 515 of memory cells. The column line decoder 615 may be positioned in a variety of locations in the memory tile 430. The column line decoder 615 may be a number of shapes and sizes. The locations and sizes shown in configurations 605, 610 are for illustrative purposes only and are not limiting. The column line decoder 615 may be an example of the row decoder 120 described with reference to FIG. 1.

[0069] The row line decoder 620 may be coupled to a row line (see row lines 705 in FIG. 7). The row line decoder 620 may be configured to access memory cells in a single deck 515 (*e.g.*, access memory cells in deck 515-1). A single row line may be associated with a single deck 515 of memory cells. The row line decoder 620 may be positioned in a variety of locations in the memory tile 430. The row line decoder 620 may be a number of shapes and sizes. The locations and sizes shown in configurations 605, 610 are for illustrative purposes only and are not limiting. The row line decoder 620 may be an example of the row decoder 120 described with reference to FIG. 1.

[0070] The row line decoder 625 may be coupled to a row line (see row lines 710 in FIG. 7). The row line decoder 625 may be configured to access memory cells in a single deck 515 (*e.g.*, access memory cells in deck 515-2). A single row line may be associated with a single deck 515 of memory cells. The row line decoder 625 may be positioned in a variety of locations in the memory tile 430. The row line decoder 625 may be a number of shapes and sizes. The locations and sizes shown in configurations 605, 610 are for illustrative purposes only and are not limiting. The row line decoder 625 may be an example of the row decoder 120 described with reference to FIG. 1. The row line decoder 625 may be an example of the row line decoder 620 described above.

[0071] The sense amplifier 630 may be coupled to a row line (see row lines 705 of FIG. 7). The sense amplifier 630 may be configured to amplify a signal on a row line during an

access operation. The sense amplifier 630 may be associated with a single deck 515 of memory cells (*e.g.*, deck 515-1). The sense amplifier 630 may be positioned in a variety of locations in the memory tile 430. The sense amplifier 630 may be a number of shapes and sizes. The locations and sizes shown in configurations 605, 610 are for illustrative purposes only and are not limiting. The sense amplifier 630 may be an example of at least a component of the sense component 125 described with reference to FIG. 1.

[0072] The sense amplifier 635 may be coupled to a row line (see row lines 710 of FIG. 7). The sense amplifier 635 may be configured to amplify a signal on a row line during an access operation. The sense amplifier 635 may be associated with a single deck 515 of memory cells (*e.g.*, deck 515-2). The sense amplifier 635 may be positioned in a variety of locations in the memory tile 430. The sense amplifier 635 may be a number of shapes and sizes. The locations and sizes shown in configurations 605, 610 are for illustrative purposes only and are not limiting. The sense amplifier 635 may be an example of at least a component of the sense component 125 described with reference to FIG. 1. The sense amplifier 635 may be an example of the sense amplifier 630 described above. In some examples, sense amplifiers 630 and 635 may be coupled to column lines rather than to row lines. In some examples, sense amplifiers 630, 635 may be coupled to bit lines. In some examples, the sense amplifiers 630, 635 may be coupled to word lines.

[0073] The configuration 605 of a memory tile 430 may be arranged such that if memory tiles 430 having the configuration 605 are placed in a repeating pattern an array of memory cells and support circuitry may be formed. The support circuitry (*e.g.*, decoders and amplifiers) may be arranged such that when memory tiles 430 are positioned next to each other a continuous pattern of components are formed. For example, if a memory tile 430-2 having the configuration 605 is placed next to a memory tile 430-1 having a configuration 605 a repeating pattern of decoders 620, decoders 615, decoders 625, decoders 615, *etc.* may be formed in a first direction. A similar pattern of decoders may be formed by configuration 605 in a second direction orthogonal to the first direction.

[0074] The configuration 610 of a memory tile 430 may be arranged such that if memory tiles 430 having the configuration 610 are placed in a repeating pattern an array of memory cells and support circuitry may be formed. Similar to configuration 605, if a memory tile 430-2 having the configuration 610 is placed next to a memory tile 430-1 having a configuration 610 a repeating pattern of decoders 620, decoders 615, decoders 625, *etc.* may

be formed in a first direction. However, a different pattern of decoders may be formed by the configuration 610 in a second direction orthogonal to the first direction.

[0075] In some instances, the core portion 420 may include multiple configurations 600 of memory tiles 430. A set of distinct configurations may be configured to cooperate with one another. For example, a core portion 420 may include two distinct configurations of memory tiles 430 arranged in an alternating pattern. In other examples, patterns that use three or more configurations may be formed using memory tiles 430.

[0076] **FIG. 7** illustrates an example of a memory tile 700 having access lines that support efficient utilization of die area for cross-point architecture. FIG. 7 depicts both a top-down view 702 and a cross-section view 704 of the memory tile 700. The top-down view 702 illustrates only components in the substrate layer and row lines for clarity. For example, portions of the memory tile may be omitted for clarity. The row lines are shown offset in a two-dimensional arrangement in 702 for clarity purposes only. The cross-section view illustrates only components in the substrate layer and row lines for clarity in addition to a few two-deck memory cells and bit lines associated with them. In another example, row lines associated with different decks may be positioned at different heights in the memory device as depicted in the cross-section view 704. As such, in some examples, row lines may overlap or may stacked on top of another as depicted in the cross-section view 704. In some examples, the memory tile 700 may be an example of the memory tile 430 described with reference to FIGs. 4-6. The memory tile 700 may be arranged in a manner similar to the configuration 605 described with reference to FIG. 6. The memory tile 700 may include row lines 705-a row line, 705-b, 705-c and a row line 710-a, 710-b overlaid the circuitry (e.g., decoders and amplifiers). The row lines 705-a, 705-b, 705-c, 710-a, 710-b may be examples of digit lines 115 described with reference to FIGs. 1 and 2. In some instances, row lines 705-a, 705-b, 705-c, 710-a, 710-b may be examples of word lines 110 described with reference to FIG. 1. References to word lines and bit lines, or their analogues are interchangeable without loss of understanding or operation.

[0077] The row lines 705-a, 705-b, 705-c, 710-a, 710-b may be coupled to memory cells 510 in the memory array. A particular row line may be dedicated to a particular deck 515 of memory cells. For example, row lines 705-a, 705-b, 705-c may be associated with a first deck 515-1 and row lines 710-a, 710-b may be associated with a second deck 515-2. The row lines 705-a, 705-b, 705-c, 710-a, 710-b may each have a common length. In some examples, row lines associated with a higher deck of memory cells may be longer than the common length. For example, a row line 710-a may extend a fixed

distance between two unassociated row decoders. Row line 710-a is associated with the second deck 515-2 of memory cells. Row line 710-a may also be associated with row line decoders 625-a and 625-b such that memory cells of the second deck 515-2 are operatively coupled to the decoders 625-a, 625-b via the row line 710-a. Row line 710-a extends from a row line decoder 620-a adjacent to the row line decoder 625-a in a first direction to a row line decoder 620-b adjacent to the row line decoder 625-b in the first direction. It should be appreciated that the row line decoders 620-a, 620-b are associated with a different deck of memory cells than the row line 710-a. Row line decoder 625-a or row line decoder 625-b or both are associated with the row line 710-a. In some instances, the row line 710-a terminates at or near a division between two adjacent row decoders associated with a different deck (e.g., row decoders 620-a and 620-b). This may occur because circuitry associated with the row decoders may prevent the row line 710-a from extending further.

[0078] In some instances, row line 705-a or row line 705-b may also terminate at a or near a division between two adjacent row decoders associated with a different deck (e.g., row decoders 625-a and 625-b). For example, area 720 between row line decoders 625-a and 625-b may prevent row lines 705-a and 705-b from extending further. In some examples, the row lines and column lines associated with an upper deck of memory cells may be longer than the row lines and column lines associated with a lower deck of memory cells. In some examples, the area 720 between row line decoders may be used for connections of row lines of higher decks. In some examples, the area 720 may be impassable to some row lines (*e.g.*, row lines 705-a, 705-b, 705-c) because a wall of vias coupled to row lines of other decks (*e.g.*, row lines 710-a, 710-b) are occupying this space. So in some examples, an access line or a subset of access lines positioned in the boundary portion may each terminate at the control circuit portion or may span to a maximum length otherwise used or designated for the array.

[0079] Row lines 705-a, 705-b, 705-c, 710-a, 710-b may span boundaries between memory tiles 700. For example, end 715 may show that row line 705-c extends beyond the specific memory tile 700 represented in FIG. 7. In some examples, the row lines 705-a, 705-b, 705-c, 710-a, 710-b may be formed by overlaying the row lines over the substrate layer 505. In some examples, there may be additional types of row lines based at least in part on the number of distinct decks 515 of memory cells that are part of the memory device 400. The row lines 705-a, 705-b, 705-c, 710-a, 710-b may be positioned in a variety of locations in the memory tile 700. The row lines 705-a, 705-b, 705-c, 710-a, 710-b may be any number of shapes and sizes. The locations and sizes shown in FIG. 7 are for illustrative purposes only and are not limiting. In some instances, a subset of row lines may have a length

that is less than the common length. For example, some row lines may be terminated early because the row lines reach an edge of the memory portion 410 of the memory device 400. In some examples, row lines 705-a, 705-b, 705-c, 710-a, 710-b may be positioned over boundary tiles 435.

[0080] The cross-section view 704 illustrates that row lines 705-a, 705-b, 705-c may be positioned at a different distance from the substrate layer 505 than row lines 710-a, 710-b. In some examples, row lines 710-a, 710-b are positioned over row lines 705-a, 705-b, 705-c. In some examples, the row lines 710-a, 710-b are positioned directly over top of row lines 705-a, 705-b, 705-c. In some examples, the row lines 710-a, 710-b may be offset from the row lines 705-a, 705-b, 705-c. Contacts 740, 745 may extend from the substrate layer 505 to their respective decks of memory cells. For example, contact 740 may couple row line decoders for the second deck (e.g., row line decoders 625-a/b) to a row line for the second deck (e.g., row lines 710-a, 710-b). In other examples, contact 745 may couple row line decoder for the first deck (e.g., row line decoders 620-b) to a row line for the first deck (e.g., row line 705-a). In some examples, the contacts 740, 745 may be vias. In some cases, the contacts 740 may configured as stacked contacts. In some examples, a plurality of the contacts 740 may form a wall that does not permit the row lines 705-a, 705-b or 705-c to extend through. In some examples, the contacts 740, 745 may not be considered part of their respective decoders. Regardless of the designation of the contacts 740, 745, it should be appreciated that memory cells may be positioned over or above the decoders 620-a/b, 625-a/b and other support circuit component 750 (e.g., column decoders or sense amplifiers).

[0081] In some examples, plate lines (now shown) or other access lines may be integrated into the memory tiles 700. For example, a plate line may be configured to bias a memory cell during an access operation. Other decoders may be incorporated into the memory device to utilize the other access lines or plate lines. Plate lines or other access lines may be in electronic communication with a memory controller of the memory device. In some examples, plate lines may be coupled to a plate associated with a capacitor of a memory cell in the memory device.

[0082] **FIG. 8** illustrates an example of boundary tile configurations 800 that supports efficient utilization of die area for cross-point architecture. FIG. 8 illustrates only components in the substrate layer for clarity. The boundary tile configurations 800 may include a first configuration 805 and a second configuration 810. The first configuration 805 may be configured and arranged to be positioned on a first side of the core portion 420 (*e.g.*, the left side of the core portion 420 shown in FIG. 4). For example, the boundary tiles 435-1 and

435-3 may be arranged using the first configuration 805. The second configuration 810 may be configured and arranged to be positioned on a second side of the core portion 420 opposite the first side (*e.g.*, the right side of the core portion 420 shown in FIG. 4). For example, the boundary tiles 435-2 and 435-4 may be arranged using the second configuration 810. The first configuration 805 and the second configuration 810 may be examples of boundary tiles 435 described with reference to FIGs. 4 and 5. A boundary portion 425 of a memory device 400 may be formed as a repeating pattern of the configuration 805, 810.

[0083] The configurations 805, 810 may correspond to a core portion 420 formed of memory tiles 430 arranged using configuration 605. In other examples, components of the configurations 805, 810 may be rearranged to correspond to configuration 610 or any other configurations of memory tiles 430.

[0084] The configurations 805, 810 include row line decoders 620, row line decoders 625, sense amplifiers 630, and sense amplifiers 635. In the illustrative example, configurations 805, 810 do not include column line decoders 615. Because memory cells are not positioned above the boundary tiles 435, column lines are also not positioned above the boundary tiles 435, and, therefore, column line decoders may not be included in the configurations 805, 810 of boundary tiles 435.

[0085] The boundary tile configurations 800 may include a number of decoders that is less than a number of decoders in a memory tile 430 of the core portion 420. For example, because memory cells are not positioned above the substrate layer of a boundary tiles 435, the boundary tile configurations 800 do not include column decoders. In other examples, the boundary tile configurations 800 include fewer row decoders 620, 625 and fewer sense amplifiers 630, 635 than are present in a memory tile 430 of the core portion 420. In some examples, the number of decoders in a single boundary tile configuration 800 (*e.g.*, first configuration 805 or second configuration 810) may be less than half of the number of decoders in a memory tile 430 of the core portion 420.

[0086] **FIG. 9** illustrates an example of a memory device 900 that supports efficient utilization of die area for cross-point architecture. The memory device 900 may include a memory portion 905 and a control circuit portion 415. The memory portion 905 may include a core portion 420 and a boundary portion 910. The memory portion 905 of the memory device 900 includes a boundary portion 910 positioned on only one side of the core portion 420. In this manner, the area of the memory portion 905 may be less than the area of the

memory portion 410 of the memory device 400. The memory device 900 may be an example of the memory devices 100 or 400 described with reference to FIGs. 1 and 4-8. The memory portion 905 may be an example of the memory portion 410 described with reference to FIGs. 4-8. The boundary portion 910 may be an example of the boundary portion 425 described with reference to FIGs. 4-8.

[0087] The area of the memory portion 905 may be less than the area of memory portion 410 of the memory device 400. The boundary portion 910 may have different dimensions from the boundary portion 425 of the memory device 400. The area of the boundary portion 910 may be less than the combined total area of the boundary portions 425 of the memory device 400. In some examples, the right boundary portion of the memory device 900 may have an area larger than the right boundary portion of the memory device 400. However, the total area of the boundary portion 910 may be less than the total area of the boundary portion 425, which may include at least a left boundary portion and a right boundary portion.

[0088] Difference in the areas of the core portion 420 and the boundary portion 910 may be appreciated based on the dimensions of the respective portions. The core portion 420 may include a number of memory tiles 430. The memory tiles 430 may define a first dimension 445 and a second dimension 450.

[0089] The boundary portion 910 may include a number of boundary tiles 915. Boundary tiles 915 may be an example of the boundary tiles 435 described with reference to FIGs. 4, 5, and 8. A boundary tile 915 may include a first dimension 920 extending a first direction and a second dimension 460 extending in a second direction orthogonal to the first direction. The first dimension 920 may be different than the first dimension 445. In some examples, the first dimension 920 of the first boundary tile 915-1 is one-half the size of the first dimension 445 of the memory tile 430. In other examples, the first dimension 920 may be any relative size compared to the first dimension 445. The dimensions 920, 460 of the first boundary tile 915-1 may be determined based at least in part on the circuitry (*e.g.*, decoders and amplifiers) used to access memory cells positioned above neighboring memory tiles 430 and above the boundary tile 915. In some examples, the first dimension 920 may be equal to the second dimension 460. In some examples, the first dimension 920 may be different from the second dimension 460.

[0090] In some examples, the first dimension 920 may be larger than the first dimension 455 of the boundary tile 435 because the boundary tile 915 includes additional components to

access memory cells positioned above the boundary tile 915. In some instances, the first dimension 920 may be larger because of additional column line decoders 615 in the boundary tile 915.

[0091] The memory portion 905 may define a number of borders. For example, the core portion 420 may include borders 930, 935, 940, 945. As used herein, a border may refer to a line separating two areas of the memory device 900. For example, the term border may refer to a line where a particular portion of the memory device 900 terminates. The first border 930, the second border 935, and the third border 940 may define an intersection of the core portion 420 with the control circuit portion 415. In some examples, the borders 930, 935, 940 may be defined as the line where an array of memory cells terminates or an array of support circuitry terminates. The fourth border 945 may define an intersection of the core portion 420 with the boundary portion 910. The fourth border 945 may be positioned opposite the first border 930.

[0092] The boundary portion 910 may include borders 950, 955, 960, 965. The first border 950, the second border 955, and the third border 960 may define an intersection of the boundary portion 910 with the control circuit portion 415. In some examples, the borders 950, 955, 960 may be defined as the line where an array of memory cells terminates or an array of support circuitry terminates. The fourth border 965 may cooperate with the fourth border 945 to define an intersection of the core portion 420 and the boundary portion 910. The fourth border 965 may be positioned opposite the first border 950. In some examples, boundaries may be defined between memory tiles 430 and/or boundary tiles 910.

[0093] In some examples, the borders 930, 935, 940, 945, 950, 955, 960, 965 may be aligned with an edge of a decoder. In some examples, the borders 930, 935, 940, 945, 950, 955, 960, 965 may extend beyond the edge of a decoder. The intersection of the core portion 420 and the boundary portion 910 or the outer boundaries (*e.g.*, as represented by border 930, 935, 940, 950) may be less precise in practice than what is depicted in FIG. 9. In some examples, the outer boundaries may be aligned with edges of the array of memory cells.

[0094] **FIG. 10** illustrates an example of a cross-section view 1000 of the memory device 900 of FIG. 9 along the line 10-10. The cross-section view 1000 shows the various layers and decks that may be included in the memory device 900. The memory device 900 may include a substrate layer 505 and decks 515 of memory cells positioned above the substrate layer 505.

The cross-section view 1000 may be an example of the cross-section view 500 described with reference to FIG. 5.

[0095] In the memory device 900, the arrays of memory cells 510 (or the decks 515) are positioned over both the core portion 420 and the boundary portion 910. In this manner, the arrays of memory cells 510 may be positioned over the entire memory portion 905.

[0096] Such a configuration of arrays of memory cells 510 may be configured to compensate for memory cells that are inaccessible near the border 930. Some memory cells positioned above a substrate layer of a particular memory tile may be accessed using support circuitry in a neighboring memory tile. For memory tiles near or at a border, boundary tiles may be positioned such that all the memory cells above the memory tiles 430 are all fully accessible. Because the memory device 900 includes a boundary portion 910 on only one side of the core portion 420, some memory cells positioned over the core portion may not be accessible. In some examples, to compensate for inaccessible memory cells above the memory tiles 430, the memory cells may be positioned above the boundary portion 910. The boundary tiles 915 may include additional components associated with the memory cells positioned above the boundary tiles.

[0097] In some examples, the decks of memory cells 510 overlap the core portion 420 and the boundary portion 910 of the substrate layer 505. Meaning an array of memory cells may extend over or cover partly the core portion 420 and the boundary portion 910 of the substrate layer 505. For example, regions of the core portion 420 and/or the boundary portion 910 may not have memory cells positioned directly above them, but still the array of memory cells may overlap those regions. In some examples, the arrays of memory cells overlap at least a part of the boundary portion 910 of the substrate layer 505.

[0098] **FIG. 11** illustrates an example of a boundary tile configuration 1100 that supports efficient utilization of die area for cross-point architecture. FIG. 11 illustrates only components in the substrate layer for clarity. To facilitate access to the memory cells positioned above the boundary portion 910, the boundary tile configuration 1100 may include column line decoders 615. The column line decoder 615 may couple to column lines positioned above the boundary portion, where the column lines may be coupled to the memory cells positioned above the boundary portion 910. The boundary tile configuration 1100 may be an example of the boundary tiles 915 described with reference to FIGs. 9 and

10. The boundary tile configuration 1100 may be an example of the configuration 810 described with reference to FIG. 8.

[0099] The boundary tile configuration 1100 may be configured and arranged to be positioned on a first side of the core portion 420 (*e.g.*, the right side of the core portion 420 shown in FIG. 9). For example, the boundary tiles 915-1 and 915-2 may be arranged using the boundary tile configuration 1100. In other examples, boundary tile configuration 1100 may be configured and arranged to be positioned on a second side of the core portion 420 (*e.g.*, the left side of the core portion 420 shown in FIG. 9).

[0100] In some examples, column decoders 615 may be positioned between row decoders (*e.g.*, row line decoders 620, 625) and the control circuit portion 415. For example, column decoders 615 may be positioned between the first border 950 and row line decoders 620, 625. The first border 950 may be positioned opposite the fourth border 965 that defines the intersection of the core portion 420 and the boundary portion 910.

[0101] The boundary tile configuration 1100 may include a number of decoders that is less than a number of decoders in a memory tile 430 of the core portion 420. For example, because memory cells are positioned above the substrate layer of a boundary tiles 435, the boundary tile configurations 800 may include a number of column decoders 615. In some examples, the number of column decoders 615 is equal to half of a number of column decoders 615 in a memory tile 430 of the core portion 420. In other examples, the boundary tile configuration 1100 includes fewer row decoders 620, 625 and fewer sense amplifiers 630, 635 than are present in a memory tile 430 of the core portion 420. In some examples, the number of decoders in a single boundary tile configuration 1100 may be less than half of the number of decoders in a memory tile 430 of the core portion 420.

[0102] **FIG. 12** illustrates an example of a memory portion 1200 that supports efficient utilization of die area for cross-point architecture. FIG. 12 illustrates only components in the substrate layer and row lines for clarity. For example, portions of the memory tile may be omitted for clarity. In another example, row lines associated with different decks may be positioned at different heights in the memory device. As such, in some examples, row lines may overlap or may be stacked on top of one another. The row lines are shown offset in a two-dimensional arrangement for clarity purposes only. The memory portion 1200 may be an example of the memory portion 905 described with reference to FIG. 9. The memory portion 1200 shows the support components and some of the access lines of the memory tiles 430 and

the boundary tiles 915. In the illustrative examples of the memory portion, the memory tiles 430 and the boundary tiles 915 are spaced apart to provide additional clarity about where each tile begins and ends. In some examples, the memory portion 1200 does not include the gaps between the memory tiles 430 and the boundary tiles 915.

[0103] Some access lines may be truncated because these access lines are near or at a border. For example, various row lines 705, 710 may be truncated at various borders between the memory portion 1200 and the control circuit portion 415 of the memory device 900. Some truncated access lines are indicated as access line 1215. Truncated access lines may have a length that is less than a common length of access lines. Other access lines, other than the ones indicated, may also be truncated. For example, some access lines coupled to decoders located in border tiles may be shorter than access lines coupled to decoders located in core memory tiles. Some access lines coupled to decoders located in the core memory tiles may have a length less than the common length. This may be because array of memory cells ends at an edge. Access lines coupled to a first deck may have a different length than access lines coupled to a second deck. Access lines (e.g., row lines) associated with different decks of memory cells may have different lengths. For example, row lines 710 associated with a higher deck may be longer than row lines 705 associated with a lower deck. In some examples, border access lines may be coupled to a memory cell positioned above a substrate layer of a core memory tile. In some examples, border access lines may be coupled to a memory cell positioned above a substrate layer of a border tile. By coupling memory cells to border access lines additional storage capacity in selected column regions may be provided.

[0104] Some access lines may be removed from the memory portion 1200 or may be inactive. Because certain memory cells are accessed using support components in neighboring tiles, certain areas of memory cells near the borders may not be accessible. In situations where a decoder is not present to access certain memory cells, the access line associated with that decoder may not be included in the memory portion 1200 or may be inactive. Some areas where access lines are omitted, inactive, or not included in the memory portion 1200 are indicated as areas 1210. Other areas, other than the ones indicated, may be present in the memory portion 1200.

[0105] Similarly to the description herein, in each of the memory tiles 430 the row lines may be coupled to memory cells in the memory array. A particular row line may be dedicated to a particular deck of memory cells. Row lines may also be associated with row line

decoders for their respective deck. In the boundary tiles 915, row decoders for each deck may be associated to corresponding row lines of the array that are not associated to row decoders in the core portion memory tiles. Such a configuration may allow accessing an increased number of memory cell, as detailed herein.

[0106] **FIG. 13** illustrates an example of a memory portion 1300 that supports efficient utilization of die area for cross-point architecture. The memory portions 1300 may include a first memory portion 1305 and a second memory portion 1310. The memory portions 1300 may be examples of memory portions 905 and 1200 described with reference to FIGs. 9, 10, and 12.

[0107] The memory portions 1300 illustrate which memory cells may be accessed in the memory device 900. Because some memory cells are accessed using support components (*e.g.*, row decoders) positioned in neighboring tiles, not all memory cells may be accessible near the borders. Memory portion 1305 illustrates which memory cells are accessible in the first deck 515-1 of memory cells associated with the memory device 900. Memory portion 1310 illustrates which memory cells are accessible in the second deck 515-2 of memory cells associated with the memory device 900. More specifically, the memory portion 1300 correspond to the configuration of components shown in FIG. 12. The gray areas of the memory portions 1300 correspond to accessible memory cells. The white areas of the memory portions 1300 correspond to memory cells that are not accessible. In some embodiments, the inaccessible memory cells correspond with areas 1210 described with reference to FIG. 12. The memory portions 1300 are for illustrative purposes only. Other configurations of accessible memory cells are also possible. Configurations of accessible memory cells may be based on the configurations of the components in the memory portion 905 of the memory device 900.

[0108] **FIG. 14** illustrates an example of a memory portion 1400 that supports efficient utilization of die area for cross-point architecture. FIG. 14 illustrates only components in the substrate layer and row lines for clarity. For example, portions of the memory tile may be omitted for clarity. In another example, row lines associated with different decks may be positioned at different heights in the memory device. As such, in some examples, row lines may overlap or may be stacked on top of one another. The row lines are shown offset in a two-dimensional arrangement for clarity purposes only. The memory portion 1400 may be an example of memory portions 905, 1200, 1300 described with reference to FIGs. 9, 10, 12,

and 13. The memory portion 1400 shows the memory portion 905 with column lines 1405. The column lines 1405 may be examples of the word lines 110 described with reference to FIG. 1. In some instances, the column lines 1405 may be examples of the digit lines 115 described with reference to FIG. 1. References to word lines and bit lines, or their analogues are interchangeable without loss of understanding or operation. The column lines 1405 may be coupled to multiple decks of memory cells. In some instances, the column lines 1405 may be positioned between row lines 705, 710. For example, a column line 1405 may be positioned above row line 705 and row line 710 may be positioned above a column line 1405. Column lines 1405 may be coupled to or associated with column line decoders in the memory tiles (either in the core portion or the border portion) as described herein.

[0109] In some examples, an active memory cell in the array of memory cells is coupled to both a row line (*e.g.*, row line 705 or row line 710 depending on the deck) and a column line 1405. The column line 1405 extends perpendicular to the row line 705, 710, in some examples. An active memory cell may be an example of a memory cell that includes both a row address and a column address or is accessible by a memory controller.

[0110] A column line 1405 may define a common length between multiple column lines 1405. In some examples, a column line 1405 may have a length that is different from the common length. For example, a column line 1405 may be shorter or longer than the common length.

[0111] **FIG. 15** illustrates an example of a memory portion 1500 that supports efficient utilization of die area for cross-point architecture. The memory portion 1500 may be an example of memory portions 905, 1200, 1300, 1400 described with reference to FIGs. 9, 10, 12, 13, and 14. The memory portion 1500 may be illustrated to show how access operations may be used with the memory device 900. Some column lines are omitted in FIG. 15 for illustrative purposes only.

[0112] The memory portion 1500 may be broken into regions 1505. The memory portion 1500 may include eight regions (regions zero through seven). A region may comprise a collection of column lines 1405. As used herein, access operations may refer to read operations (*i.e.*, sense operations) or write operations. While eight regions 1505 are shown in FIG. 15, other numbers of regions may be configured.

[0113] During an access operation, a memory controller may activate one of the regions. For example, the memory controller may activate region three (3). A number of memory cells

are coupled to the column lines in region three (3) via the row lines that intersect the column lines in region three (3). In some examples, the number of access operations in a region is equal to the number of intersections 1510, 1515 of row lines and column lines in the region.

[0114] In memory portion 1500, each region is capable of performing a certain number of access operations. For example, in the illustrative example of memory portion 1500, region zero through region three may each be able to perform seventy-six access operations. Some cells in regions zero through three may not be accessible because the cells are near the border (*e.g.*, as shown in FIG. 13 where only decoded row lines are depicted). In addition, some cells positioned above the boundary portion may not be accessible, such as those positioned near the border at the boundary portion. However, other memory cells positioned above the boundary portion are available in regions zero through three. To illustrate the number of access operations, a detailed explanation of region 3 is presented. It should be appreciated that such a description also corresponds to regions 0, 1, and 2. The leftmost column line in region 3 is capable of accessing fourteen cells on the first deck via intersecting row lines for the first deck and is capable of accessing fourteen cells on the second deck via intersecting row lines for the second deck. The center column line in region 3 is capable of accessing sixteen cells on the first deck via intersecting row lines for the first deck and is capable of accessing sixteen cells on the second deck via intersecting row lines for the second deck. The rightmost column line in region 3 is capable of accessing eight cells on the first deck via intersecting row lines for the first deck and is capable of accessing eight cells on the second deck via intersecting row lines for the second deck. In total the column lines in region 3 (e.g., leftmost, center, and rightmost) are capable of accessing seventy-six memory cells. It should be appreciated that FIG. 15 may represent only a portion of a memory array. As such, the principles outlined may be expanded to cover additional and/or larger implementations.

[0115] In memory portion 1500, region four through region seven may each be able to perform sixty-four access operations. In the illustrative example, regions four through seven do not include accessing any memory cells positioned over the boundary portion 910. It should be appreciated that if the boundary portion 910 were positioned on the other side of the core portion 420, the numbering of the region numbers and characteristics may be different. For example, regions zero through three may be capable of performing sixty-four access operations and regions four through seven may be capable of performing seventy-six access operations. The number of access operations that are able to be performed by a region may vary depending on the size of the region and/or the size of the memory portion 1500. For

example, as the memory portion 1500 gets larger, the number of access operation able to be performed by a region may increase. To illustrate the number of access operations, a detailed explanation of region 5 is presented. It should be appreciated that such a description also corresponds to regions 4, 6, and 7. The leftmost column line in region 5 is capable of accessing sixteen cells on the first deck via intersecting row lines for the first deck and is capable of accessing sixteen cells on the second deck via intersecting row lines for the second deck. The rightmost column line in region 5 is capable of accessing sixteen cells on the first deck via intersecting row lines for the first deck and is capable of accessing sixteen cells on the second deck via intersecting row lines for the second deck. In total the column lines in region 5 (e.g., leftmost and rightmost) are capable of accessing sixty-four memory cells. It should be appreciated that FIG. 15 may represent only a portion of a memory array. As such, the principles outlined may be expanded to cover additional and/or larger implementations.

[0116] **FIG. 16** shows a block diagram 1600 of a memory array 1605 that supports efficient utilization of die area for cross-point architecture in accordance with various embodiments of the present disclosure. Memory array 1605 may be referred to as an electronic memory apparatus, and may be an example of a component of a memory controller 140 as described with reference to FIG. 1.

[0117] Memory array 1605 may include one or more memory cells 1610, a memory controller 1615, a word line 1620, a plate line 1625, a reference component 1630, a sense component 1635, a digit line 1640, and a latch 1645. These components may be in electronic communication with each other and may perform one or more of the functions described herein. In some cases, memory controller 1615 may include biasing component 1650 and timing component 1655.

[0118] Memory controller 1615 may be in electronic communication with word line 1620, digit line 1640, sense component 1635, and plate line 1625, which may be examples of word line 110, digit line 115, and sense component 125 described with reference to FIG. 1, and 2. Memory array 1605 may also include reference component 1630 and latch 1645. The components of memory array 1605 may be in electronic communication with each other and may perform some aspects of the functions described with reference to FIGs. 1 through 15. In some cases, reference component 1630, sense component 1635, and latch 1645 may be components of memory controller 1615.

[0119] In some examples, digit line 1640 is in electronic communication with sense component 1635 and a capacitor of memory cells 1610. In some examples, the capacitor may be a ferroelectric capacitor and the memory cell 1610 may be a ferroelectric memory cell. A memory cell 1610 may be writable with a logic state (*e.g.*, a first or second logic state). Word line 1620 may be in electronic communication with memory controller 1615 and a selection component of memory cell 1610. Plate line 1625 may be in electronic communication with memory controller 1615 and a plate of the capacitor of memory cell 1610. Sense component 1635 may be in electronic communication with memory controller 1615, digit line 1640, latch 1645, and reference line 1660. Reference component 1630 may be in electronic communication with memory controller 1615 and reference line 1660. Sense control line 1665 may be in electronic communication with sense component 1635 and memory controller 1615. These components may also be in electronic communication with other components, both inside and outside of memory array 1605, in addition to components not listed above, via other components, connections, or busses.

[0120] Memory controller 1615 may be configured to activate word line 1620, plate line 1625, or digit line 1640 by applying voltages to those various nodes. For example, biasing component 1650 may be configured to apply a voltage to operate memory cell 1610 to read or write memory cell 1610 as described above. In some cases, memory controller 1615 may include a row decoder, column decoder, or both, as described with reference to FIG. 1. This may enable memory controller 1615 to access one or more memory cells 105. Biasing component 1650 may also provide voltage potentials to reference component 1630 in order to generate a reference signal for sense component 1635. Additionally, biasing component 1650 may provide voltage potentials for the operation of sense component 1635.

[0121] In some cases, memory controller 1615 may perform its operations using timing component 1655. For example, timing component 1655 may control the timing of the various word line selections or plate biasing, including timing for switching and voltage application to perform the memory functions, such as reading and writing, discussed herein. In some cases, timing component 1655 may control the operations of biasing component 1650.

[0122] Reference component 1630 may include various components to generate a reference signal for sense component 1635. Reference component 1630 may include circuitry configured to produce a reference signal. In some cases, reference component 1630 may be implemented using other memory cells 105. Sense component 1635 may compare a signal

from memory cell 1610 (through digit line 1640) with a reference signal from reference component 1630. Upon determining the logic state, the sense component may then store the output in latch 1645, where it may be used in accordance with the operations of an electronic device that memory array 1605 is a part. Sense component 1635 may include a sense amplifier in electronic communication with the latch and the memory cell.

[0123] Memory controller 1615 may identify at least one cell of an array of memory cells that overlaps a boundary portion of a substrate layer, where the array is coupled to decoders of a core portion and the boundary portion via access lines, and where the substrate layer includes a control circuit portion exclusive of decoders and access the at least one cell using a decoder of the boundary portion. In some examples, the control circuit portion may be exclusive of row decoders, column decoders, sense amplifiers, or combinations thereof. In some examples, memory cells 1610 may comprise PCM or chalcogenide-material-based memory cells.

[0124] **FIG. 17** shows a block diagram 1700 of an access operation manager 1715 that supports efficient utilization of die area for cross-point architecture in accordance with various embodiments of the present disclosure. The access operation manager 1715 may be an example of embodiments of an access operation manager 1815 described with reference to FIGs. 15, 16, and 18. The access operation manager 1715 may include biasing component 1720, timing component 1725, memory cell manager 1730, decoder manager 1735, access line manager 1740, and portion manager 1745. Each of these modules may communicate, directly or indirectly, with one another (*e.g.*, via one or more buses).

[0125] Memory cell manager 1730 may identify at least one cell of an array of memory cells that overlaps a boundary portion of a substrate layer, where the array is coupled to decoders of a core portion and the boundary portion via access lines, and where the substrate layer includes a control circuit portion exclusive of decoders. Decoder manager 1735 may access the at least one cell using a decoder of the boundary portion.

[0126] Access line manager 1740 may be configured to manage access lines such as row lines or column lines. In some cases, accessing the at least one cell includes: activating an access line coupled between the at least one cell and a decoder of the boundary portion.

[0127] Portion manager 1745 may be configured to manage various parts of the memory device. In some cases, accessing the at least one cell includes: accessing a first portion of the array of memory cells that overlaps the core portion of the substrate layer and accessing a

second portion of the array of memory cells that overlaps the boundary portion of the substrate layer. In some cases, the core portion of the substrate layer includes a set of sections each that include a common configuration of components. In some cases, the boundary portion of the substrate layer includes a set of sections that each include a same configuration of components as other sections of the boundary portion, where the sections of the boundary portion have a different configuration of components from the sections of the core portion.

[0128] **FIG. 18** shows a diagram of a system 1800 including a device 1805 that supports efficient utilization of die area for cross-point architecture in accordance with various embodiments of the present disclosure. Device 1805 may be an example of or include the components of memory controller 140 as described above, *e.g.*, with reference to FIG. 1. Device 1805 may include components for bi-directional voice and data communications including components for transmitting and receiving communications, including access operation manager 1815, memory cells 1820, basic input/output system (BIOS) component 1825, processor 1830, I/O controller 1835, and peripheral components 1840. These components may be in electronic communication via one or more busses (*e.g.*, bus 1810).

[0129] Memory cells 1820 may store information (*i.e.*, in the form of a logical state) as described herein. BIOS component 1825 be a software component that includes BIOS operated as firmware, which may initialize and run various hardware components. BIOS component 1825 may also manage data flow between a processor and various other components, *e.g.*, peripheral components, input/output control component, *etc.* BIOS component 1825 may include a program or software stored in read only memory (ROM), flash memory, or any other non-volatile memory.

[0130] Processor 1830 may include an intelligent hardware device, (*e.g.*, a general-purpose processor, a digital signal processor (DSP), a central processing unit (CPU), a microcontroller, an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a programmable logic device, a discrete gate or transistor logic component, a discrete hardware component, or any combination thereof). In some cases, processor 1830 may be configured to operate a memory array using a memory controller. In other cases, a memory controller may be integrated into processor 1830. Processor 1830 may be configured to execute computer-readable instructions stored in a memory to perform various functions (*e.g.*, functions or tasks supporting reducing the die area by removing boundaries in a quilt architecture).

[0131] I/O controller 1835 may manage input and output signals for device 1805. I/O controller 1835 may also manage peripherals not integrated into device 1805. In some cases, I/O controller 1835 may represent a physical connection or port to an external peripheral. In some cases, I/O controller 1835 may utilize an operating system such as iOS®, ANDROID®, MS-DOS®, MS-WINDOWS®, OS/2®, UNIX®, LINUX®, or another known operating system.

[0132] Peripheral components 1840 may include any input or output device, or an interface for such devices. Examples may include disk controllers, sound controller, graphics controller, Ethernet controller, modem, universal serial bus (USB) controller, a serial or parallel port, or peripheral card slots, such as peripheral component interconnect (PCI) or accelerated graphics port (AGP) slots.

[0133] Input 1845 may represent a device or signal external to device 1805 that provides input to device 1805 or its components. This may include a user interface or an interface with or between other devices. In some cases, input 1845 may be managed by I/O controller 1835, and may interact with device 1805 via a peripheral component 1840.

[0134] Output 1850 may also represent a device or signal external to device 1805 configured to receive output from device 1805 or any of its components. Examples of output 1850 may include a display, audio speakers, a printing device, another processor or printed circuit board, *etc.* In some cases, output 1850 may be a peripheral element that interfaces with device 1805 via peripheral component(s) 1840. In some cases, output 1850 may be managed by I/O controller 1835.

[0135] The components of device 1805 may include circuitry designed to carry out their functions. This may include various circuit elements, for example, conductive lines, transistors, capacitors, inductors, resistors, amplifiers, or other active or inactive elements, configured to carry out the functions described herein. Device 1805 may be a computer, a server, a laptop computer, a notebook computer, a tablet computer, a mobile phone, a wearable electronic device, a personal electronic device, or the like. Or device 1805 may be a portion or element of such a device.

[0136] **FIG. 19** shows a flowchart illustrating a method 1900 that supports efficient utilization of die area for cross-point architecture in accordance with various embodiments of the present disclosure. The operations of method 1900 may be implemented by a memory controller 140 or its components as described herein. For example, the operations of method

1900 may be performed by an access operation manager as described with reference to FIGs. 16 through 18. In some examples, a memory controller 140 may execute a set of codes to control the functional elements of the device to perform the functions described below. Additionally or alternatively, the memory controller 140 may perform some of the functions described below using special-purpose hardware.

[0137] In some cases, the method may also include identifying at least one cell of an array of memory cells that overlaps a boundary portion of a substrate layer, wherein the array is coupled to decoders of a core portion and the boundary portion via access lines, and wherein the substrate layer includes a control circuit portion exclusive of decoders. In some cases, the method may also include accessing the at least one cell using a decoder of the boundary portion. In some cases, accessing the at least one cell comprises: activating an access line coupled between the at least one cell and a decoder of the boundary portion. In some cases, accessing the at least one cell comprises: accessing a first portion of the array of memory cells that overlaps the core portion of the substrate layer and accessing a second portion of the array of memory cells that overlaps the boundary portion of the substrate layer. In some cases, the core portion of the substrate layer comprises a plurality of sections each that include a common configuration of components. In some cases, the boundary portion of the substrate layer comprises a plurality of sections that each include a same configuration of components as other sections of the boundary portion, wherein the sections of the boundary portion have a different configuration of components from the sections of the core portion. In some cases, accessing the at least one cell comprises: activating an access line coupled to the at least one cell and to the decoder of the boundary portion, the access line being shorter than an access line coupled to a decoder of the core portion.

[0138] At block 1905 the memory controller 140 may identify at least one cell of an array of memory cells that overlaps a boundary portion of a substrate layer, wherein the array is coupled to decoders of a core portion and the boundary portion via access lines, and wherein the substrate layer includes a control circuit portion exclusive of decoders. The operations of block 1905 may be performed according

to the methods described with reference to FIGs. 1 through 15. In certain examples, embodiments of the operations of block 1905 may be performed by a memory cell manager as described with reference to FIGs. 16 through 18.

[0139] At block 1910 the memory controller 140 may access the at least one cell using a decoder of the boundary portion. The operations of block 1910 may be performed according to the methods described with reference to FIGs. 1 through 15. In certain examples, embodiments of the operations of block 1910 may be performed by a decoder manager as described with reference to FIGs. 16 through 18.

[0140] An apparatus for performing the method 1900 is described. The apparatus may include means for identifying at least one cell of an array of memory cells that overlaps a boundary portion of a substrate layer, and means for accessing the at least one cell using a decoder of the boundary portion. In some cases, the array is coupled to decoders of a core portion and the boundary portion via access lines. In some cases, the substrate layer includes a control circuit portion exclusive of decoders

[0141] In some examples of the method 1900 and apparatus described above may further include processes, features, means, or instructions for activating an access line coupled between the at least one cell and a decoder of the boundary portion. Some examples of the method 1900 and apparatus described above may further include processes, features, means, or instructions for accessing a first portion of the array of memory cells that overlaps the core portion of the substrate layer and accessing a second portion of the array of memory cells that overlaps the boundary portion of the substrate layer.

[0142] In some examples of the method 1900 and apparatus described above, the core portion of the substrate layer comprises a plurality of sections each that include a common configuration of components.

[0143] In some examples of the method 1900 and apparatus described above, the boundary portion of the substrate layer comprises a plurality of sections that each include a same configuration of components as other sections of the boundary portion. In some cases, the sections of the boundary portion have a different configuration of components from the sections of the core portion.

[0144] Some examples of the method 1900 and apparatus described above may further include processes, features, means, or instructions for activating an access line coupled to the at least one cell and to the decoder of the boundary portion, the access line being shorter than an access line coupled to a decoder of the core portion.

[0145] It should be noted that the methods described above describe possible implementations, and that the operations and the steps may be rearranged or otherwise

modified and that other implementations are possible. Furthermore, features or steps from two or more of the methods may be combined.

[0146] Information and signals described herein may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof. Some drawings may illustrate signals as a single signal; however, it will be understood by a person of ordinary skill in the art that the signal may represent a bus of signals, where the bus may have a variety of bit widths.

[0147] As used herein, the term "virtual ground" refers to a node of an electrical circuit that is held at a voltage of approximately zero volts (0V) but that is not directly connected with ground. Accordingly, the voltage of a virtual ground may temporarily fluctuate and return to approximately 0V at steady state. A virtual ground may be implemented using various electronic circuit elements, such as a voltage divider consisting of operational amplifiers and resistors. Other implementations are also possible. "Virtual grounding" or "virtually grounded" means connected to approximately 0V.

[0148] The term "electronic communication" refers to a relationship between components that supports electron flow between the components. This may include a direct connection between components or may include intermediate components. Components in electronic communication may be actively exchanging electrons or signals (*e.g.*, in an energized circuit) or may not be actively exchanging electrons or signals (*e.g.*, in a de-energized circuit) but may be configured and operable to exchange electrons or signals upon a circuit being energized. By way of example, two components physically connected via a switch (*e.g.*, a transistor) are in electronic communication regardless of the state of the switch (*i.e.*, open or closed).

[0149] The term "isolated" refers to a relationship between components in which electrons are not presently capable of flowing between them; components are isolated from each other if there is an open circuit between them. For example, two components physically connected by a switch may be isolated from each other when the switch is open.

[0150] As used herein, the term "shorting" refers to a relationship between components in which a conductive path is established between the components via the activation of a single

intermediary component between the two components in question. For example, a first component shorted to a second component may exchange electrons with the second component when a switch between the two components is closed. Thus, shorting may be a dynamic operation that enables the flow of charge between components (or lines) that are in electronic communication.

[0151] The devices discussed herein, including memory device 100, may be formed on a semiconductor substrate, such as silicon (Si), germanium, silicon-germanium alloy, gallium arsenide (GaAs), gallium nitride (GaN), etc. In some cases, the substrate is a semiconductor wafer. In other cases, the substrate may be a silicon-on-insulator (SOI) substrate, such as silicon-on-glass (SOG) or silicon-on-sapphire (SOP), or epitaxial layers of semiconductor materials on another substrate. The conductivity of the substrate, or sub-regions of the substrate, may be controlled through doping using various chemical species including, but not limited to, phosphorous, boron, or arsenic. Doping may be performed during the initial formation or growth of the substrate, by ion-implantation, or by any other doping means.

[0152] Chalcogenide materials may be materials or alloys that include at least one of the elements S, Se, and Te. Phase change materials discussed herein may be chalcogenide materials. Chalcogenide materials may include alloys of S, Se, Te, Ge, As, Al, Sb, Au, indium (In), gallium (Ga), tin (Sn), bismuth (Bi), palladium (Pd), cobalt (Co), oxygen (O), silver (Ag), nickel (Ni), platinum (Pt). Example chalcogenide materials and alloys may include, but are not limited to, Ge-Te, In-Se, Sb-Te, Ga-Sb, In-Sb, As-Te, Al-Te, Ge-Sb-Te, Te-Ge-As, In-Sb-Te, Te-Sn-Se, Ge-Se-Ga, Bi-Se-Sb, Ga-Se-Te, Sn-Sb-Te, In-Sb-Ge, Te-Ge-Sb-S, Te-Ge-Sn-O, Te-Ge-Sn-Au, Pd-Te-Ge-Sn, In-Se-Ti-Co, Ge-Sb-Te-Pd, Ge-Sb-Te-Co, Sb-Te-Bi-Se, Ag-In-Sb-Te, Ge-Sb-Se-Te, Ge-Sn-Sb-Te, Ge-Te-Sn-Ni, Ge-Te-Sn-Pd, or Ge-Te-Sn-Pt. The hyphenated chemical composition notation, as used herein, indicates the elements included in a particular compound or alloy and is intended to represent all stoichiometries involving the indicated elements. For example, Ge-Te may include Ge_xTe_y, where x and y may be any positive integer. Other examples of variable resistance materials may include binary metal oxide materials or mixed valence oxide including two or more metals, e.g., transition metals, alkaline earth metals, and/or rare earth metals. Embodiments are not limited to a particular variable resistance material or materials associated with the memory components of the memory cells. For example, other examples of variable resistance materials can be used to form memory components and may include chalcogenide materials, colossal magnetoresistive materials, or polymer-based materials, among others.

[0153] A transistor or transistors discussed herein may represent a field-effect transistor (FET) and comprise a three terminal device including a source, drain, and gate. The terminals may be connected to other electronic components through conductive materials, *e.g.*, metals. The source and drain may be conductive and may comprise a heavily-doped, *e.g.*, degenerate, semiconductor region. The source and drain may be separated by a lightly-doped semiconductor region or channel. If the channel is n-type (*i.e.*, majority carriers are electrons), then the FET may be referred to as a n-type FET. If the channel is p-type (*i.e.*, majority carriers are holes), then the FET may be referred to as a p-type FET. The channel may be capped by an insulating gate oxide. The channel conductivity may be controlled by applying a voltage to the gate. For example, applying a positive voltage or negative voltage to an n-type FET or a p-type FET, respectively, may result in the channel becoming conductive. A transistor may be "on" or "activated" when a voltage greater than or equal to the transistor's threshold voltage is applied to the transistor gate. The transistor may be "off" or "deactivated" when a voltage less than the transistor's threshold voltage is applied to the transistor gate.

[0154] The description set forth herein, in connection with the appended drawings, describes example configurations and does not represent all the examples that may be implemented or that are within the scope of the claims. The term "exemplary" used herein means "serving as an example, instance, or illustration," and not "preferred" or "advantageous over other examples." The detailed description includes specific details for the purpose of providing an understanding of the described techniques. These techniques, however, may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the concepts of the described examples.

[0155] In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label, such as a letter or number, that distinguishes among the similar components. If just the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0156] Information and signals described herein may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands,

information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0157] The various illustrative blocks and modules described in connection with the disclosure herein may be implemented or performed with a general-purpose processor, a DSP, an ASIC, an FPGA or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices (*e.g.*, a combination of a digital signal processor (DSP) and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration).

[0158] The functions described herein may be implemented in hardware, software executed by a processor, firmware, or any combination thereof. If implemented in software executed by a processor, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Other examples and implementations are within the scope of the disclosure and appended claims. For example, due to the nature of software, functions described above can be implemented using software executed by a processor, hardware, firmware, hardwiring, or combinations of any of these. Features implementing functions may also be physically located at various positions, including being distributed such that portions of functions are implemented at different physical locations. Also, as used herein, including in the claims, "or" as used in a list of items (for example, a list of items prefaced by a phrase such as "at least one of" or "one or more of") indicates an inclusive list such that, for example, a list of at least one of A, B, or C means A or B or C or AB or AC or BC or ABC (*i.e.*, A and B and C). Also, as used herein, the phrase "based on" shall not be construed as a reference to a closed set of conditions. For example, an exemplary step that is described as "based on condition A" may be based on both a condition A and a condition B without departing from the scope of the present disclosure. In other words, as used herein, the phrase "based on" shall be construed in the same manner as the phrase "based at least in part on."

[0159] Computer-readable media includes both non-transitory computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A non-transitory storage medium may be any available medium that can be accessed by a general purpose or special purpose computer. By way of example, and not limitation, non-transitory computer-readable media can comprise RAM, ROM, electrically erasable programmable read only memory (EEPROM), compact disk (CD) ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other non-transitory medium that can be used to carry or store desired program code means in the form of instructions or data structures and that can be accessed by a general-purpose or special-purpose computer, or a general-purpose or special-purpose processor. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, include CD, laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above are also included within the scope of computer-readable media.

[0160] The description herein is provided to enable a person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not limited to the examples and designs described herein, but is to be accorded the broadest scope consistent with the principles and novel features disclosed herein.

CLAIMS

What is claimed is:

1. An electronic memory device, comprising:

a substrate layer that comprises a core portion, a boundary portion, and a control circuit portion, wherein the core portion includes a first plurality of decoders having a first configuration, the boundary portion includes a second plurality of decoders having a second configuration different from the first configuration, and the control circuit portion is exclusive of decoders; and

an array of memory cells that overlaps the core portion and at least a part of the boundary portion of the substrate layer, wherein memory cells of the array are coupled with the first plurality of decoders and the second plurality of decoders via a plurality of access lines.

2. The device of claim 1, wherein:

the second plurality of decoders includes a plurality of column decoders.

3. The device of claim 2, wherein:

the plurality of column decoders are associated with memory cells of the array that overlap the boundary portion.

4. The device of claim 2, wherein:

the second plurality of decoders includes a plurality of row decoders.

5. The device of claim 1, wherein:

at least one decoder of the first plurality of decoders is coupled with a memory cell of the array of memory cells that overlaps the boundary portion.

6. The device of claim 1, wherein:

at least one decoder of the second plurality of decoders is coupled with a memory cell of the array that overlaps the boundary portion.

7. The device of claim 1, wherein:

the core portion of the substrate layer comprises a plurality of sections that each include a common configuration of components.

8. The device of claim 7, wherein:

the boundary portion comprises a plurality of sections that each include a same configuration as other sections of the boundary portion, wherein the sections of the boundary portion have a different configuration from the sections of the core portion.

9. The device of claim 8, wherein:

each section of the core portion is defined by a first dimension in a first direction and a second dimension in a second direction that is orthogonal to the first direction; and

each section of the boundary portion is defined by a third dimension in the first direction and a fourth dimension in the second direction, wherein the third dimension is less than the first dimension and the fourth dimension is equal to the second dimension.

10. The device of claim 8, wherein:

at least one section of the boundary portion includes a first number of decoders that is less than a second number of decoders included in at least one section of the core portion.

11. The device of claim 10, wherein:

the first number of decoders is less than half of the second number of decoders.

12. The device of claim 1, wherein:

the array of memory cells includes at least two decks of memory cells, a first deck of memory cells positioned over the core portion and the boundary portion and a second deck of memory cells positioned over the first deck of memory cells.

13. The device of claim 1, wherein:

the core portion and the boundary portion comprise a CMOS under array (CuA).

14. The device of claim 1, wherein:

the control circuit portion is exclusive of row decoders and column decoders.

15. An electronic memory device, comprising:

a substrate layer that comprises a core portion, a boundary portion, and a control circuit portion, wherein the core portion includes a first plurality of decoders having a first configuration, the boundary portion includes a second plurality of decoders having a second configuration different from the first configuration, and the control circuit portion is exclusive of decoders, wherein the core portion comprises a first border and a second border positioned opposite the first border, the first border defining a first boundary between the core portion and the control circuit portion and the second border defining a second boundary between the core portion and the boundary portion; and

an array of memory cells including a first subset of memory cells positioned over the core portion of the substrate layer and a second subset of memory cells positioned over the boundary portion of the substrate layer, wherein the first subset of memory cells are coupled with the first plurality of decoders and the second subset of memory cells are coupled with the second plurality of decoders via a plurality of access lines.

16. The device of claim 15, wherein:

the core portion further comprises: a third border defining a third boundary between the core portion and the control circuit portion; and

the device further comprising a fourth border positioned opposite the third border, the fourth border defining a fourth boundary between the core portion and the control circuit portion.

17. The device of claim 15, further comprising:

a subset of access lines extends across the second boundary defined by the second border of the core portion, wherein the subset of access lines is coupled with the second subset of memory cells.

18. The device of claim 15, wherein:

at least one of the second plurality of decoders is configured to access a memory cell of the second subset of memory cells.

19. The device of claim 15, wherein:

at least one of the first plurality of decoders is configured to access a memory cell of the second subset of memory cells.

20. The device of claim 15, wherein:

the core portion of the substrate layer comprises a plurality of sections that each include a common configuration of components.

21. The device of claim 15, wherein:

the boundary portion comprises a first boundary border cooperating with the second border of the core portion to define the second boundary between the boundary portion and the core portion and a second boundary border positioned opposite the first boundary border, the second boundary border defining a third boundary between the boundary portion and the control circuit portion.

22. The device of claim 21, further comprising:

a plurality of column decoders positioned between each row decoder of the second plurality of decoders and the second boundary border.

23. The device of claim 15, further comprising:

a first subset of access lines terminate at the first border and define a first length less than a second length of a second subset of access lines.

24. The device of claim 15, further comprising:

a third subset of access lines are positioned in the boundary portion, each access line of the third subset of access lines terminating at the control circuit portion.

25. The device of claim 15, wherein:

an active memory cell in the array of memory cells is coupled to a first access line and a second access line extending perpendicular to the first access line.

26. An electronic memory device, comprising:

a substrate layer that comprises a core portion, a boundary portion, and a control circuit portion, wherein the core portion includes a first plurality of decoders having a first configuration, the boundary portion includes a second plurality of decoders having a second configuration different from the first configuration and the boundary portion comprises a plurality of column decoders, and the control circuit portion is exclusive of decoders; and

an array of memory cells positioned over at least the core portion of the substrate layer, wherein memory cells of the array of memory cells are coupled with the first plurality of decoders and the second plurality of decoders via a plurality of access lines.

27. The device of claim 26, wherein:

the plurality of column decoders are configured to assist in accessing memory cells positioned over the boundary portion.

28. The device of claim 27, further comprising:

a subset of the array of memory cells positioned over the boundary portion of the substrate layer, and wherein plurality of the column decoders are coupled to the subset of the array of memory cells positioned over the boundary portion.

29. An electronic memory device, comprising:

a substrate layer that comprises a core portion, a boundary portion, and a control circuit portion, wherein the core portion includes a first plurality of decoders having a first configuration, the boundary portion includes a second plurality of decoders having a second configuration different from the first configuration, and the control circuit portion is exclusive of decoders;

an array of memory cells that overlaps the core portion and at least a part of the boundary portion of the substrate layer, wherein memory cells of the array are coupled with the first plurality of decoders and the second plurality of decoders via a plurality of access lines;

a controller in electronic communication with the substrate layer and the array of memory cells, wherein the controller is operable to:

identify a region of the array of memory cells to access during an access operation;

determine that the identified region of the array of memory cells includes memory cells positioned over the boundary portion of the substrate layer; and

execute the access operation on the memory cells that are part of the identified region and are positioned over the boundary portion of the substrate layer based at least in part on the determination using decoders of the first plurality or the second plurality.