

PATENT SPECIFICATION

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(54) VIDEO DISPLAY SYSTEM

(71) We, HONEYWELL INFORMATION SYSTEMS INC., a Corporation organised and existing under the laws of the State of Delaware, United States of America of 200 Smith Street, Waltham, Massachusetts 02154, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates generally to the video display of information on a display apparatus. In particular, this invention relates to the manner in which information is initially entered and thereafter displayed on a communication terminal.

Information which is to appear on a video display of a communication terminal is often first stored in a memory within the terminal device itself. This stored information is sequentially accessed from the memory and subsequently displayed on a cathode ray tube commonly known as a CRT. The sequential accessing from memory and subsequent display of information on the CRT is usually accomplished at a sufficiently rapid rate to create the impression of a continuous image to the viewer. The image usually appears as a number of distinct rows of characters arranged across the CRT.

In order to preserve continuity in the image thus being viewed, it is common practice to initially enter new information on the bottommost row of the video display. The previously appearing rows of characters are simultaneously moved upwardly on the display so that the data previously appearing in the bottommost row reappears in the row next to the bottommost row. In this manner, each succeeding row appears one row above its previous display position. This is commonly referred to as a "roll-over" of displayed information.

In order to facilitate the aforementioned roll-over of information internally, it has

heretofore been a common practice to rearrange the rows of information within the memory portion of the display device. To do this, the previous topmost row is erased from that portion of memory dedicated to storing the topmost row. At the same time, each of the other rows appearing below the previous topmost row is erased from its particular memory location and rewritten in the memory location for the next row above it. In this manner, the previous bottommost row is moved to the next-to-bottom row, and the topmost row which has been previously displayed is erased and no longer internally stored within memory.

It is evident that a considerable amount of time is thus expended in the reconfiguration of the internal memory during a roll-over of displayed information. Furthermore, a considerable amount of logic must be dedicated to the task of reconfiguring the internal memory in good time. Finally, it is evident that this logic must be operational for long periods of time when new information is sequentially being displayed on a display device.

We have now discovered that it is possible to avoid this complete reconfiguration of the stored information within the memory.

Accordingly, the present invention provides a video display system comprising:
a memory having a plurality of storage locations, arranged in rows and columns, for storing respective characters;
a display device on which the stored characters may be displayed in a corresponding number of rows and columns;

video row and column counters which select characters from memory for display and locate their display on the display device.

storage row and column counters which select locations in memory for storing incoming characters;

multiplexing means which select outputs from the storage or video column counters

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and from a fixed count value or the video row counters for storing or display respectively; and

means for adding, modulo the number of rows, the output of the storage row counter to the row count selected by the multiplexer to determine the row of memory to be addressed.

Figure 1 shows a keyboard entry computer terminal with a video display;

Figure 2 illustrates the video display appearing on the computer terminal of Figure 1;

Figure 3 illustrates a particular character formed on the video display of Figure 2; and

Figure 4 is a block diagram of the logic utilized in the terminal of Figure 1.

Figure 1 shows a communications terminal 10 with a keyboard 12 for data entry and a video display 14 for data display. The video display 14 is capable of displaying information received either from the keyboard 12 or from an external communication line attached to the terminal 10.

Figure 2 shows the video display 14 of Figure 1 enlarged. There are twelve rows 16 across the video display 14, each of which contains a number of alphanumeric characters sequentially formed from left to right in up to eighty column positions 18, the rows 16 and columns 18 forming a matrix 20 of 12x80 character positions. Such an arrangement of characters is formed row by row with the characters sequentially formed from left to right in the column locations within a given row.

Figure 3 shows a particular row and column location with the particular alphanumeric character being the letter "E", which comprises a plurality of illuminated dots. The character is formed by sequentially illuminating dots along a group of horizontal lines 0-9 beginning with the second horizontal line. Dots are illuminated within a particular horizontal line beginning with the second dot location, 1' and extending to the sixth dot location 5'. The horizontal line counts are thus 0 to 9 and the vertical dots counts are 0' to 6' in Figure 3. It is to be noted that the dot counts begin at 1' and extend to 5' and the line counts begin at 1 and extend to 7; no part of a character is formed during a line count of 8, 9 or 0.

Figure 4 illustrates in block diagram form the internal logic essential to forming the characters appearing on the display 14. The display logic of Figure 4 first receives a data input from either the keyboard 12 of the terminal 10 or an external communications source to the terminal 10. This data input is subsequently processed through the display

logic of Figure 4 and exits as a video output to be displayed on the video display 14.

The data input appears at a terminal 22 and consists of either a serial flow of information from an external communication line or a parallel input from the keyboard 12, with a character being defined when seven data bits are received from either source. The seven data bits are encoded in accordance with the standard seven-bit ASCII code. This code differentiates between characters that are subsequently to be displayed and characters that are merely to serve as internal control for the communications terminal 10, the sixth and seventh bits of a control character being zero.

The data input appearing on the terminal 22 is applied to a conventional uniform asynchronous receiver transmitter (UART) which converts the data input for each character into a seven-bit parallel output which is applied to a control circuit 26 and a memory 28 via a bus 30. The control circuit 26 first of all decodes the sixth and seventh bits of the seven-bit parallel input from the UART 24 so as to determine whether or not the seven-bit character is a control character or a display character. If a display character is identified, then a write data signal is generated and applied to a memory control 32 via a line 34. The memory control circuit 32 subsequently conditions the memory 28 via a line 35 for receipt of the seven-bit character appearing on the bus 30. The control circuit 26 may conveniently contain an OR gate fed with the sixth and seventh bits of the character on bus 30 and a set of four decoder circuits which detect the first to fifth bits of the four control characters described below and disabled by the output of the OR gate. The OR gate also feeds the memory control circuit 32, which may conveniently consist of two one-shots in series, the first generating the signal on line 35 and the second generating a signal on a line 36 which increments a column feed counter 38. The column feed counter 38 is a scale-of-eighty counter, each count corresponding to a respective one of the eighty columns of the display, and maintains a column count of the newly-entered information to the memory 28. It will be remembered from a discussion of Figure 2 that each character occupies a particular column position within a row; hence each time an additional character is entered, it must be counted as a column increment.

The column feed counter 38 also receives three additional signals from the control circuit 26; namely a forward space signal, a back space signal, and a carriage return signal, on lines 40, 42

and 44 respectively. Each of these signals is generated by decoding of a particular control character. When a control character is thus decoded, the write data signal remains inoperative thereby not activating the memory control 32, and control characters are thus never stored in the memory 28.

The control circuit 26 also produces a row feed signal in response to a row feed control character. The row feed signal is fed over a line 48 to a row feed counter 46 which maintains a cyclical row feed count equal to the number of newly-entered rows in the memory 28 and corresponding to the video display 14 of Figure 2. This counter is a cyclic scale-of-twelve counter, counting from 0 to 11, corresponding to the twelve rows that can be displayed. This row feed count is applied to an address adder 50 over a bus 52.

The column feed counter 38 applies the column feed count signal over a bus 54 to the column count input side 56 of an address multiplex circuit 58. The column input 56 of the address multiplex circuit 58 also receives a video column count from a video column counter 60. The column feed count and the video column count are seven-bit cyclical counts defining an eighty column count corresponding to eighty character positions in a given row on the video display 14 of Figure 2.

The address multiplex circuit 58 also contains a row input terminal 62 which receives a four-bit video row count from a video row counter 64 and a constant input row count, set at eleven, which identifies the twelfth and bottommost row in the video display 14. As will become apparent hereinafter, this input row count guarantees that the latest information to be entered into the memory 28 will always be in the bottommost row position of the video display 14.

The address multiplex circuit 58 gates either the input row count and the column feed count, or the video row and column counts, dependent on the video line count from a video line counter 66. It will be remembered from the discussion of Figure 3 that a character is not displayed during a video line count of eight, nine or zero. These particular line counts permit the gating of the constant row input count and the particular line counts permit the gating of the constant row input count and the column feed count. When the video line count is other than eight, nine or zero, the video row and column counts are gated by the address multiplex circuit 58. This circuit may conveniently contain decoder circuitry for detecting the "one" and "eight" counts of the video line counter 66; a flip-flop which is set by the decoded "eight" count

and reset by the decoded "one" count, thus being in the set state for counts of eight, nine, and zero; and 11-bit multiplexing gate circuitry which gates the constant row input count and column feed count through when the flip-flop is set and the video row and column counts through when the flip-flop is reset.

The row and column counts from the multiplex circuit 58 form an initial address which is applied to an address adder 50 via bus 68. The address adder 50 adds the row feed count from bus 52 to the row portion of the address appearing on bus 68. The resulting address is fed via bus 70 to a memory address interface 72 which adjusts the resulting address from the address adder 50 so as to conform to the addressing within the memory 28, by reducing the two portion of the address modulo 12 (leaving the column portion unchanged).

More specifically, the memory address interface 72 operates to determine whether the row portion of the address from the adder 50 is in the range 0 to 11 or the range 12 to 23, and if it is in the latter range, to reduce it by 12 (so that it is transformed into the range 0 to 11). This may conveniently be done as follows. Let the 11 bits of the address from the multiplexer circuit 58 be called A_1 to A_{11} , where the first 7 bits are the column portion of the address and the last 4 bits (A_8 to A_{11}) the row portion, and the four bits from the row feed counter 52 be called R_1 to R_4 . In the adder 50, bits R_1 to R_4 are added to bits A_8 to A_{11} , producing sum bits B_8 to B_{12} . (The low order A bits A_1 to A_7 pass through unchanged). In the memory address interface 72, the low-order A bits A_1 to A_7 , again pass through unchanged, but the sum bits B_8 to B_{12} must be reduced to modulo 12 form. For this, bits B_8 and B_9 are simply passed on unchanged, but bit B_{10} must be inverted for counts (B_8 to B_{12}) of 12 to 23, and bit B_{11} must be inverted for counts of 12 to 15 and 20 to 23. (Bit B_{12} is always converted to binary 0, and thus does not pass on at all.) Two logic circuits are therefore provided. The first mechanizes the logical expression

$$\overline{B_{10}} \cdot \overline{B_{11}} \cdot \overline{B_{12}},$$

which is true for counts 0 to 11 and false for counts 12 to 23; this logic circuit controls a conditional inverter for signal B_{10} , which is inverted when the expression is false. The second logic circuit mechanizes the logical expression

$$\overline{B_{10}} \cdot \overline{B_{11}} \cdot \overline{B_{10}} \cdot \overline{B_{12}},$$

which is true for counts 0 to 11 and 16 to 19

and false for counts 12 to 15 and 20 to 23; this logic circuit controls a conditional inverter for signal B_{11} , which is inverted when the expression is false.

The adjusted memory address is applied to the memory 28 via a bus 74. The adjusted address defines a location within the memory 28 for either a storage (write) operation or a display (read) operation. If a storage operation is to take place, the adjusted address defines a location in memory into which the character is to be stored. If on the other hand, a display operation is to occur, then the character stored at the particular adjusted address location within memory is made available to a character generator 76. The character generator 76 subsequently generates each line of the dot pattern for the character. This information is loaded into a video register 80 pursuant to a line count from the video line counter 66. The stored dot pattern for the particular line count is thereafter serially shifted from the video register 80 in response to the dot count from the video dot counter 82. The dot information is subsequently displayed in a continuous illuminated path by the raster sweep of the CRT. A visual representation of the character thus appears at the particular row and column location defined by the original video row and column counts.

The raster sweep of the CRT is slaved to a master clock which also drives the video dot counter 82. In this manner, a common clocking is maintained between the various video counts and the raster sweep of the CRT. Also, a definitive relationship exists between the various video counts. Thus the video column counter cycles through eighty column counts during each particular row count. At the same time, the video line counter provides ten individual line counts within each row count, and the video dot counter provides seven separate dot counts within each column count. The line count and dot counts are of course dictated by the character formation requirements of Figure 3 whereas the row and column counts are dictated by the row and column arrangement of Figure 2.

In operation, the system reads information from the memory for display during video line counts one to eight, and stores incoming information in the memory during video line counts nine, ten, and zero.

During display periods, the particular location addressed in memory is determined by the video row and column counters. The column counter determines the column of the memory location directly. The row counter, however, has its count added, modulo 12, to the count in the row feed counter. Thus the count in the row

feed counter determines which row of locations in memory is displayed as the first (top) row, row count 0 from the video row counter. The next row down in the memory is displayed as the second row, the video row counter count of 1 being added to the row feed counter count to locate the appropriate row of locations in the memory. Successively lower rows of locations in the memory are read out as successively lower rows for display. When the last (twelfth) row of locations in the memory is read out, the modulo 12 summing of the row addresses results in the first row of locations in the memory being selected next. Thus the rows of locations in the memory are in effect arranged cyclically, with the row feed counter selecting one of them as the first for read-out for display.

During storage periods, the column feed counter selects the appropriate column of storage locations in the memory for storing fresh information. The row feed counter defines, as mentioned above, the row of storage locations corresponding to the first row on the display. Incoming information, however, has to be stored in the last row of the display. The constant count of 11 (binary 1011) is therefore selected by the address multiplex circuit and added, modulo 12, to the count from the row feed counter to select the row of locations which is 11 rows on (i.e. 1 row back) in the memory from the row defined by the row feed counter. Thus the count from the row feed counter is reduced by 1 (modulo 12) to select the row of locations containing the most recent information for the storage of further information into that row.

The three column feed counter control signals—forward space, back space, and carriage return—are self-explanatory; these respective increment the column feed counter count by 1, decrease it by 1, and reset it to 0. The row feed signal steps on the row feed counter cyclically by 1, thereby causing what was the oldest row in the memory to be regarded instead as the most recent row. This row will therefore now be displayed at row 12 on the display, and will have incoming information written into it.

It will be realized that much of the circuitry of this system is conventional. The main circuits not present in the prior systems are: the row feed counter; the address adder; and the memory address interface. However, in the prior art, the receipt of a row feed control signal brought into action circuitry, not present in the present system, which carried out a read-shift-write cycle through the entire memory, moving each stored character down one row in its respective column. It

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WHAT WE CLAIM IS:—

1. A video display system comprising:
a memory having a plurality of storage locations, arranged in rows and columns for storing respective characters;

a display device on which the stored characters may be displayed in a corresponding number of rows and columns;

video row and column counters which select characters from memory for display and locate their display on the display device;

storage row and column counters which select locations in memory for storing incoming characters;

multiplexing means which select outputs from the storage or video column counters and from a fixed count value or the video row counter for storing or display respectively; and

means for adding, modulo the number of rows, the output of the storage row counter to the row selected by the multiplexer to determine the row of memory to be addressed.

2. A video display system substantially as herein described with reference to the accompanying drawings.

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