

ABSTRACT

A memory device includes a memory cell array including a plurality of memory cells; a voltage generator configured to generate voltages used for a program operation and a verify operation for the memory cells; and control logic configured to perform a plurality of program loops while writing data to the memory cell array, such that first to N-th (e.g., $N \geq 1$) program loops including a program operation and a verify operation are performed and at least two program loops in which the verify operation is skipped are performed when a pass/fail determination of the program operation in the N-th program loop indicates a pass.

FIG. 1