CLAIMS

What is claimed is

1. A device, comprising:

a substrate, wherein the substrate comprises a silicon fin;

a pair of gate spacers on the substrate, wherein the gate spacers comprise a dielectric material;

a gate dielectric layer formed to abut the silicon fin, wherein the gate dielectric layer is formed from high-k dielectric materials;

an NMOS metal gate electrode disposed above the gate dielectric layer and between the pair of gate spacers, wherein the NMOS metal gate electrode comprises:

a first metal layer conformally deposited adjacent the pair of gate spacers and above the gate dielectric layer, wherein the first metal layer is formed from a material comprising a composition including aluminum, titanium and carbon;

a second metal layer conformally deposited on the first metal layer, wherein the second metal layer is formed from a material selected from a group including titanium nitride;

a source region proximate to one of the pair of gate spacers, and a drain region proximate the other one of the pair of gate spacers, wherein the source region and the drain region comprise an n-type dopant;

a first contact coupled to the source region, wherein the first contact comprises a tungsten material above a first barrier layer; and

a second contact coupled to the drain region, wherein the second contact comprises a tungsten material above a second barrier layer,

wherein a portion of the NMOS metal gate electrode is removed to form a recess and a recessed transistor gate, wherein the recessed transistor gate is recessed between the pair of gate spacers, and wherein there is a capping dielectric structure on the recessed transistor gate and between the pair of gate spacers.

2. The device of claim 1, wherein the NMOS metal gate electrode is non-planar.

3. The device of claim 1, wherein the NMOS metal gate electrode comprises between 20 percent by weight to 40 percent by weight aluminum, between 30 weight percent to 50 weight percent titanium, and between 10 weight percent to 30 weight percent carbon.

4. The device of claim 1, wherein the NIMOS metal gate electrode further comprises a tungsten-containing gate fill material adjacent the second metal layer, wherein the first metal layer, second metal layer and the tungsten-containing gate fill material have a flush surface between the gate spacers.

5. The device of claim 1, wherein the first metal layer comprises a work function layer.

6. The device of claim 1, wherein the second metal layer comprises a barrier layer.

7. The transistor gate of claim 3, wherein the NMOS metal gate electrode comprises between about 33% by weight aluminum, between about 43% by weight titanium, and between about 24% by weight carbon.

8. A device, comprising:

a substrate, wherein the substrate comprises a silicon fin;

a pair of gate spacers on the substrate, wherein the gate spacers comprise a dielectric material;

a gate dielectric layer formed to abut the silicon fin, wherein the gate dielectric layer is formed from high-k dielectric materials;

an NMOS metal gate electrode disposed above the gate dielectric layer and between the pair of gate spacers, wherein the NMOS metal gate electrode comprises:

a workfunction metal layer conformally deposited adjacent the pair of gate spacers and above the gate dielectric layer, wherein the workfunction metal layer comprises aluminum, titanium and carbon;

a first metal layer conformally deposited on the workfunction metal layer, wherein the first metal layer comprises titanium and nitrogen; and

a second metal layer on the first metal layer, wherein the second metal layer comprises tungsten;

a source region proximate to one of the pair of gate spacers, and a drain region proximate the other one of the pair of gate spacers, wherein the source region and the drain region comprise an n-type dopant;

a first contact coupled to the source region, wherein the first contact comprises a tungsten material above a first barrier layer; and

a second contact coupled to the drain region, wherein the second contact comprises a tungsten material above a second barrier layer,

wherein a portion of the NMOS metal gate electrode is removed to form a recess and a recessed transistor gate, wherein the recessed transistor gate is recessed between the pair of gate spacers and wherein there is a capping dielectric structure on the recessed transistor gate and between the pair of gate spacers.

9. The device of claim 8, wherein the NMOS metal gate electrode is non-planar.

10. The device of claim 8, wherein the wherein the workfunction metal layer, the first metal layer and the second metal layer have a flush surface between the gate spacers.

11. The device of claim 8, wherein the first metal layer comprises a barrier layer.

12. The device of claim 8, wherein the second metal layer comprises a fill layer.

13. An assembly, comprising:

a plurality of transistors, each transistor comprising:

a substrate, wherein the substrate comprises a silicon fin;

a pair of gate spacers on the substrate, wherein the gate spacers comprise a dielectric material;

a gate dielectric layer formed to abut the silicon fin, wherein the gate dielectric layer is formed from high-k dielectric materials;

a NMOS metal gate electrode disposed above the gate dielectric layer and between the pair of gate spacers, wherein the NMOS metal gate electrode comprises:

a work function layer conformally adjacent the pair of gate spacers and above the gate dielectric layer, wherein the work function layer comprises aluminum, titanium and carbon;

a barrier layer conformally deposited on the work function layer,

wherein the barrier layer comprises titanium and nitrogen;

a source region proximate to one of the pair of gate spacers, and a drain region proximate the other one of the pair of gate spacers, wherein the source region and the drain region comprise an n-type dopant;

a first contact coupled to the source region, wherein the first contact comprises a tungsten material above a first barrier layer;

a second contact coupled to the drain region, wherein the second contact comprises a tungsten material above a second barrier layer; and

wherein a portion of the NMOS metal gate electrode is removed to form a recess and a recessed transistor gate, wherein the recessed transistor gate is recessed between the pair of gate spacers and wherein there is a capping dielectric structure on the recessed transistor gate and between the pair of gate spacers.

14. The assembly of claim 13, wherein the assembly comprises a portion of an integrated circuit.

15. A method of fabricating a transistor gate, comprising:

forming a pair of gate spacers;

forming a gate electrode disposed between the pair of gate spacers comprising

conformally depositing a NMOS work function material adjacent the pair of gate spacers, the MOS work function material comprises aluminum, titanium and carbon;

conformally depositing a titanium-containing gate fill barrier adjacent the NMOS work-function material; and

depositing a tungsten-containing gate fill material adjacent the gate fill barrier;

forming a recess between the gate spacers by removing a portion of the gate electrode; and

in the recess, forming a capping dielectric structure over the gate electrode.