potential difference between the memory gate electrode MG and the fin S2.

[0121] Thus, when the memory cell MC is downsized by reducing the distance between the drain region 12a and the source region 12b on the surface of the fin S2 with a high impurity concentration inside the fin S2, the potential difference between the memory gate electrode MG and the fin S2 can be reduced by setting the shape (height and width) of the fin S2 so that a depleted layer is formed entirely inside the fin S2, and the occurrence of disturbance can be suppressed by reducing electric field applied to the depleted layer. Accordingly, the memory cell MC achieves downsizing and suppression of the occurrence of disturbance.

[0122] The gate widths of the memory gate structure 2, the first select gate structure 3, and the second select gate structure 4 extend in C shapes along both side surfaces and the surface of the fin S2 such that the height of the fin S2 serves as part of the gate widths. The configuration leads to height increase by the height of the fin S2 but also leads to reduction of the formation area of each gate width in the x direction in which the memory gate structure 2, the first select gate structure 3, and the second select gate structure 4 extend over the fin S2, thereby achieving downsizing accordingly.

[0123] When no data is to be programmed to the memory cell MC, voltage applied to the bit line BL and the source line SL is not restricted to a high charge storage gate voltage applied to the memory gate electrode MG but can be reduced to voltage for achieving a non-conductive state inside the fin S2 directly below the first select gate structure 3 and the second select gate structure 4. Thus, the thicknesses of the first select gate insulating films 17a and 18a of the first select gate structure 3

operations in nonvolatile semiconductor storage device" are applicable.

[0149] In the memory cell MC illustrated in FIGS. 3A and 3B, the first select gate insulating films 17a and 18a are in a two-layer structure, and the second select gate insulating films 17b and 18b are in a two-layer structure, but the present invention is not limited thereto. A one-layer structure including one of the first select gate insulating films 17a and 18a and a one-layer structure including one of the second select gate insulating films 17b and 18b are applicable.

[0150] In the above-described embodiments, the memory gate sidewall insulating films 15a and 15b are provided along the sidewalls of the memory gate electrode MG (FIGS. 3A and 3B), but the present invention is not limited thereto. Any one of the memory gate sidewall insulating films 15a and 15b may be provided along one of the sidewalls of the memory gate electrode, or none of the memory gate sidewall insulating films 15a and 15b may be provided to the memory gate electrode.

[0151] In the above-described embodiments, the first select gate sidewall insulating film 19a and the sidewall-part sidewall insulating film 20a are provided along the sidewalls of the first select gate electrode DG (FIGS. 3A and 3B), but the present invention is not limited thereto. Any one of the first select gate sidewall insulating film 19a and the sidewall-part sidewall insulating film 20a may be provided along one of the sidewalls of the first select gate electrode, or none of the first select gate sidewall insulating film 19a and the sidewall-part sidewall insulating film 20a may be provided to the first select gate electrode.

[0152] In the above-described embodiments, the second select gate sidewall insulating film 19b and the sidewall-part sidewall insulating film 20b are provided

When data programming is prevented by preventing charge injection into the charge storage layer EC in the memory cell MC3 having the above-described configuration according to the present embodiment, similarly to the above-described embodiments, a depleted layer is formed entirely inside the fin S2 surrounded by the memory gate structure 2 to reduce the potential difference between the memory gate electrode MG and the fin S2. Thus, when the memory cell MC3 is downsized by reducing the distance between the drain region 12a and the source region 12b on the surface of the fin S2 with a high impurity concentration inside the fin S2, the potential difference between the memory gate electrode MG and the fin S2 can be reduced by setting the shape (height and width) of the fin S2 so that a depleted layer is formed entirely inside the fin S2, and the occurrence of disturbance can be suppressed by reducing electric field applied to the depleted layer. Accordingly, the memory cell MC3 achieves downsizing and suppression of the occurrence of disturbance.

[0174] In addition, the memory cell MC3 includes the insulating layer IS1 with which the distance H4 between the semiconductor substrate S1 and the lower surface of the lower memory gate insulating film 13 is larger than the distance H5 between the semiconductor substrate S1 and the lower surfaces of the first and second select gate insulating films 17a and 17b. With the configuration, the lower surfaces of the first and second select gate electrodes DG and SG are positioned closer to the semiconductor substrate S1 than the lower surface of the memory gate electrode MG in a region in which the insulating layer IS1 is provided.

[0175] In the memory cell MC3 thus configured, the first and second select transistors T1 and T2 in the regions on the side surfaces of the fin S2 can be more reliably

embodiment, the lower insulating layer 53) on the upper and lower surfaces thereof, the memory transistor MT is a fully-depleted transistor. In the present embodiment, the relation of H1fin > Wfin holds where H1fin represents the height of the fin S3.

[0185] In the present embodiment, as illustrated in FIG. 21A, a distance H7 between the semiconductor substrate S1 and the lower surface of the fin S3 is set to be larger than the distance H1 between the semiconductor substrate S1 and the lower surface of the memory gate electrode MG in the region in which the fin S3 is not provided. Accordingly, the lower surface of the memory gate electrode is positioned lower than the lower surface of the fin S3 so that the memory gate electrode MG completely covers the side surfaces of the fin S3. The configuration prevents leakage current, which would otherwise cause a false operation, from flowing between the drain region 12a and the source region 12b along regions on the side surfaces of the fin S3.

[0186] The distance H7 between the semiconductor substrate S1 and the lower surface of the fin S3 desirably differs from the distance H1 between the semiconductor substrate S1 and the lower surface of the memory gate electrode MG by an half or more of the width Wfin of the fin S3. A configuration in which the lower insulating layer 53 is not provided will be described later.

[0187] FIG. 21B, in which any corresponding part to that in FIG. 4B is denoted by an identical reference sign, is a cross-sectional view illustrating a sectional configuration taken along line D-D' in FIG. 19. The fin S3 is sandwiched between the upper insulating layer 54 and the insulating layer IS2 (in the present embodiment, the lower insulating layer 53) on the upper and lower surfaces thereof and surrounded by the first select gate

[0191] The same above description of "(3) Circuit configuration of nonvolatile semiconductor storage device" and "(4) Voltage at various operations in nonvolatile semiconductor storage device" applies to the memory cell MC4 according to the present embodiment, and thus is not given in the following.

[0192] The memory cell MC4 including the fin S3 on the insulating layer IS1 may be manufactured by sequentially stacking a semiconductor substrate, an insulating layer, a semiconductor layer to be formed into a fin, and an insulating layer to be formed into an upper insulating layer, before the fin formation process illustrated in FIG. 8, and then fabricating, in the fin formation process, parts of the semiconductor layer to be formed into a fin and the insulating layer by using, as a hard mask, the patterned insulating layer to be formed into an upper insulating layer. Alternatively, a silicon-on-insulator (SOI) substrate may be used as the semiconductor substrate, the insulating layer, and the semiconductor layer to be formed into a fin.

[0193] (10-2) Operations and effects

When data programming is prevented by preventing charge injection into the charge storage layer EC in the memory cell MC4 having the above-described configuration, the occurrence of disturbance can be suppressed according to a principle same as that in the above-described embodiments by reducing the potential difference between the memory gate electrode MG and the fin S3 and reducing electric field applied to a depleted layer. Accordingly, the memory cell MC 4 achieves downsizing and suppression of the occurrence of disturbance.

[0194] In addition, the memory transistor MT, the first select transistor T1, and the second select transistor T2 of the memory cell MC4 can operate as fully-depleted transistors since the fin S3 is sandwiched between the

between the semiconductor substrate S1 and the lower surface of the memory gate electrode MG in the region in which the fin S3 is not provided (H7 > H1), but the present invention is not limited thereto. The distance H7 between the semiconductor substrate S1 and the lower surface of the fin S3 may be equal to or smaller than the distance H1 between the semiconductor substrate S1 and the lower surface of the memory gate electrode MG in the region in which the fin S3 is not provided (H7 ≤ H1).

[0198] For example, when the lower insulating layer 53 is provided on the layered insulating layer 52, the distance H7 between the semiconductor substrate S1 and the lower surface of the fin S3 may be larger than the distance H5 between the semiconductor substrate S1 and the surface of the layered insulating layer 52 and smaller than the distance H1 between the semiconductor substrate S1 and the lower surface of the memory gate electrode MG illustrated in FIG. 21A (H5 < H7 < H1).

[0199] In the above-described embodiments, the lower insulating layer 53 protruding from the layered insulating layer 52 is provided on the layered insulating layer 52, and the layered insulating layer 52, the lower insulating layer 53, the fin S3, and the upper insulating layer 54 are stacked in this order on the semiconductor substrate S1, but the present invention is not limited thereto. The layered insulating layer 52, the fin S3, and the upper insulating layer 54 may be stacked in this order on the semiconductor substrate S1 without the lower insulating layer 53. In this case, the lower surface of the fin S3 may be positioned flush with the surface of the layered insulating layer 52.

[0200] In the above-described embodiments, the upper insulating layer 54 is provided on the fin S3, and the insulating layer IS2, the fin S3, and the upper insulating layer 54 are stacked in this order on the

Claims

1. A memory cell comprising:

a semiconductor substrate covered by an insulating layer;

a fin disposed on the semiconductor substrate and protruding from the insulating layer;

a memory gate structure including a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a memory gate electrode stacked, and being disposed on the insulating layer so as to extend over the fin;

a first select gate structure including a first select gate electrode stacked on a first select gate insulating film, and being disposed on the insulating layer so as to extend over the fin along a first sidewall spacer disposed on one sidewall of the memory gate structure;

a second select gate structure including a second select gate electrode stacked on a second select gate insulating film, and being disposed on the insulating layer so as to extend over the fin along a second sidewall spacer disposed on the other sidewall of the memory gate structure;

a drain region provided adjacent to the first select gate structure on a surface of the fin, insulated from the first select gate electrode, and electrically connected with a bit line; and

a source region provided adjacent to the second select gate structure on the surface of the fin, insulated from the second select gate electrode, and electrically connected with a source line, wherein

the first select gate structure, the memory gate structure, and the second select gate structure are

provided between the drain region and the source region, and

in the insulating layer:

a distance between the semiconductor substrate and a lower surface of the lower memory gate insulating film is longer than distances between the semiconductor substrate and lower surfaces of the first select gate insulating film and the second select gate insulating film; and

positions of the lower surfaces of the first select gate electrode and the second select gate electrode with respect to the semiconductor substrate are closer than the lower surface of the memory gate electrode with respect to the semiconductor substrate.

2. The memory cell according to claim 1, wherein the insulating layer includes:

a layered insulating layer provided on the semiconductor substrate, and

a convex portion insulating layer provided in a region in which the memory gate structure is provided on the layered insulating layer.

3. The memory cell according to claim 2, wherein the convex portion insulating layer has a thickness equal to or larger than a half of a width of the fin in a direction in which the memory gate structure, the first select gate structure, and the second select gate structure extend over the fin.

4. A memory cell comprising:

a semiconductor substrate covered by an insulating layer;

a fin disposed on the insulating layer;

a memory gate structure including a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a memory gate electrode stacked, and being disposed on the insulating layer so as to extend over the fin;

a first select gate structure including a first select gate electrode stacked on a first select gate insulating film, and being disposed on the insulating layer so as to extend over the fin along a first sidewall spacer disposed on one sidewall of the memory gate structure;

a second select gate structure including a second select gate electrode stacked on a second select gate insulating film, and being disposed on the insulating layer so as to extend over the fin along a second sidewall spacer disposed on the other sidewall of the memory gate structure;

a drain region provided adjacent to the first select gate structure on a surface of the fin, insulated from the first select gate electrode, and electrically connected with a bit line; and

a source region provided adjacent to the second select gate structure on the surface of the fin, insulated from the second select gate electrode, and electrically connected with a source line, wherein

the first select gate structure, the memory gate structure, and the second select gate structure are provided between the drain region and the source region,

an upper insulating layer is provided on an upper surface of the fin in a region where the memory gate structure, the first sidewall spacer, the first select gate structure, the second sidewall spacer, and the second select gate structure are provided , and

the insulating layer includes:

a layered insulating layer provided on the semiconductor substrate; and

a lower insulating layer that is provided on the layered insulating layer, made of a material same as a material of the layered insulating layer, and integrated with the layered insulating layer, and on a surface of which the fin is provided, and the layered insulating layer, the lower insulating layer, the fin, and the upper insulating layer are stacked in this order on the semiconductor substrate.

5. The memory cell according to claim 4, wherein a lower surface of the fin is positioned higher than a lower surface of the memory gate electrode in a region in which the fin is not provided.

6. A nonvolatile semiconductor storage device comprising a plurality of memory cells arranged in a matrix of rows and columns and each including a memory gate electrode connected with a memory gate line, wherein each memory cell is the memory cell according to any one of claims 1 to 5, and the memory gate line is shared by the memory cells arranged in the matrix.