Description

Field of the Invention

The present invention relates to a CPU (Central Processing Unit) core suitable for use in a single-chip microcomputer and which is operable at high speed and small in chip size.

Description of the Prior Art

In the field of the art to which the present invention pertains, elaborate technologies have been reported by Yamada et al in "8-Bit Flexible Microcontroller", the Institute of Electronics and Communication Engineers of Japan, Materials for Study Meeting, SSD86-92, pp. 7-12, 1986 (hereinafter referred to as document 1), and also reported in "Opening of CPU Core ASIC Age", Nikkei Microdevices, No. 1989-1, pp. 35-43, BP Company (hereinafter referred to as document 2).

There is an increasing demand for a single-chip microcomputer which allows peripheral circuits matching particular applications to be built therein without consuming a long time for development. To meet such a demand, the document 1 proposes a core device in the form of a CPU core to which desired peripheral circuits may be interconnected according to the user's needs. This kind of single-chip microcomputer or so-called ASIC microcomputer chip will have optimum specifications matching a desired application.

A CPU core intended for the above purpose has to adapt itself to various kinds of applications. Hence, prerequisites with such a CPU core are, among others, rapid operation processing, extended design freedom, ease of connection of peripheral circuits, small exclusive area, a broad operable range (voltage, temperature and so forth). The document 1 teaches a CPU core made up of various blocks such as a CPU block, interrupt control block, an input/output control block, and a RAM, and configured to execute instruction processing by sixteen bits for the purpose of promoting high-speed operations.

However, a CPU core having the above configuration has some problems left unsolved. Namely, increasing the processing speed and reducing the exclusive area for a CPU core are contradictory to each other. Fetching an instruction from a ROM, executing pipeline processing, and providing the processing system with a 16-bit width as disclosed in the document 1 are typical approaches available for enhancing high-speed operations. However, all of such approaches would complicate the hardware of an 8-bit microcomputer and would increase the exclusive area for the CPU core due to the increase in processing speed.

The prior art CPU core includes RAMs, clock generators, and various control circuits therein and is satisfactory so long as a desired application can be implemented by the specifications of such built-in components. However, when the specifications cannot meet the user's demand, e.g., when the number of RAMS should be increased or decreased or when the specifications of the control circuits should be changed, it is necessary to redesign the portions of the CPU core where the specifications should be changed and to adequately distribute the functions to the CPU core and the peripheral circuits to be connected to the CPU core. This kind of CPU core, therefore, is not fully satisfactory when it comes to the ease of connection of peripheral circuits and the design freedom available for the peripheral circuits (ELECTRONIQUE APPLICATIONS, No. 50, October-November 1986, pages 71-77, Paris, FR; R. KANNENBERG: "La programmation de microprocesseurs personnalisés").

Hence, the configuration of a CPU core has decisive influence on the design freedome of peripheral circuits and the chip size. When a CPU core has a great number of components, the user-oriented selectable range of specifications is extremely limited and the chip size is increased. The resultant CPU core would be contrary to the intention, i.e., a broad range of applications. If the number of components of a CPU is relatively small, the design freedom of peripheral circuits will be enhanced and the chip-size will be reduced. Such a CPU, however, would increase the user's burden concerning the design of peripheral circuits and would require manifold know-hows on CPUs for the connection of peripheral circuits to the CPU core. This impedes the reduction of developing time which is the object of an ASIC microcomputer. Thus, a CPU core for an ASIC microcomputer which allows various kinds of peripheral circuits to be efficiently and easily connected thereto, i. e. , which has ample design freedom has not been reported yet.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a CPU core which is operable at high speed and occupies a minimum of exclusive area, enhances the design freedom of peripheral circuits, and promotes the ease of connection with peripheral circuits.

A CPU core of the present invention as claimed in claim 1 includes an internal resource made up of various kinds of registers, and a controller a bus control circuit which controls the input and output of data and others among various kinds of buses. A terminal group has a plurality of terminals for interconnecting the CPU core to a peripheral circuit and an external memory. The buses comprise an internal bus to which individual circuits incorporated in the CPU core are interconnected, a data bus interconnected between the CPU core and the external memory for allowing data to be inputted and outputted between the CPU core and the external memory, and a peripheral data bus interconnected between the CPU core and the peripheral circuit for allowing data to be inputted and outputted between the CPU core and the peripheral circuit. The input and output terminals of all of the circuit portions constituting the internal resource

are interconnected to the internal bus. The bus control circuit has input and output terminals interconnected to the internal bus, data bus, and peripheral data bus for controlling the input and output of data and others among the buses and comprises first control means for controlling input and output of data between said internal bus and said data bus and second control means for controlling input and output of data between said internal bus and said peripheral data bus.

The present invention enhances efficient manipulation of peripheral circuits, reduces the chip size, and allows desired peripheral circuits to be designed with greater freedom than the prior art.

In accordance with the present invention, the bus control circuit eliminates the problem particular to a CPU having a single bus structure as will be described, speeds up processing, and reduces chip size.

Further as claimed in claim 5, the bus control circuit precharges the peripheral data bus prior to the input of data from the peripheral data bus, whereby the individual peripheral circuits are desirably scaled down and the data interchange is sped up.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the present invention will become more apparent from the consideration of the following detailed description taken in conjunction with the accompanying drawings in which:

FIGS. 1A and 1B are block diagrams schematically showing a CPU core embodying the present invention;

FIG. 2 is a timing chart demonstrating a specific operation of the CPU core of FIGS. 1A and 1B for executing an instruction;

FIG. 3 is a block diagram schematically showing a specific construction of a bus control circuit included in the CPU core of FIG. 1 and an arrangement associated therewith;

FIG. 4 is a timing chart representative of a procedure for interconnecting the bus control circuit of FIG. 3 and an external memory;

FIG. 5 is a timing chart representative of a procedure for interconnecting the bus control circuit of FIG. 3 and a peripheral circuit;

FIG. 6 is a diagram showing in detail a connection part between an internal bus included in the bus control circuit of FIG. 3 and a peripheral data bus; and

FIGS. 7A and 7B are diagrams each schematically showing a particular construction of the peripheral circuit shown in FIG. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIGS. 1A and 1B of the drawings, a CPU core embodying the present invention is shown. As shown, the CPU core has an internal resource 10 having registers which are interconnected to a single internal bus 11 in a so-called single bus configuration. A controller 20 supervises the entire CPU core by decoding instructions and delivering various kinds of control signals. The controller 20 interchanges signals with the outside of the CPU core.

The internal resource 10 has an accumulator (ACC) 12 for storing the results of arithmetic and logical operations, a B register 12 which is a general-purpose working register, a stack pointer 14 for pointing a location of a stack memory or similar storage from which data should be read out, a condition code register 15, an arithmetic and logic unit (ALU) 16 for performing arithmetic and logic operations, an upper program counter 17H and a lower program counter 17L for memorizing the location of an instruction which should be read out next, etc. All these components of the internal resource 10 are interconnected to the internal bus 11.

The controller 20 has temporary registers 21X and 21Y each for temporarily storing data, an instruction register 22 for temporarily storing an instruction, an instruction decoder 23 for decoding an instruction lodged in the instruction register 22 to generate various kinds of control signals, a timing control circuit 24, a peripheral address latch 25 for latching a peripheral address (address of a peripheral circuit), an upper external memory address latch 26H and a lower external memory address latch 26L for latching an address of an external memory, and a bus control circuit 27.

The timing control circuit 24 is operated by a reset signal RES and a clock signal CLK which are fed thereto from the outside and, in turn, generates timing signals ø1 to ø4 which are necessary the execution of instructions and other various control timing signals meant for various sections of the CPU core. Further, the timing control circuit 24 delivers to the outside a synchronizing signal SYNC which is a timing signal for causing a peripheral circuit or similar circuit into connection with the CPU core, a clock output signal CLKOUT, an input timing signal $\overline{RD}$, an output timing signal $\overline{WR}$, an input timing signal $\overline{PRD}$ assigned to peripheral data, an output timing signal $\overline{PWR}$ also assigned to peripheral data, etc. The bus control circuit 27 is interconnected between the internal bus 11 and a data bus DB and a peripheral data bus PDB so as to control the input and output of data thereto.

The terminal group 30 has terminals 31-1 and 31-2 to which the reset signal RES and clock signal CLK are respectively applied as control inputs, and terminals 32-1 to 32-6 from which the clock output signal CLKOUT, synchronizing signal SYNC, input timing signal $\overline{RD}$, output timing signal $\overline{WR}$, peripheral input timing signal $\overline{PRD}$, and peripheral output timing signal $\overline{PWR}$ are fed out as timing outputs. The terminal group 30 also has an output terminal assigned to the address bus AB, an input and an output terminal assigned to the data bus DB, an output terminal assigned to a peripheral address bus PAB,

and an input and an output terminal assigned to a peripheral data bus PDB, all of which are collectively represented by a single block in FIG. 1B and adapted for the connection with the outside.

The operation of the CPU core having the above construction will be described with reference to FIG. 2 and by taking the execution of a relatively simple addition instruction as an example.

In FIG. 2, successive instruction processing cycles I1, I2 and so forth each is constituted by four successive timing states S1 to S4 which occur in synchronism with the basic timing signals ø1 to ø4, respectively. In the timing state S4 of the instruction processing cycle which immediately precedes the cycle I1 and the timing states S1 and S2 of the cycle I1, an instruction is fetched from an external memory, not shown, to the instruction register 22 via the data bus DB, bus control circuit 27, and internal bus 11. The address of the external memory is indicated by the program counters 17H and 17L and fed to the external memory over the address bus AB.

The instruction decoder 23 decodes the instruction and, based on the result of decoding, generates control timing signals meant for various sections of the CPU core. Then, processing conforming to the instruction is executed in response to such control timing signals in the timing states S3 and S4 of the instruction processing cycle I1 and the timing state S3 of the following instruction processing cycle I2. The basic timing signals ø1 to ø4 which the instruction decoder 23 needs are fed from the timing control circuit 24.

In the event of the execution of an addition instruction, the instruction is fetched and decoded as stated earlier in the timing state S4 of the instruction processing cycle immediately preceding the cycle I1 and the timing states S1 and S2 of the cycle I1. During the period of time Ta allocated to the timing state S3 of the instruction processing cycle I1, data from a peripheral circuit, not shown, which is interconnected to the outside of the CPU core is loaded in one temporary register 21Y via the peripheral data bus PDB, bus control circuit 27, and internal bus 11. Assume that one of two different data to be added together has already been loaded in the other temporary register 21X by the execution of an instruction prior to the execution of the addition instruction.

During the period of time Tc of the timing states S3 and S4 of the instruction processing cycle I1, the ALU 16 adds the data stored in the temporary registers 21Y and 21X. During a period of time Tb of the timing states S4 and S1 of the instruction processing cycles I1 and I2, respectively, the result of addition is outputted to the peripheral data bus PDB via the internal bus 11 and bus control circuit 27. The condition code register 15 preserves the condition of the CPU which has executed the addition instruction as stated above.

The peripheral address latch 25 indicates an address of the peripheral circuit, not shown, and this address is fed to the peripheral circuit by way of the peripheral address bus PAB.

An addition instruction is executed as outlined above. When the objects of operation exist within the internal resource 10 having the accumulator 12, B register 13, stack pointer 14 and so forth, the instruction decoder 23 delivers control signals such that data stored in registers of interest of the internal resource 10 are read out and fed to the internal bus 11, instead of data being fetched via the peripheral data bus PDB. Then, instruction processing cycles will be executed in the same manner as with the addition instruction.

With the illustrative embodiment, therefore, external peripheral circuits interconnected to the peripheral data bus PDB can be dealt with in the same manner as the internal resource 10 with respect to timing. This is successful in enhancing the efficient manipulation of peripheral circuits. Moreover, an oscillation circuit, a CPU control circuit for executing stops, halts and other similar power-down control, a ROM, a RAM, an interruption circuit and other various kinds of cicuitry are connectable to the CPU core as peripheral circuits. Hence, peripheral circuits can be designed to meet particular market needs, whereby design freedom is enhanced.

Generally, while a CPU having a single bus structure promotes the reduction of chip size and the ease of pattern layout, the execution of an instruction with such a CPU involves a period during which the fetching of an instruction and the execution of an instruction fetched previously overlap each other (e. g. a period of time Tb extending over successive timing stages S4 and S1 as shown in FIG. 2. To eliminate this undesirable period, either one of the fetching of an instruction and the execution of the previous instruction has to be delayed at the sacrifice of processing rate. In the light of this, the bus control circuit 27 of the illustrative embodiment has a unique construction as shown in FIG. 3.

FIG. 3 shows a specific construction of the bus control circuit 27 of the CPU core of FIG. 1 and an arrangement associated therewith. In the CPU core shown in FIG. 3, the individual registers and other elements included in the internal resource 10 each is interconnected to the 8-bit internal bus 11 via respective one of a plurality of output drivers 18 which are controlled by the basic timing signal ø4. The output of the peripheral address latch 25 interconnected to the internal bus 11 is interconnected to the 8-bit peripheral address bus PAB via an output driver 28. The outputs of the program counters 17H and 17L or the outputs of the external memory address latch circuits 26H and 26L are interconnected to the address bus AB via an output buffer 19, depending on the kind of instruction to be executed.

The bus control circuit 27 is made up of a peripheral data bus control section 27A for controlling the interchange of data between the internal bus 11 and the peripheral data bus PDB, and a data bus control section 27B for controlling the interchange of data and others between the internal bus 11 and the data bus DB. The peripheral data bus control section 27A has an output latch 40 for latching data to be fed out from the internal

bus 11 to the peripheral data bus PDB, an output driver 41 for controlling the output timing of data having been latched in the output latch 40, and an input driver 42 for controlling the input timing of data to be applied from the peripheral data bus PDB to the internal bus 11. The data bus control section 27B has an output latch 50 for latching data and others to be fed out from the internal bus 11 to the data bus DB, an output driver 51 for controlling the output timing of data and others having been latched by the output latch 50, and an input driver 52 for controlling the input timing of data and others to be fed from the data bus DB to the internal bus 11.

The output latch 40 latches output data in response to an output timing signal PWR·T4 associated with the timing state T4, while the output latch 50 latches output data in response to a clock signal T4·CLK associated with the state T4. The output drivers 41 and 51 are operated by an input timing signal $\overline{PRD}$ and a data output signal VLW, respectively. The input drivers 42 and 52 are respectively operated by an input timing signal PRD·T3 associated with the timing state T3 and an input timing signal RD·T1 associated with the state T1.

At the outside of the CPU core, a plurality of peripheral circuits 60 each is interconnected to the peripheral data bus PDB via a bus driver, not shown. A plurality of external memories 61 each is also interconnected to the outside of the CPU core between the address bus AB and the data bus DB via a bus driver, not shown. An address decoder 62 decodes an address on the peripheral address bus PAB and feeds the decoded address to a terminal $\overline{CS}$ of each peripheral circuit 60, whereby one of the peripheral circuits 60 is selected. Each peripheral circuit 60 has a terminal $\overline{WR}$ interconnected to a signal line on which the peripheral data output timing signal $\overline{PWR}$ appears, a terminal $\overline{OE}$ interconnected to a signal line on which the peripheral data input timing signal appears, and eight terminals $I/\overline{O}$ interconnected to the peripheral data bus PDB via the bus driver.

An address decoder 63 decodes an address on the address bus AB and delivers the decoded address to the terminals $\overline{CS}$ of the individual external memories 61 so as to select one them which is designted by the decoded address. The external memories 61 each has a terminal ADDR interconnected to the address bus AB via the associated bus driver, a terminal $\overline{WR}$ interconnected to a signal line on which the output timing signal $\overline{WR}$ appears, a terminal $\overline{OE}$ interconnected to a signal line on which the input timing signal $\overline{RD}$ appears, and eight terminals $I/\overline{O}$ interconnected to the data bus DB via the associated bus driver.

The operation of the bus control circuit 27 shown in FIG. 3 will be described with reference to FIGS. 4 and 5. Specifically, FIG. 4 is a timing chart demonstrating the interconnection of the bus control circuit 27 and any one of the external memories 61, while FIG. 5 is a timing chart representative of the interconnection of the bus control circuit 27 and any one of the peripheral circuits 60. In these figures, there are shown machine cycles M1 and M2, timing states T1 to T4, a precharge timing signal Stp, and a peripheral address PAB.

As shown in FIG. 4, as the CPU core delivers an input timing signal $\overline{RD}$ to the terminal OE of particular one of the external memories 61 for fetching an instruction, an instruction is read out of the memory 61 of interest and then applied to the input driver 52 of the bus control circuit 27 via the data bus DB. It is noteworthy that the instruction being propagated through the data bus DB is prevented from conflicting with other data because the output driver 51 is held in a high impedance state by a data output signal VLW which is in (logical) "1" level. The instruction applied to the input drivcr 52 is fed to the internal bus 11 at a particular timing, i. e., in the timing state T1 of the machine cycle 2 which is smaller in signal width than thc input timing signal $\overline{RD}$, as shown in FIG. 4.

On the other hand, data on the internal bus 11 is delivered to the peripheral circuit 60 by the following procedure. Specifically, the data on the internal bus 11, i. e., the content of the internal resource 10 is latched in the output latch 40 via the output driver 18 in the timing state T4 of the machine cycle M1. Subsequently, as shown in FIG. 5, data existing in the period which extends from the state T4 of the machine cycle M1 to the state T1 of the next machine cycle M2 is fed out to the peripheral data bus PDB via the output driver 41 as valid data. Hence, when the CPU core feeds an output timing signal $\overline{PWR}$ to the terminal $\overline{WR}$ of the peripheral circuit 60, the data on the peripheral data bus PDB is written to the peripheral circuit 60.

With the circuit arrangement of FIG. 3, therefore, it is true that the fetching of an instruction and the execution of a previous instruction overlap each other, as viewed from the outside of the CPU core. Nevertheless, within the CPU core, output data and an instruction are fed to the internal bus 11 in the state T4 of the machine cycle M1 and in the state T1 of the machine cycle M2, respectively. This is successful in eliminating the problem of overlapping period particular to a CPU having a single bus structure as discussed previously.

Data on the internal bus 11 is delivered to the external memory 61 in the same manner as to the peripheral circuit 60. Specifically, as shown in FIG. 4, data of the internal resource 10 appearing on the internal bus 11 in the state T4 of the machine cycle M1 is latched in the output latch 50 by a signal T4·CLK which is outputted in the latter half of the state T4 of the machine cycle M1. The latched data is fed to the data bus DB by the output driver 51 which is operated by the data output signal VLW up to the state T2 of the next machine cycle M2. As a result, the data outputted to the data bus DB is written to the external memory 61 by the output timing signal $\overline{WR}$.

With the construction and timings of the bus control circuit 27 stated above, it is possible to overcome the drawback particular to a CPU having a single bus structure without lowering the instruction execution rate.

Another characteristic feature of the illustrative embodiment is as follows. The interchange of data between

the CPU core and any one of the peripheral circuits 60 has to be executed in the timing states S3 and S4, as shown in FIG. 2. Assuming that the clock signal CLK has a frequency of 10 megahertz, for example, then the timing states S3 and S4 last 100 nanoseconds. The exclusive area to be occupied by the various peripheral circuits 60 which are interconnected to the CPU core has to be reduced as far as possible because they will be built in a single-chip microcomputer in the event of quantity production. Specifically, a prerequisite with the interconnection of the CPU core and the peripheral circuits 60 is that not only high-speed data interchange but also minimum space requirement be achieved.

However, the response of the peripheral data bus PDB is sequentially slowed down with the increase in the number of peripheral circuits 60 interconnected thereto due to the load capacity of the circuits 60. Here, the words "load capacity" refer to the sum of the wiring capacities of buses interconnecting the peripheral circuits 60, the capacities of bus drivers and input gates of the peripheral circuits 60, etc. Especially, the bus drivers each being built in respective one of the peripheral circuits 60 are implemented by transistors which occupy a substantial area, in order to charge and discharge the peripheral data bus PDB at high speed. Such bus drivers, therefore, have a load capacity, or output capacity, which is great enough to influence the chip size.

Considering the above situation, the illustrative embodiment further includes a unique circuit which allows a peripheral circuit to connect itself to the CPU at high speed while occupying a minimum of exclusive area, as will be described with reference to FIG. 6. This circuit is built in the bus control circuit 27 to precharge the peripheral data bus PDB. While a precharging method has heretofore been extensively practiced with dynamic RAMs, for example, the illustrative embodiment effectively applies it to a peripheral bus in the configuration which will be described.

Fig. 6 is a diagram showing how the internal bus 11 and peripheral data bus PDB are interconnected in the bus control circuit 27, FIG. 3, in detail. FIGS. 7A and 7B are diagrams each showing a peripheral circuit 60, FIG. 3, having a different construction.

In the bus control circuit 27, the peripheral data bus section 27A interfaces the internal bus 11 and the 8-bit peripheral data bus PDB having bus lines PDB0 to PDB7. FIG. 6 shows a circuit portion of the peripheral data bus section 27A that interfaces a bus line 11-0 included in the internal bus 11 and the bus line PDB0 of the peripheral data bus PDB. As shown, the interfacing circuit portion has a NOR gate 43 having two inputs which are respectively interconnected to the output terminal Q of the output latch 40 and a control line 100 on which the precharge timing signal Stp appears. The output of the NOR gate 43 is interconnected to the input terminal D of the output latch 40 via the output driver 41 and input driver 42. Seven more such interfacing circuit portions are provided between the other bus lines 11-1 to 11-7 of the internal bus and the other bus lines PDB1 to PDB7 of the peripheral data bus PDB.

As shown in FIGS. 7A and 7B, a plurality of peripheral circuits 60 each having a particular construction are interconnected to the peripheral data bus PDB. Specifically, the peripheral circuit 60 of FIG. 7A has a peripheral body 60A and a bus driver 60B. The bus driver 60B has an inverter 70 which is interconnected to the terminal $\overline{OE}$ of the peripheral body 60A. P-channel MOS (PMOS) transistors 71 and 72 and n-channel MOS (NMOS) transistors 73 and 74 are interconnected in series to the terminal I/$\overline{O}$ of the peripheral body 60A and the output of the inverter 70 between the power source and ground. On the other hand, the peripheral circuit 60 of FIG. 7B has a bus driver 60B-1 which is comprised of NMOS transistors S73 and S74 only.

Referring again to FIG. 5, the operation of the circuitry shown in FIGS. 6, 7A and 7B will be described. To read data out of the peripheral circuit 60 of interest, the CPU core delivers an input timing signal $\overline{PRD}$ to the terminal $\overline{OE}$ of the peripheral circuit 60. Prior to the input timing signal $\overline{PRD}$, a precharge timing signal Stp is fed to the NOR gate 43 in the state T2 of the machine cycle M1. Then, output of the NOR gate 43 turns to (logical) "0" level and is inverted by the output driver 41 to "1" level. As a result, the output of the output driver 41 turns to "1" level and thereby precharges the bus line PDB0 of the peripheral data bus PDB0 to "1" level during a precharging period Tp.

As soon as the input timing signal $\overline{PRD}$ turns to "0" level after the bus line PDB0 has been precharged as stated above, data is read out of the peripheral circuit 60 and fed to the peripheral data section 27A via the bus line PDB0. In this instance, the input timing signal $\overline{PRD}$ is in "0" level and, therefore, the output driver 41 is in a high impedance state. Consequently, the data read out of the peripheral circuit 60 is fed to the internal bus 11-0 via the input buffer 42 in the timing state T3 of the machine cycle M1, without conflicting with other data.

As stated above, the precharging circuit built in the peripheral data bus section 27A and made up of the NOR gate 43 and output driver 41 allows a "1" level signal to be applied only to the peripheral data bus PDB while preventing the operating state of the internal bus 11 from being disturbed.

As shown in FIG. 7A, it has been customary to provide the bus driver 60B of the peripheral circuit 60 with the PMOS transistors 71 and 72 and inverter 70 for outputting a "1" level signal. In the illustrative embodiment, since a "1" level signal can be fed only to the peripheral data bus PDB due to the function of the unique precharging circuit, the PMOS transistors 71 and 72 and inverter 70 are not necessary as is the case with the bus driver 60B-1 of FIG. 7B. More specifically, the bus driver 60B-1 can be implemented only by the NMOS transistors S73 and S74. It follows that the NMOS transistors 73 and 74 do not have to be turned on when the "1" level signal is outputted, i. e., they are turned on only when the "0" level

signal is outputted. The precharging circuit, therefore, reduces the load capacity of and exclusive area for a bus to less than one half of the conventional bus driverr 60B.

The output timing signal $\overline{PRD}$, precharge timing signal Stp and other similar timing signals are easy to generate on the basis of the clock signal CLK and basic timing sinals ø1 to ø4 which are shown in FIG. 2.

In summary, in accordance with the present invention, a CPU core has at least an internal resource including registers, a controller for supervising the entire CPU core, and a terminal group having a plurality of terminals for interconnecting the CPU core to the outside. This, coupled with the fact that the internal resource interchanges data via an internal bus without exception, promotes efficient manipulation of peripheral circuits, reduction of the chip size, and peripheral circuit design matching manifold market needs.

A bus control circuit is interconnected between the internal bus and a data bus and a peripheral bus. When data is to be inputted to the CPU core, the width of a timing signal actually fed to the internal bus is selected to be smaller than the width of a timining signal adapted to input the data. On the other hand, when data is to be outputted, data on the internal bus is latched and then outputted. These in combination eliminate the problem particular to a CPU having a single bus structure and thereby implements rapid processing and the reduction of chip size. Further, before data to be outputted to the peripheral data bus is fetched, the peripheral data bus is precharged, and the output of the bus control circuit connected to the peripheral data bus is set up to a high impedance state in the event of the following input of the data. This desirably scales down the individual peripheral circuits and realizes the interchange of high-speed data.

The present invention, therefore, implements a CPU core which is small in chip size and has excellent peripheral circuit manipulability and unprecedented design freedom.

While the present invention has been described with reference to the particular illustrative embodiment, it is not to be restricted by the embodiment. It is to be appreciated that those skilled in the art can change or modify the embodiment without departing from the scope of the present invention. For example, registers or similar circuits may be added to the internal resource and control circuit 20 shown in FIG. 1. The terminals in the terminal group 30 may be partly omitted or may be combined with additional terminals, as desired.

Claims

1. A CPU core comprising :

   an internal resource (10) comprising plural kinds of registers;
   a control circuit (20) having a bus control circuit (27) for controlling input and output of data and others among plural kinds of buses (11, DB, PDB) ; and
   a terminal group (30) comprising a plurality of terminals (31-1~31-2, 32-1~32-6) for interconnecting said CPU core to a peripheral circuit (60) and an external memory (61) ;
   CHARACTERIZED IN THAT
   said plural kinds of buses (11, DP, PDB) comprising an internal bus (11) to which individual circuits incorporated in said CPU core are interconnected, a data bus (DB) interconnected between said CPU core and the external memory (61) for allowing data to be inputted and outputted between said CPU core and said external memory (61), and a peripheral data bus (PDB) inerconnected between said CPU core and the peripheral circuit (60) for allowing data to be inputted and outputted between said CPU core and said peripheral circuit (60) ;
   input terminals and output terminals of all of circuit portions which constitute said internal resource (10) being interconnected to said internal bus (11) ;
   said bus control circuit (17) having input terminals and output terminals interconnected to said internal bus (11), said data bus (DB), and said peripheral data bus (PDB) for controlling input and output of data and others among said buses (11, DB, PDB), and comprising
   first control means (27B) for controlling input and output of data between said internal bus (11) and said data bus (DB) ; and
   second control means (27A) for controlling input and output of data between said internal bus (11) and said peripheral data bus (PDB).

2. A CPU core in accordance with claim 1, CHARACTERIZED IN THAT said internal resource (10) comprises:

   an accumulator (12) for storing a result of operation;
   a general-purpose working register (13) ;
   a stack pointer (14) for pointing a location from which data is to be read out;
   program counters (17H, 17L) for storing a location on a memory where an instruction to be read out next is stored; and
   an arithmetic and logic unit (16) for executing arithmetic and logic operations;
   a control circuit (20) comprising :
   temporary registors (21X, 21Y) for temporarily storing data;
   an instruction register (22) for temporarily storing an instruction;
   an instruction decoder (23) for decoding an instruction stored in said instruction register (22)

signal is outputted. The precharging circuit, therefore, reduces the load capacity of and exclusive area for a bus to less than one half of the conventional bus driverr 60B.

The output timing signal $\overline{PRD}$, precharge timing signal Stp and other similar timing signals are easy to generate on the basis of the clock signal CLK and basic timing sinals ø1 to ø4 which are shown in FIG. 2.

In summary, in accordance with the present invention, a CPU core has at least an internal resource including registers, a controller for supervising the entire CPU core, and a terminal group having a plurality of terminals for interconnecting the CPU core to the outside. This, coupled with the fact that the internal resource interchanges data via an internal bus without exception, promotes efficient manipulation of peripheral circuits, reduction of the chip size, and peripheral circuit design matching manifold market needs.

A bus control circuit is interconnected between the internal bus and a data bus and a peripheral bus. When data is to be inputted to the CPU core, the width of a timing signal actually fed to the internal bus is selected to be smaller than the width of a timining signal adapted to input the data. On the other hand, when data is to be outputted, data on the internal bus is latched and then outputted. These in combination eliminate the problem particular to a CPU having a single bus structure and thereby implements rapid processing and the reduction of chip size. Further, before data to be outputted to the peripheral data bus is fetched, the peripheral data bus is precharged, and the output of the bus control circuit connected to the peripheral data bus is set up to a high impedance state in the event of the following input of the data. This desirably scales down the individual peripheral circuits and realizes the interchange of high-speed data.

The present invention, therefore, implements a CPU core which is small in chip size and has excellent peripheral circuit manipulability and unprecedented design freedom.

While the present invention has been described with reference to the particular illustrative embodiment, it is not to be restricted by the embodiment. It is to be appreciated that those skilled in the art can change or modify the embodiment without departing from the scope of the present invention. For example, registers or similar circuits may be added to the internal resource and control circuit 20 shown in FIG. 1. The terminals in the terminal group 30 may be partly omitted or may be combined with additional terminals, as desired.

Claims

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an internal resource (10) comprising plural kinds of registers;
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a terminal group (30) comprising a plurality of terminals (31-1~31-2, 32-1~32-6) for interconnecting said CPU core to a peripheral circuit (60) and an external memory (61) ;
CHARACTERIZED IN THAT
said plural kinds of buses (11, DP, PDB) comprising an internal bus (11) to which individual circuits incorporated in said CPU core are interconnected, a data bus (DB) interconnected between said CPU core and the external memory (61) for allowing data to be inputted and outputted between said CPU core and said external memory (61), and a peripheral data bus (PDB) inerconnected between said CPU core and the peripheral circuit (60) for allowing data to be inputted and outputted between said CPU core and said peripheral circuit (60) ;
input terminals and output terminals of all of circuit portions which constitute said internal resource (10) being interconnected to said internal bus (11) ;
said bus control circuit (17) having input terminals and output terminals interconnected to said internal bus (11), said data bus (DB), and said peripheral data bus (PDB) for controlling input and output of data and others among said buses (11, DB, PDB), and comprising
first control means (27B) for controlling input and output of data between said internal bus (11) and said data bus (DB) ; and
second control means (27A) for controlling input and output of data between said internal bus (11) and said peripheral data bus (PDB).

2. A CPU core in accordance with claim 1, CHARACTERIZED IN THAT said internal resource (10) comprises:

an accumulator (12) for storing a result of operation;
a general-purpose working register (13) ;
a stack pointer (14) for pointing a location from which data is to be read out;
program counters (17H, 17L) for storing a location on a memory where an instruction to be read out next is stored; and
an arithmetic and logic unit (16) for executing arithmetic and logic operations;
a control circuit (20) comprising :
temporary registors (21X, 21Y) for temporarily storing data;
an instruction register (22) for temporarily storing an instruction;
an instruction decoder (23) for decoding an instruction stored in said instruction register (22)

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to generate various control signals;
a timing control circuit (24) for generating timing signals necessary for operations of circuit portions;
a peripheral address latch (25) for latching a peripheral address which is an address of the peripheral circuit (60) ; and
external memory address latches (26H, 26L) for latching an external memory address which is an address of the external memory (61) ;
a terminal group (30) comprising:
an output terminal of an address bus (AB), an input and an output terminal of said data bus (DB), an input and an output terminal of a peripheral address bus (PAB) used to designate an address of the peripheral circuit (60), an input and an output terminal of said peripheral data bus (PDB), output terminals (32-1~32-6) assigned to timing signals which are generated by said timing control circuit (24), and input terminals (31-1, 31-2) assigned to control signals applied to said timing control circuit (24).

3. A CPU core in accordance with claim 2, CHARACTERIZED IN THAT

said first control means (27B) comprises :
a first output latch (50) for latching data to be outputted from said internal bus (11) to said data bus (DB) ;
a first output driver (51) for controlling an output timing of the data latched by said output latch (50) ; and
first input driver (52) for controlling an input timing of data to be inputted from said data bus (DB) to said internal bus (11) ; and in that
said second control means (27A) comprises :
a second output latch (40) for latching data to be outputted from said internal bus (11) to said peripheral data bus (PDB) ;
a second output driver (41) for controlling an output timing of data latched by said second output latch (40) ; and
a second input driver (42) for controlling an input timing of data to be inputted from said peripheral data bus (PDB) to said internal bus (11).

4. A CPU core in accordance with claim 3, CHARACTERIZED IN THAT said first control means (27B) is constructed such that when an instruction or data is to be inputted from said data bus (DB) to said internal bus (11), said timing control circuit (24) delivers to said first input driver (52) a signal having a smaller width than a timing signal which is used to input data from the outside via said data bus (DB) ;

said first control means (27B) being further constructed such that when data is to be outputted from said internal bus (11) to said data bus (DB), data outputted to said internal bus (11) is latched by said first output latch (50) and then outputted to said data bus (DB) via said first output driver (51).

5. A CPU core in accordance with claim 4, CHARACTERIZED IN THAT said second control means (27A) is constructed such that when data is to be inputted from said peripheral data bus (PDB) to said internal bus (11), said second output driver (41) delivers a logical "1" signal to said peripheral data bus (PDB) to precharge said peripheral data bus (PDB) prior to the input of said data, and then said second output driver (41) is turned to a high impedance state by a timing signal fed from said timing signal control circuit (24) so as to input said data from said peripheral data bus (PDB) to said internal bus (11) via said second input driver (42).

Patentansprüche

1. CPU-Kern, mit:

einem internen Betriebsmittel (10), das mehrere Arten von Registern enthält;
einer Steuerschaltung (20), die eine Bussteuerschaltung (27) zur Steuerung der Eingabe und Ausgabe von Daten und anderen von mehreren Arten von Bussen (11, DB, PDB) enthält; und
einer Anschlußgruppe (30), die mehrere Anschlüsse (31-1~31-2, 32-1~32-6) für den Anschluß des CPU-Kerns an eine Peripherieeinheit (60) und einen externen Speicher (61) enthält;
DADURCH GEKENNZEICHNET, DASS
die mehreren Arten von Bussen (11, DP, PDB) einen internen Bus (11), an den einzelne Schaltungen, die im CPU-Kern enthalten sind, angeschlossen sind, einen Datenbus (DB), der zwischen dem CPU-Kern und dem externen Speicher (61) angeschlossen ist und ermöglicht, Daten zwischen dem CPU-Kern und dem externen Speicher (61) einzugeben und auszugeben, sowie einen Peripheriedatenbus (PDB) enthalten, der zwischen dem CPU-Kern und der Peripherieschaltung (60) angeschlossen ist, um zu ermöglichen, Daten zwischen dem CPU-Kern und der Peripherieschaltung (60) einzugeben und auszugeben;
die Eingangsanschlüsse und Ausgangsanschlüsse sämtlicher Schaltungsabschnitte, die das interne Betriebsmittel (10) bilden, an den internen Bus (11) angeschlossen sind;
die Bus-Steuerschaltung (17) Eingangsanschlüsse und Ausgangsanschlüsse besitzt, die an den internen Bus (11), den Datenbus (DB) und den Peripheriedatenbus (PDB) angeschlossen sind, um die Eingabe und Ausgabe

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von Daten und anderem zwischen den Bussen (11, DB, PDB) zu steuern, und
dadurch, daß sie enthält:
eine erste Steuereinrichtung (27B) zum Steuern der Eingabe und Ausgabe von Daten zwischen dem internen Bus (11) und dem Datenbus (DB); und
eine zweite Steuereinrichtung (27A) zum Steuern der Eingabe und Ausgabe von Daten zwischen dem internen Bus (11) und dem Peripheriedatenbus (PDB).

2. CPU-Kern nach Anspruch 1, DADURCH GEKENNZEICHNET, DASS das interne Betriebsmittel (10) enthält:

einen Akkumulator (12) zum Speichern eines Operationsergebnisses;
ein Universalbetriebsregister (13);
einen Stapelzeiger (14), der einen Platz anzeigt, von dem Daten ausgelesen werden sollen;
Programmzähler (17H, 17L) zum Speichern eines Platzes in einem Speicher, an dem ein als nächstes auszulesender Befehl gespeichert ist; und
eine Arithmetik- und Logikeinheit (16) für die Ausführung von Arithmetik- und Logikoperationen;
eine Steuerschaltung (20), die enthält:
Pufferregister (21X, 21Y) zum vorübergehenden Speichern von Daten;
ein Befehlsregister (22) zum vorübergehenden Speichern eines Befehls;
einen Befehlsdecodierer (23) zum Decodieren eines im Befehlsregister (22) gespeicherten Befehls, um verschiedene Steuersignale zu erzeugen;
eine Zeitablauf-Steuerschaltung (24) zum Erzeugen von Zeitablaufsignalen, die für Operationen der Schaltungsabschnitte notwendig sind;
einen Peripherieadressen-Zwischenspeicher (25) zum Zwischenspeichern einer Peripherieadresse, die eine Adresse der Peripherieschaltung (60) ist; und
Externspeicheradressen-Zwischenspeicher (26H, 26L) zum Zwischenspeichern einer Externspeicheradresse, die eine Adresse des externen Speichers (61) ist;
eine Anschlußgruppe (30), die enthält:
einen Ausgangsanschluß eines Adreßbusses (AB), einen Eingangs- und einen Ausgangsanschluß des Datenbusses (DB), einen Eingangs- und einen Ausgangsanschluß eines Peripherieadressenbusses (PAB), der dazu verwendet wird, eine Adresse der Peripherieschaltung (60) zu bezeichnen, einen Eingangs- und einen Ausgangsanschluß des Peripheriedatenbusses (PDB), Ausgangsanschlüsse (32-1~32-6), die Zeitablaufsignalen zugeordnet sind, die durch die Zeitablauf-Steuerschaltung (24) erzeugt werden, und Eingangsanschlüsse (31-1, 31-2), die Steuersignalen zugeordnet sind, die an die Zeitablauf-Steuerschaltung (24) angelegt werden.

3. CPU-Kern nach Anspruch 2, DADURCH GEKENNZEICHNET, DASS

die erste Steuereinrichtung (27B) enthält:
einen ersten Ausgabe-Zwischenspeicher (50) zum Zwischenspeichern von Daten, die vom internen Bus (11) zum Datenbus (DB) ausgegeben werden sollen;
einen ersten Ausgabetreiber (51) zum Steuern eines Ausgabezeitverlaufs der vom Ausgangszwischenspeicher (50) zwischengespeicherten Daten; und
einen ersten Eingabetreiber (52) zum Steuern eines Eingabezeitverlaufs von Daten, die vom Datenbus (DB) in den internen Bus (11) eingegeben werden sollen; und dadurch, daß
die zweite Steuereinrichtung (27A) enthält:
einen zweiten Ausgabe-Zwischenspeicher (40) zum Zwischenspeichern von Daten, die vom internen Bus (11) zum Peripheriedatenbus (PDB) ausgegeben werden sollen;
einen zweiten Ausgabetreiber (41) zum Steuern eines Ausgabezeitverlaufs der Daten, die vom zweiten Ausgabe-Zwischenspeicher (40) zwischengespeichert werden; und
einen zweiten Eingabetreiber (42) zum Steuern eines Eingabezeitverlaufs der Daten, die vom Peripheriedatenbus (PDB) in den internen Bus (11) eingegeben werden sollen.

4. CPU-Kern nach Anspruch 3, DADURCH GEKENNZEICHNET, DASS die erste Steuereinrichtung (27D) in der Weise konstruiert ist, daß dann, wenn ein Befehl oder Daten vom Datenbus (DB) in den internen Bus (11) eingegeben werden sollen, die Zeitablauf-Steuerschaltung (24) an den ersten Eingabetreiber (52) ein Signal liefert, dessen Breite kleiner als ein Zeitablaufsignal ist, welches dazu verwendet wird, Daten von aussen über den Datenbus (DB) einzugeben;

die erste Steuereinrichtung (27B) ferner in der Weise konstruiert ist, daß dann, wenn Daten vom internen Bus (11) zum Datenbus (DB) ausgegeben werden sollen, Daten, die zum internen Bus (11) ausgegeben werden, vom ersten Ausgabe-Zwischenspeicher (50) zwischengespeichert und dann über den ersten Ausgabetreiber (51) zum Datenbus (DB) ausgegeben werden.

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5. CPU-Kern nach Anspruch 4, DADURCH GEKENNZEICHNET, DASS die zweite Steuereinrichtung (27A) in der Weise konstruiert ist, daß dann, wenn Daten vom Peripheriedatenbus (PDB) in den internen Bus (11) eingegeben werden sollen, der zweite Ausgabetreiber (41) ein logisches "1"-Signal an den Peripheriedatenbus (PDB) liefert, um den Peripheriedatenbus (PDB) vor der Eingabe der Daten vorzuladen, und dann der zweite Ausgangstreiber (41) durch ein Zeitablaufsignal, das von der Zeitablaufsignal-Steuerschaltung (24) geliefert wird, in einen Zustand hoher Impedanz geschaltet wird, um die Daten vom Peripheriedatenbus (PDB) über den zweiten Eingangstreiber (42) in den internen Bus (11) einzugeben.

Revendications

1. Noyau d'unité centrale de traitement (CPU) comprenant:

une ressource interne (10) comprenant plusieurs types de registres;
un circuit de commande (20) comportant un circuit (27) de commande de bus pour commander l'entrée et la sortie de données et autres, parmi plusieurs types de bus (11, DB, PDB) ; et
un groupe (30) de bornes comprenant une pluralité de bornes (31-1~31-2, 32-1~32-6) pour interconnecter ledit noyau de CPU à un circuit périphérique (60) et à une mémoire externe (61);
caractérisée en ce que
ladite pluralité de types de bus (11, DP, PDB) comprenant un bus interne (11) auquel des circuits individuels incorporés dans le noyau de CPU sont interconnectés, un bus de données (DB) interconnecté entre ledit noyau de CPU et la mémoire externe (61) pour permettre aux données d'être introduites et délivrées entre ledit noyau de CPU et ladite mémoire externe (61), et un bus de données périphérique (PDB) interconnecté entre ledit noyau de CPU et le circuit périphérique (60) pour permettre aux données d'être introduites et délivrées entre ledit noyau de CPU et ledit circuit périphérique (60);
les bornes d'entrée et les bornes de sortie de toutes les parties de circuit qui constituent ladite ressource interne (10) étant interconnectées audit bus interne (11);
ledit circuit (17) de commande de bus comportant des bornes d'entrée et des bornes de sortie interconnectées audit bus interne (11), audit bus de données (DB), et audit bus de données périphérique (PDB) pour commander l'entrée et la sortie de données et autres, parmi lesdits bus (11, DB, PDB) , et comprenant
un premier moyen de commande (27B) pour commander l'entrée et la sortie des données entre ledit bus interne (11) et ledit bus de données (DB); et
un second moyen de commande (27A) pour commander l'entrée et la sortie de données entre ledit bus interne (11) et ledit bus de données périphérique (PDB).

2. Noyau de CPU selon la revendication 1, **caractérisé en ce que** ladite ressource interne (10) comprend:

un accumulateur (12) pour stocker un résultat d'opération;
un registre de travail universel (13);
un pointeur (14) de pile pour pointer un emplacement à partir duquel des données doivent être lues;
des compteurs (17H, 17L) de programmes pour stocker un emplacement dans une mémoire, où une instruction à lire ultérieurement est stockée; et
une unité arithmétique et logique (16) pour exécuter des opérations arithmétiques et logiques;
un circuit de commande (20) comprenant:
des registres temporaires (21X, 21Y) pour stocker temporairement des données;
un registre d'instruction (22) pour stocker temporairement une instruction;
un décodeur d'instruction (23) pour décoder une instruction stockée dans ledit registre d'instruction (22) afin de générer divers signaux de commande;
un circuit (24) de commande de synchronisation pour générer des signaux de synchronisation nécessaires pour des opérations de parties de circuit;
un dispositif (25) de verrouillage d'adresse périphérique pour verrouiller une adresse périphérique qui est une adresse du circuit périphérique (60); et
des dispositifs (26H, 26L) de verrouillage d'adresse de mémoire externe pour verrouiller une adresse de mémoire externe qui est une adresse de la mémoire externe (61);
un groupe (30) de bornes comprenant:
une borne de sortie d'un bus d'adresse (AB), une borne d'entrée et de sortie dudit bus de données (DB), une borne d'entrée et de sortie d'un bus d'adresse périphérique (PAB), utilisée pour désigner une adresse du circuit périphérique (60), une borne d'entrée et de sortie dudit bus de données périphérique (PDB), des bornes de sortie (32-1~32-6) assignées à des signaux de synchronisation qui sont générés par ledit circuit (24) de commande de synchronisation, et des bornes d'entrée (31-1, 31-2) assignées à

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des signaux de commande appliqués audit circuit (24) de commande de synchronisation.

3. Noyau de CPU selon la revendication 2, **caractérisé en ce que**

ledit premier moyen de commande (27B) comprend:
un premier dispositif (50) de verrouillage de sortie pour verrouiller des données à délivrer par ledit bus interne (11) audit bus de données (DB);
un premier dispositif (51) de commande de sortie pour commander la synchronisation de sortie des données verrouillées par ledit dispositif (50) de verrouillage de sortie; et
un premier dispositif (52) de commande d'entrée pour commander la synchronisation d'entrée de données destinées à être introduites par ledit bus de données (DB) dans ledit bus interne (11) ; et en ce que
ledit second moyen de commande (27A) comprend:
un second dispositif (40) de verrouillage de sortie pour verrouiller des données destinées à être délivrées par ledit bus interne (11) audit bus de données périphérique (PDB);
un second dispositif (41) de commande de sortie pour commander la synchronisation de sortie de données verrouillées par ledit second dispositif (40) de verrouillage de sortie; et
un second dispositif (42) de commande d'entrée pour commander la synchronisation d'entrée de données destinées à être introduites par ledit bus de données périphérique (PDB) dans ledit bus interne (11).

4. Noyau de CPU selon la revendication 3, **caractérisé en ce que** ledit premier moyen de commande (27B) est construit de telle sorte que lorsqu'une instruction de données doit être introduite par ledit bus de données (DB) dans ledit bus interne (11), ledit circuit (24) de commande de synchronisation délivre audit premier dispositif (52) de commande d'entrée un signal ayant une largeur inférieure à un signal de synchronisation qui est utilisé pour introduire des données depuis l'extérieur, par l'intermédiaire du bus de données (DB);

ledit premier moyen de commande (27B) étant en outre construit de telle sorte que lorsque des données doivent être délivrées par ledit bus interne (11) audit bus de données (DB), les données délivrées audit bus interne (11) sont verrouillées par ledit premier dispositif (50) de verrouillage de sortie puis sont délivrées audit bus de données (DB) par l'intermédiaire dudit premier dispositif (51) de commande de sortie.

5. Noyau de CPU selon la revendication 4, **caractérisé en ce que** ledit second moyen de commande (27A) est construit de telle sorte que lorsque des données doivent être introduites par ledit bus de données périphérique (PDB) dans ledit bus interne (11), ledit second dispositif (41) de commande de sortie délivre un signal "1" logique audit bus de données périphérique (PDB) pour pré-charger ledit bus de données périphérique (PDB) avant l'entrée desdites données, puis ledit second dispositif (41) de commande de sortie est mis dans un état d'impédance élevée par un signal de synchronisation émis par ledit circuit (24) de commande de signal de synchronisation, de manière à introduire lesdites données en provenance dudit bus de données périphérique (PDB) dans ledit bus interne (11), par l'intermédiaire dudit second dispositif (42) de commande d'entrée.

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