

CLAIMS

1. An electrostatic chuck comprising:
 - (a) a top surface of the electrostatic chuck having a total area and a bottom surface, the top surface of the electrostatic chuck comprising:
 - (i) a central region (CR) comprising a plurality of substrate support mesas extending from a CR top surface and having a contact area coverage;
 - (ii) an inner channel (IC) with an IC bottom surface and an IC width, wherein the inner channel surrounds the central region;
 - (iii) an inner band (IB) with an IB top surface and an IB width,
 - (1) wherein the inner band surrounds the inner channel; and
 - (2) wherein a first depth from the CR top surface to the IC bottom surface is less than a second depth from the IB top surface to the IC bottom surface;
 - (iv) an outer channel (OC) with an OC bottom surface and an OC width surrounding the inner band; and
 - (v) an outer band (OB) with an OB top surface and an OB width surrounding the outer channel, wherein the first depth is less than a third depth from the OB top surface to the OC bottom surface; and
 - (b) a controller configured to control temperature across a wafer secured to the top surface of the electrostatic chuck during processing.
2. The electrostatic chuck of claim 1, wherein a maximum pressure of coolant within the inner channel and the outer channel is 20 Torr.
3. The electrostatic chuck of claim 1, wherein a pressure within the inner channel (IC pressure) is less than a pressure within the outer channel (OC pressure).
4. The electrostatic chuck of claim 3, wherein a difference between the IC pressure and the OC pressure is greater than or equal to 8 Torr.

5. The electrostatic chuck of claim 3, wherein the OC pressure is greater than or equal to 14 Torr.
6. The electrostatic chuck of claim 3, wherein a ratio of the OC pressure to the IC pressure is in a range of 2.5 to 4.
7. The electrostatic chuck of claim 1,
wherein the electrostatic chuck is configured to have a concentration of hydrogen (H%) across a surface of the wafer secured to the electrostatic chuck during processing with a range in variability divided by 2 ($R/2$) of less than or equal to 2% across the wafer during processing.
8. The electrostatic chuck of claim 7, wherein the $R/2$ is less than or equal to 0.5% across the surface of the wafer.
9. The electrostatic chuck of claim 1, wherein the contact area coverage of the plurality of substrate support mesas is less than 7% of the total area of the top surface of the electrostatic chuck.
10. The electrostatic chuck of claim 1, wherein surface roughness of the outer band is less than or equal to 20 arithmetic mean roughness (Ra) as measured by a surface profilometer.
11. The electrostatic chuck of claim 1, wherein the plurality of substrate support mesas are circular in shape.
12. The electrostatic chuck of claim 1, wherein the contact area coverage of the plurality of substrate support mesas is less than 5% of the total area of the top surface of the electrostatic chuck.

13. The electrostatic chuck of claim 1, wherein an area of the plurality of substrate support mesas comprises less than 10% of a total area of the top surface of the electrostatic chuck.
14. The electrostatic chuck of claim 1, wherein the OC width is in a range of 2 mm to 6 mm.
15. The electrostatic chuck of claim 1, wherein the OB width is in a range of 3.5 mm to 4 mm.
16. The electrostatic chuck of claim 1, wherein the OB width is in a range of 2.8 mm to 3.1 mm.
17. The electrostatic chuck of claim 1, wherein the IB width is in a range of 1.2 mm to 1.6 mm.