

TITLE OF THE INVENTION
DIGITAL BROADCAST RECEIVER

BACKGROUND OF THE INVENTION

The present invention relates to a digital broadcast receiver for receiving a digital broadcast signal transmitted as a digitally modulated video signal.

A usual satellite broadcast receiver is a receiver for receiving an FM (frequency modulated) satellite broadcast signal transmitted with a frequency modulated video signal and as shown in FIG. 14, a desired frequency modulated signal is frequency converted from a first IF (intermediate frequency) signal from a digitally modulated signal into a designated second intermediate frequency signal, a frequency modulated signal in the desired channel is taken out at a channel filter and then it is frequency demodulated.

A local oscillation signal used for the frequency conversion is generated at a PLL (phase-locked loop) synthesizer 30, which is composed of a local oscillator 31, a prescaler 32 frequency dividing a local oscillation signal, a programmable frequency divider 33, a phase frequency detector 34, a reference frequency signal divider 35, a reference frequency signal generator 36 and a loop filter 37. The local oscillation frequency F_{vco} is expressed by (eq. 1).

$$fvco = (fr / R) \times Npsc \times Np \dots\dots\dots (eq. 1)$$

where $fvco$: oscillation frequency of the local oscillator,

fr : frequency of the reference frequency signal,

$Npsc$: frequency dividing ratio of the prescaler,

Np : frequency dividing ratio of the programmable frequency divider, and

R : frequency dividing ratio of the reference frequency

signal.

The local oscillation signal according to the frequency of the desired channel is obtained by varying the dividing ratio of programmable frequency divider 33 by microcomputer (CPU) 50. AFC (automatic frequency control) for compensating the frequency drift of the first IF signal due to the frequency drift of a frequency converter (not shown in the drawing) in a receiving antenna for satellite broadcast is made by that microcomputer 50 controls the frequency dividing ratio of programmable frequency divider 33 in PLL synthesizer 30 by a frequency drift detecting signal outputted from a FM demodulator 201, as disclosed in USP 1871000.

A usual receiver for digital broadcast receiving a transmitted signal using QPSK (quarternary phase-shift keying) modulation as a digital modulation shown in FIG. 15 is a receiver for FM satellite broadcast frequency-modulating a video signal and a QPSK-modulated PCM (pulse code modulation) audio signal and a desired FM signal is obtained by frequency-converting into a designated second IF signal from the first IF signal outputted from the antenna for satellite broadcast and an FM signal of the desired channel is taken out through a channel filter and is frequency modulated and then it is separated into a video signal and an audio signal and they are processed.

A local oscillation signal used for the frequency conversion is generated at a PLL synthesizer 30, which is composed of a local oscillator 31, a prescaler 32 frequency dividing a local oscillation signal, a programmable frequency divider 33, a reference frequency signal generator 36, a reference frequency signal divider 35, phase detection means 34 and a loop filter 37. The local oscillation frequency can be expressed by (eq. 1) like the case of broadcast receiver receiving a previously-mentioned FM signal.

Therefore, a local oscillation signal corresponding to a desired channel frequency is obtained by varying a frequency dividing ratio of the programmable frequency divider by microcomputer 50.

The control by microcomputer 50 is necessary for a control of many LSIs (large scale integrations) such as not only PLL synthesizer 30 but also PCM sound signal processor 205 and the like. A common bus such as an IIC (inter integrated circuit) bus is used as a control bus because the number of output terminals of microcomputer 50 has a limitation.

AFC for compensating the frequency drift of the first IF signal due to the frequency drift of a frequency converter in a receiving antenna for satellite broadcast is made by that microcomputer 50 controls the frequency dividing ratio of programmable frequency divider 33 in PLL synthesizer 30 by a frequency drift detecting signal outputted from a FM demodulator 201, as disclosed in USP 1871000, like an example of the prior art. The control data of the microcomputer is renewed at every several tens milliseconds, considering malfunction of a PLL synthesizer and each LSI (large scale integration circuit) due to a surge of thunder even after signal reception.

However, in the case in which a usual AFC is done at a PLL synthesizer for channel selection, the reference frequency f_r/R of a phase detection at the PLL synthesizer determines AFC accuracy and if the frequency dividing ratio of the reference frequency signal is so much decreased, the number of steps of AFC control becomes large and a correct AFC can not be done. In a receiver of digital modulation such as QPSK modulation, because the phase noise characteristic of a local oscillation frequency signal influences a bit error rate, the phase noise must be small and it is necessary not only to improve a phase noise characteristic of a local oscillator circuit itself but also to improve a phase noise characteristic by the PLL synthesizer

such as making a reference frequency f_r/R of the PLL synthesizer for phase frequency detection large.

In the case of a receiver receiving a digitally modulated signal such as QPSK modulation, when a control data is inputted from a microcomputer to a PLL synthesizer, the control data gives an interference to the local oscillator circuit for channel selection and the noise characteristic of the local oscillation signal rapidly deteriorates. Thus, the noise characteristic of the local oscillation signal gives an influence to the bit error rate.

By using a control bus from the microcomputer to the PLL synthesizer in common with a control bus of the other signal processing LSIs, when the other signal processing LSIs are controlled during reception, the control data is inputted also to the PLL synthesizer and whenever AFC during reception is made in the PLL synthesizer or the control data is periodically renewed against malfunction of the PLL synthesizer due to a surge or the like, noise in the local oscillation signal becomes big and deteriorates the bit error rate and the quality of reception. This is a problem.

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SUMMARY OF THE INVENTION

The present invention aims to make a high performance reception possible which can simultaneously attain improvement of AFC function at channel selection means and improvement of bit error rate possible in a receiver receiving a digitally modulated signal. To achieve this object, a digital broadcast receiver receiving a digitally modulated signal of the present invention includes:

channel selection means inputting said digitally modulated signal of an RF band and for frequency-converting a desired digitally modulated signal into an IF signal;

oscillation means for generating a local oscillation

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signal used for a frequency conversion at the channel selection means;

oscillation frequency control means for controlling a frequency of a local oscillation signal of the oscillation means;

phase noise characteristic control means for improving the phase noise characteristic of the local oscillation signal generated at the oscillation means;

filter means for extracting the IF signal corresponding to the selected channel;

orthogonal detection means for orthogonally detecting the IF signal extracted at the filter means;

A/D conversion means for converting an analog output of the orthogonal detection means into a digital signal; and

digital demodulation means for demodulating the digital output of the A/D conversion means; and wherein

the phase noise characteristic of the local oscillation signal is improved.

The present invention is a digital broadcast receiver in which a phase noise characteristic of a local oscillation signal is improved, keeping an AFC accuracy by that the phase noise characteristic control means does AFC (automatic frequency control) continuously at the orthogonal detection means using an AFC signal expressing a frequency drift of a receiving signal detected at the digital demodulation means and the reference frequency of phase detection of the PLL synthesizer comprising the oscillation means and the oscillation frequency control means is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced by making an open loop gain of the PLL synthesizer large.

The present invention is a digital broadcast receiver in which the phase noise characteristic control means prevents deterioration of a noise characteristic of a local oscillation signal by using an exclusive control bus for transmitting a

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control signal of oscillation frequency control means and separating it from the other control buses for transmitting control signals of the other devices including digital demodulation means.

The present invention is a digital broadcast receiver in which the phase noise characteristic of the local oscillation signal can be prevented to deteriorate and the bit error rate characteristic can be prevented to deteriorate with the control data supplied from the microcomputer during reception by limiting the control of the oscillation frequency control means to the case in which a channel is selected or the demodulation signal is not synchronized.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a digital satellite broadcast receiver in accordance with a first exemplary embodiment of the present invention.

FIG. 2 is a block diagram of a digital satellite broadcast receiver in accordance with a second exemplary embodiment of the present invention.

FIG. 3 is a block diagram of a digital satellite broadcast receiver in accordance with a third exemplary embodiment of the present invention.

FIG. 4 is a circuit diagram of a voltage controlled oscillator composing a PLL synthesizer for channel selection.

FIG. 5 is a phase noise characteristic of a voltage controlled oscillator composing a PLL synthesizer for channel selection.

FIG. 6 is an AFC characteristic of an orthogonal detection voltage controlled oscillator.

FIG. 7 is a block diagram of a digital satellite broadcast receiver in accordance with a fourth exemplary embodiment of the present invention.

FIG. 8 is a block diagram of a digital satellite

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broadcast receiver in accordance with a fifth exemplary embodiment of the present invention.

FIG. 9 is a block diagram of a digital satellite broadcast receiver in accordance with a sixth exemplary embodiment of the present invention.

FIG. 10 is a block diagram of a digital satellite broadcast receiver in accordance with a seventh exemplary embodiment of the present invention.

FIG. 11 is a block diagram of a digital satellite broadcast receiver in accordance with an eighth exemplary embodiment of the present invention.

FIG. 12 is a block diagram of a digital satellite broadcast receiver in accordance with a ninth exemplary embodiment of the present invention.

FIG. 13 is an exemplary circuit diagram of an orthogonal detection voltage controlled oscillator.

FIG. 14 is a block diagram of a satellite broadcast receiver in accordance with the prior art.

FIG. 15 is a block diagram of a digital satellite broadcast receiver in accordance with the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Some exemplary embodiments of the present invention are explained below, referring to FIGs. 1 to 12.

(First exemplary embodiment)

In FIG. 1, the terminal 10 is an input terminal of a first IF signal from a receiving antenna for satellite broadcast. The block 11 is a mixer for frequency-converting a desired QPSK modulation signal into a designated second IF signal. The block 12 is a bandpass filter for extracting only the designated second IF signal from the output of mixer 11. The block 16 is orthogonal detector inputting the output of bandpass filter 12 and for obtaining base band signals of an in-phase component I and a quadrature component Q by orthogonal detection. The block 21 is an A/D converter inputting the output of the I/Q orthogonal

detector 16 and for converting the I and Q base band signals into digital signals. The block 22 is a QPSK demodulator inputting the digitalized I and Q signals and for demodulating the inputted I and Q signals by QPSK. The block 30 is a PLL synthesizer for generation a local oscillation signal necessary when the desired QPSK modulation signal is frequency-converted into a designated second IF signal at mixer 11. The block 17 is an orthogonal detection voltage-controlled oscillator for generating a local oscillation signal necessary for orthogonal detection.

The function of a digital broadcast receiver composed like the above is explained below. The first IF signal from a digitally modulated signal of RF band received from a receiving antenna for satellite broadcast is mixed with a local oscillation signal generated at PLL synthesizer 30 at mixer 11 and a desired QPSK modulation signal of the first IF signal is frequency-converted into a designated second IF signal.

PLL synthesizer 30 is composed of a local oscillator 31, a prescaler 32, a programmable frequency divider 33, a phase frequency detector 34, a reference frequency signal divider 35, a reference frequency signal generator 36 and a loop filter 37.

The output of local oscillator 31 is frequency-divided at prescaler 32, is inputted to programmable frequency divider 33 and is further frequency-divided. The output of programmable frequency divider 33 is inputted to phase detector 34 and PLL synthesizer 30 is controlled so that the inputted signal to phase detector 34 coincides with a reference frequency signal 40 obtained by dividing the output of a reference frequency signal generator 36 at a reference frequency signal divider 35 in frequency and phase. The local oscillation frequency f_{vco} is expressed by eq. 2.

$$f_{vco} = (f_r / R) \times N_{psc} \times N_p \dots\dots\dots (eq. 2)$$

where f_{vco} : oscillation frequency of the local oscillator,

f_r : frequency of the reference frequency signal,

N_{psc} : frequency dividing ratio of the prescaler,

N_p : frequency dividing ratio of the programmable frequency divider, and

R : frequency dividing ratio of the reference frequency signal.

A local oscillation frequency corresponding to a frequency of a desired QPSK modulation signal can be obtained by varying the frequency dividing ratio N_p of programmable frequency divider 33 at microcomputer 50.

The QPSK modulation signal frequency-converted into a designated second IF signal at mixer 11 is inputted to orthogonal detector 16 after being extracted at bandpass filter 12. At orthogonal detector 16, an oscillation signal generated at orthogonal detection voltage-controlled oscillator 17 with a designated second IF and a signal phase-shifted by 90 degrees from the oscillation signal are supplied to mixers 13 and 15, respectively and they are mixed with the output signal of bandpass filter 12 there and base band signals of an in-phase component I and a quadrature component Q in the QPSK modulation signal are obtained, respectively. The I and Q base band signals are converted to digital signals at an A/D converter 21 and are digitally demodulated at QPSK demodulator 22. QPSK demodulator 22 includes a carrier recovery and a clock recovery necessary for demodulation, an AGC detector and an AFC detector.

The oscillation frequency of local oscillator 31 generating a local frequency signal used for channel selection of a QPSK modulation signal is expressed by (eq. 3).

$$f_{vco} = f_{1stIF} + f_{2ndIF} \dots\dots\dots (eq. 3)$$

where f_{vco} : oscillation frequency of the local oscillator for channel selection,

f_{1stIF} : frequency of the first IF, and

f_{2ndIF} : frequency of the second IF.

The oscillation frequency of local oscillator 31 is

higher than the frequency of the first IF inputted from the receiving antenna for satellite broadcast by the frequency of the second IF and a frequency range of the first IF signal is necessary as an oscillation frequency range.

As an oscillator circuit to obtain such a wide frequency range, an oscillator having a resonant circuit using a microstrip line and a variable capacitance diode as shown in FIG. 4 is necessary.

In a digital modulation like QPSK, the phase noise of a local oscillation signal used for frequency conversion influences on a reception performance (bit error rate) of the receiver, different from a usual FM modulation. As a phase noise not to influence on bit error rate, 85 dBc/Hz at a frequency off-set by 10 kHz from the oscillation frequency and 95 dBc/Hz at a frequency off-set by 100 kHz from the oscillation frequency.

The phase noise of a local oscillation signal having a wide oscillation frequency range, however, becomes large because the quality factor Q of the resonant circuit decreases due to an internal resistance of the variable capacitance diode and the phase noise power decreases according to increase of frequency deviation from the oscillation frequency as shown in FIG. 5. That is a $1/f$ characteristic. The noise characteristic near the oscillation frequency such as at 10 kHz and 100 kHz previously described can be improved by using a PLL synthesizer and can be realized by making a reference frequency of the phase detection at PLL synthesizer 30 high and making an open loop gain high. The reference frequency is determined by an oscillation frequency at reference frequency signal generator 36 and a frequency dividing ratio at reference frequency signal divider 35 and it is selected as high as the phase noise near the oscillation frequency can be reduced and its value is several hundreds kHz. The reference frequency (f_r/R) of the phase frequency detection is a step

frequency of PLL synthesizer 30 and the output frequency of local oscillator 31 is integer times of the reference frequency and does not always coincide with local oscillation frequency to convert the first IF signal into a designated second IF signal.

That is, a deviation occurs in the frequency of the second IF signal. Therefore, by making orthogonal detection voltage-controlled oscillator 17 so that the oscillation frequency continuously varies by an AFC signal outputted from QPSK demodulator 22 as shown in FIG. 6, frequency drift of a frequency converter (not shown) in a receiving antenna for satellite broadcast and frequency drift from the original second IF frequency due to frequency drift by increasing the reference frequency of phase frequency detection at PLL synthesizer 30 can be compensated with high accuracy at orthogonal detector 16.

Thus, according to the first exemplary embodiment of the present invention, the characteristic of bit error rate as a receiver can be kept good, because a phase noise characteristic of the local oscillation frequency is improved keeping AFC accuracy.

The frequency drift of the second IF signal can be also compensated with a high accuracy at orthogonal detector 16 by controlling orthogonal detection voltage-controlled oscillator 17 by PLL synthesizer, making its step frequency smaller enough than the step frequency of PLL synthesizer 30 used for channel selection and varying the oscillation frequency according to an AFC signal outputted from QPSK demodulator 22. Thus, the characteristic of bit error rate as a receiver can be kept good, because a phase noise characteristic of the local oscillation frequency is improved keeping AFC accuracy.

Although a reception of satellite broadcast is described in the exemplary embodiment, it is obvious to have the same effect as described above in general kinds of receivers receiving a digitally modulated signal.

(Second exemplary embodiment)

In FIG. 2, the terminal 10 is an input terminal of a first IF signal from a receiving antenna for satellite broadcast. The block 11 is a mixer for frequency-converting a desired QPSK modulation signal into a designated second IF signal. The block 12 is a bandpass filter for extracting only the designated second IF signal from the output of mixer 11. The block 16 is orthogonal detection means inputting the output of bandpass filter 12 and for obtaining base band signals of an in-phase component I and a quadrature component Q by orthogonal detection. The block 21 is an A/D converter inputting the output of the I/Q orthogonal detection means 16 and for converting the base band signals of I and Q components into digital signals. The block 22 is a QPSK demodulator inputting the digitalized I and Q signals and for demodulating the inputted I and Q signals by QPSK. The block 30 is a PLL synthesizer for generation a local oscillation signal necessary when the desired QPSK modulation signal is frequency-converted into a designated second IF signal at mixer 11. The block 17 is an orthogonal detection voltage-controlled oscillator for generating a local oscillation signal necessary for orthogonal detection.

The function of a digital broadcast receiver composed like the above is explained below. The first IF signal received through a receiving antenna for satellite broadcast is mixed with a local oscillation signal generated at PLL synthesizer 30 at mixer 11 and a desired QPSK modulation signal of the first IF signal is frequency-converted into a designated second IF signal.

PLL synthesizer 30 is composed of a local oscillator 31, a prescaler 32, a programmable frequency divider 33, a phase frequency detector 34, a reference frequency signal divider 35 and a loop filter 37.

The output of local oscillator 31 is frequency-divided at prescaler 32, is inputted to programmable frequency divider 33 and is further frequency-divided. The output of programmable

frequency divider 33 is inputted to phase detector 34 and PLL synthesizer 30 is controlled so that the inputted signal to phase detector 34 coincides with a reference frequency signal 40 obtained by dividing the symbol clock of QPSK recovered at QPSK demodulator 22 at a reference frequency signal divider 35 in frequency and phase. The local oscillation frequency f_{vco} is expressed by (eq. 4).

$$f_{vco} = (f_r / R) \times N_{psc} \times N_p \dots\dots\dots(\text{eq. 4})$$

where f_{vco} : oscillation frequency of the local oscillator,

f_r : frequency of the reference frequency signal,

N_{psc} : frequency dividing ratio of the prescaler,

N_p : frequency dividing ratio of the programmable frequency divider, and

R : frequency dividing ratio of the reference frequency signal.

A local oscillation frequency corresponding to a frequency of a desired QPSK modulation signal can be obtained by varying frequency dividing ratio N_p of programmable frequency divider 33 by microcomputer 50.

The QPSK modulation signal frequency-converted into a designated second IF signal at mixer 11 is inputted to orthogonal detector 16 after being extracted at bandpass filter 12. At orthogonal detector 16, an oscillation signal generated at orthogonal detection voltage-controlled oscillator 17 with a designated second IF and a signal phase-shifted by 90 degrees from the oscillation signal are supplied to mixers 13 and 15, respectively and they are mixed with the output signal of bandpass filter 12 there and base band signals of an in-phase component I and a quadrature component Q of the QPSK modulation signal, respectively.

The I and Q base band signals are converted to digital signals at an A/D converter 21 and are digitally demodulated at QPSK demodulator 22. QPSK demodulator 22 includes a carrier

recovery and a clock recovery necessary for demodulation, an AGC detector and an AFC detector.

The oscillation frequency of local oscillator 31 generating a local frequency signal used for channel selection of a QPSK modulation signal is expressed by (eq. 5).

$$fvco = f1stIF + f2ndIF \dots\dots\dots(eq. 5)$$

where fvco: oscillation frequency of the local oscillator for channel selection,

f1stIF: frequency of the first IF, and

f2ndIF: frequency of the second IF.

The oscillation frequency of local oscillator 31 is higher than the frequency of the first IF inputted from the receiving antenna for satellite broadcast by the frequency of the second IF and a frequency range of the first IF signal is necessary as an oscillation frequency range. As an oscillator circuit to obtain such a wide frequency range, an oscillator having a resonant circuit using a microstrip line and a variable capacitance diode as shown in FIG. 4 is necessary.

In a digital modulation like QPSK, the phase noise of a local oscillation signal used for frequency conversion influences on a reception performance (bit error rate) of the receiver, different from a usual FM modulation. As a phase noise not to influence on bit error rate, 85 dBc/Hz at a frequency off-set by 10 kHz from the oscillation frequency and 95 dBc/Hz at a frequency off-set by 100 kHz from the oscillation frequency.

The phase noise of a local oscillation signal having a wide oscillation frequency range, however, becomes large because the quality factor Q of the resonant circuit decreases due to an internal resistance of the variable capacitance diode and the phase noise power decreases according to increase of frequency deviation from the oscillation frequency as shown in FIG. 5. That is a 1/f characteristic. The noise characteristic near the

oscillation frequency such as at 10 kHz and 100 kHz previously described can be improved by using a PLL synthesizer and can be realized by making a reference frequency of the phase detection at PLL synthesizer 30 high and making an open loop gain high. The reference frequency is determined by a frequency f_r of a QPSK symbol clock (baud rate of QPSK) recovered at QPSK demodulator 22 and a frequency dividing ratio R at reference frequency signal divider 35 and it is selected as high as the phase noise near the oscillation frequency of local oscillator 31 can be reduced and its value is several hundreds kHz.

In Japan, the symbol clock frequency is 21.096 MHz in a digital satellite broadcast and to exceed the reference frequency of several hundreds kHz, a frequency dividing ratio of 32 to 128 is necessary as a frequency dividing ratio of reference frequency signal divider 35. The reference frequency f_r/R of the phase frequency detection is a step frequency of PLL synthesizer 30 and the output frequency of local oscillator 31 is integer times of the reference frequency and does not always coincide with local oscillation frequency to convert the first IF signal into a designated second IF signal. That is, a deviation occurs in the frequency of the second IF signal.

Therefore, by making orthogonal detection voltage-controlled oscillator 17 so that the oscillation frequency continuously varies by an AFC signal outputted from QPSK demodulator 22 as shown in FIG. 6, frequency drift of a frequency converter (not shown) in a receiving antenna for satellite broadcast and frequency drift from the original second IF frequency due to frequency drift by increasing the reference frequency of PLL synthesizer 30 can be compensated with high accuracy at orthogonal detector 16.

Thus, according to the second exemplary embodiment of the present invention, because a phase noise characteristic of the

local oscillation frequency is improved keeping AFC accuracy, the characteristic of bit error rate as a receiver can be kept good and because a clock signal recovered at QPSK demodulator 20 is frequency-divided and the divided signal is used as a reference frequency signal of phase frequency detection at PLL synthesizer 30 and a clock signal of the transmitter side in good accuracy is used as a reference frequency signal, the frequency accuracy of the reference frequency signal against temperature variation is kept good and a reference frequency signal generator in PLL synthesizer 30 can be eliminated.

It is obvious that a similar effect can be obtained also in the case in which the reference frequency signal of the phase frequency detection at PLL synthesizer 30 is obtained by frequency-dividing a sampling clock of the A/D converter 21 recovered at QPSK demodulator 22 and a reference frequency signal divider 35 having a frequency dividing ratio corresponding to that of the sampling clock.

Also by controlling orthogonal detection voltage-controlled oscillator 17 by PLL synthesizer, making the step frequency smaller enough than the step frequency of PLL synthesizer 30 used for channel selection and varying the oscillation frequency according to the AFC signal outputted from QPSK demodulator 22, frequency drift of the second IF signal can be compensated with high accuracy at orthogonal detector 16 and the characteristic of bit error rate as a receiver can be kept good, because a phase noise characteristic of the local oscillation frequency is improved keeping AFC accuracy.

(Third exemplary embodiment)

In FIG. 3, the terminal 10 is an input terminal of a first IF signal from a receiving antenna for satellite broadcast. The block 11 is a mixer for frequency-converting a desired QPSK modulation signal into a designated second IF signal. The block

12 is a bandpass filter for extracting only the designated second IF signal from the output of mixer 11. The block 16 is orthogonal detection means inputting the output of bandpass filter 12 and for obtaining base band signals of an in-phase component I and a quadrature component Q by orthogonal detection. The block 21 is an A/D converter inputting the output of the I/Q orthogonal detection means 16 and for converting the I and Q base band signals into digital signals. The block 22 is a QPSK demodulator inputting the digitalized I and Q signals and for demodulating the inputted I and Q signals by QPSK. The block 23 is an error correction decoder. The block 24 is a demultiplexer for demultiplexing a transport stream in which band compressed video and sound signals are multiplexed. The block 30 is a PLL synthesizer for generation a local oscillation signal necessary when the desired QPSK modulation signal is frequency-converted into a designated second IF signal at mixer 11. The block 17 is an orthogonal detection voltage-controlled oscillator for generating a local oscillation signal necessary for orthogonal detection.

The function of a digital broadcast receiver composed like the above is explained below.

The first IF signal received through a receiving antenna for satellite broadcast is mixed with a local oscillation signal generated at PLL synthesizer 30 at mixer 11 and a desired QPSK modulation signal of the first IF signal is frequency-converted into a designated second IF signal. PLL synthesizer 30 is composed of a local oscillator 31, a prescaler 32, a programmable frequency divider 33, a phase frequency detector 34, a reference frequency signal divider 35 and a loop filter 37.

The output of local oscillator 31 is frequency-divided at prescaler 32, is inputted to programmable frequency divider 33 and is further frequency-divided. The output of programmable frequency divider 33 is inputted to phase detector 34 and PLL synthesizer 30 is controlled so that the inputted signal to phase

detector 34 coincides with a reference frequency signal 40 obtained by dividing the system clock signal generated at demultiplexer 24 at a reference frequency signal divider 35 in frequency and phase. The local oscillation frequency f_{vco} is expressed by (eq. 6).

$$f_{vco} = (f_r / R) \times N_{psc} \times N_p \dots\dots\dots(\text{eq. 6})$$

where f_{vco} : oscillation frequency of the local oscillator,

f_r : frequency of the reference frequency signal,

N_{psc} : frequency dividing ratio of the prescaler,

N_p : frequency dividing ratio of the programmable frequency divider and

R : frequency dividing ratio of the reference frequency signal.

A local oscillation frequency corresponding to a frequency of a desired QPSK modulation signal can be obtained by varying frequency dividing ratio N_p of programmable frequency divider 33 by microcomputer 50.

The QPSK modulation signal frequency-converted into a designated second IF signal at mixer 11 is inputted to orthogonal detector 16 after being extracted at bandpass filter 12. At orthogonal detector 16, an oscillation signal generated at orthogonal detection voltage-controlled oscillator 17 with a designated second IF and a signal phase-shifted by 90 degrees from the oscillation signal are supplied to mixers 13 and 15, respectively and they are mixed with the output signal of bandpass filter 12 there and base band signals of an in-phase component I and a quadrature component Q of the QPSK modulation signal, respectively.

The I and Q base band signals are converted to digital signals at an A/D converter 21 and are digitally demodulated at QPSK demodulator 22. QPSK demodulator 22 includes a carrier recovery and a clock recovery necessary for demodulation, an AGC detector and an AFC detector. The output of QPSK demodulator 22

does Viterbi decoding, deinterleaving, Reed-Solomon decoding or the like at error correction decoder 23 and corrects the error generated at a transmission route. The output signal from error correction decoder 23 is a transport stream multiplexed with video and sound signals encoded for band compression. Demultiplexer 24 demultiplexes and extracts video and sound signals encoded from the transport stream. The output of demultiplexer 24 is band expanded for each of video and sound signals and video and sound signals are reproduced.

The oscillation frequency of local oscillator 31 generating a local frequency signal used for channel selection of a QPSK modulation signal is expressed by (eq. 7).

$$fvco = flstIF + f2ndIF \dots\dots\dots(eq. 7)$$

where fvco: oscillation frequency of the local oscillator for channel selection,

flstIF: frequency of the first IF, and

f2ndIF: frequency of the second IF.

The oscillation frequency of local oscillator 31 is higher than the frequency of the first IF inputted from the receiving antenna for satellite broadcast by the frequency of the second IF and a frequency range of the first IF signal is necessary as an oscillation frequency range.

As an oscillator circuit to obtain such a wide frequency range, an oscillator having a resonant circuit using a microstrip line and a variable capacitance diode as shown in FIG. 4 is necessary. In a digital modulation like QPSK, the phase noise of a local oscillation signal used for frequency conversion influences on a reception performance (bit error rate) of the receiver, different from a usual FM modulation. As a phase noise not to influence on bit error rate, 85 dBc/Hz and 95 dBc/Hz are necessary at frequencies off-set by 10 kHz and 100 kHz from the oscillation frequency, respectively.

The phase noise of a local oscillation signal having a wide oscillation frequency range, however, becomes large because the quality factor Q of the resonant circuit decreases due to an internal resistance of the variable capacitance diode and the phase noise power decreases according to increase of frequency deviation from the oscillation frequency as shown in FIG. 5. That is a $1/f$ characteristic. The noise characteristic near the oscillation frequency such as at 10 kHz and 100 kHz previously described can be improved by using a PLL synthesizer and can be realized by making a reference frequency of the phase detection at PLL synthesizer 30 high and making an open loop gain high. The reference frequency is determined by a frequency of a QPSK system clock generated at demultiplexer 24 and a frequency dividing ratio at reference frequency signal divider 35 and it is selected as high as the phase noise near the oscillation frequency of local oscillator 31 can be reduced and its value is several hundreds kHz. The system clock frequency generated at demultiplexer 24 is 27 MHz and to exceed the reference frequency of several hundreds kHz, a frequency dividing ratio of 32 to 128 is necessary as a frequency dividing ratio of reference frequency signal divider 35. The reference frequency (f_r/R) is a step frequency of PLL synthesizer 30 and the output frequency of local oscillator 31 is integer times of the reference frequency and does not always coincide with local oscillation frequency to convert the first IF signal into a designated second IF signal. That is, a deviation occurs in the frequency of the second IF signal.

Therefore, by making orthogonal detection voltage-controlled oscillator 17 so that the oscillation frequency continuously varies by an AFC signal outputted from QPSK demodulator 22 as shown in FIG. 6, frequency drift of a frequency converter (not shown) in a receiving antenna for satellite broadcast and frequency drift from the original second IF frequency due to frequency drift by increasing the reference frequency of PLL synthesizer 30 can be compensated with high

accuracy at orthogonal detector 16.

Thus, according to the third exemplary embodiment of the present invention, because a phase noise characteristic of the local oscillation frequency is improved keeping AFC accuracy, the characteristic of bit error rate as a receiver can be kept good and because a system clock signal at demultiplexer means of encoded and multiplexed video and sound signals is frequency-divided and the divided signal is used as a reference frequency signal of phase frequency detection at PLL synthesizer 30 and a clock signal of the transmitter side in good accuracy is used as a reference frequency signal, the frequency accuracy of the reference frequency signal against temperature variation is kept good and a reference frequency signal generator in PLL synthesizer 30 can be eliminated.

Also by controlling orthogonal detection voltage-controlled oscillator 17 by PLL synthesizer, making the step frequency smaller enough than the step frequency of PLL synthesizer 30 used for channel selection and varying the oscillation frequency according to the AFC signal outputted from QPSK demodulator 22, frequency drift of the second IF signal can be compensated with high accuracy at orthogonal detector 16 and the characteristic of bit error rate as a receiver can be kept good, because a phase noise characteristic of the local oscillation frequency is improved keeping AFC accuracy.

(Fourth exemplary embodiment)

In FIG. 7, the terminal 10 is an input terminal of a first IF signal from a receiving antenna for satellite broadcast. The block 11 is a mixer for frequency-converting a desired QPSK modulation signal into a designated second IF signal. The block 12 is a bandpass filter for extracting only the designated second IF signal from the output of mixer 11. The block 16 is orthogonal detection means inputting the output of bandpass filter 12 and

for obtaining base band signals of an in-phase component I and a quadrature component Q by orthogonal detection. The block 21 is an A/D converter inputting the output of the I/Q orthogonal detection means 16 and for converting the base band signals of I and Q components into digital signals. The block 22 is a QPSK demodulator inputting the digitalized I and Q signals and for demodulating the inputted I and Q signals by QPSK. The block 23 is an error correction decoder. The block 24 is a transport demultiplexer for separating a transport stream signal which band compressed video and sound signals are multiplexed. The block 30 is a PLL synthesizer for generation a local oscillation signal necessary when the desired QPSK modulation signal is frequency-converted into a designated second IF signal at mixer 11. The block 17 is an orthogonal detection oscillator for generating a local oscillation signal necessary for orthogonal detection. The block 50 is a microcomputer. The block 111 is a control bus from microcomputer 50 to PLL synthesizer 30. The block 112 is a control bus from microcomputer 50 to QPSK demodulator 22 and the like.

The function of a digital broadcast receiver composed like the above is explained below.

The first IF signal received through a receiving antenna for satellite broadcast is mixed with a local oscillation signal generated at PLL synthesizer 30 at mixer 11 and a desired QPSK modulation signal of the first IF signal is frequency-converted into a designated second IF signal. PLL synthesizer 30 is composed of a local oscillator 31, a prescaler 32, a programmable frequency divider 33, a phase frequency detector 34, a reference frequency signal divider 35, reference frequency signal generator 36 and a loop filter 37.

The output of local oscillator 31 is inputted to programmable frequency divider 33 and frequency-divided after being frequency-divided at prescaler 32. The output of programmable frequency divider 33 is inputted to phase frequency detector 34 and PLL synthesizer 30 is controlled so that the

inputted signal to phase detector 34 coincides in frequency and phase with a reference frequency signal 40 obtained by dividing the output of a reference frequency signal generator 36 at a reference frequency signal divider 35. The local oscillation frequency F_{vco} is expressed by (eq. 2) as previously shown and a local oscillation frequency corresponding to a frequency of desired QPSK modulation signal can be obtained by varying a frequency dividing ratio N_p of programmable frequency divider 33 by microcomputer 50. The QPSK modulation signal frequency-converted into a designated second IF at mixer 11 is inputted to orthogonal detector 16 after being extracted at bandpass filter 12.

At orthogonal detector 16, an oscillation signal generated at orthogonal detection oscillator 17 with a designated second IF and a signal phase-shifted by 90 degrees from the oscillation signal are supplied to mixers 13 and 15, respectively and they are mixed with the output signal of bandpass filter 12 there and base band signals of an in-phase component I and a quadrature component Q of the QPSK modulation signal, respectively.

The base band signals of I and Q components are converted to digital signals at an A/D converter 21 and are digitally demodulated at QPSK demodulator 22. QPSK demodulator 22 includes a carrier recovery and a clock recovery necessary for demodulation, an AGC detector and an AFC detector. The output of QPSK demodulator 22 does Viterbi decoding, deinterleaving, Reed-Solomon decoding or the like at error correction decoder 23 and corrects the error generated at a transmission route. The output signal from error correction decoder 23 is a transport stream signal multiplexed with video and sound signals encoded for band compression. Transport demultiplexer 24 separates and extracts video and sound signals encoded from the transport stream signal. The output of transport demultiplexer 24 is band expanded for each of video and sound signals and video and sound signals are reproduced.

To prevent deterioration of bit error rate due to a control signal from the microcomputer during reception, the control bus of microcomputer 50 is separated into a bus 111 to PLL synthesizer 30 and another bus 112 to QPSK demodulator 22, error correction decoder 23, etc.. Because synchronization at transport demultiplexer 24 becomes impossible when PLL synthesizer 30 malfunctions by a surge and the like due to a thunder during reception and a channel selection becomes impossible, microcomputer 50 checks a synchronization establishment signal 113 from transport demultiplexer 24, renews the control data to PLL synthesizer 30 when transport demultiplexer 24 can not synchronize and makes a channel selection again.

It is obvious that a similar effect is obtained also when the circuit is composed so that microcomputer 50 checks synchronization establishment signal 113 from transport demultiplexer 24 through control bus 112.

Thus, it is possible to prevent deterioration of receiving quality due to deterioration of noise characteristic of a local oscillation signal during a reception.

(Fifth exemplary embodiment)

A fifth exemplary embodiment of the present invention is explained below, referring to FIG. 8.

In FIG. 8, the terminal 10 is an input terminal of a first IF signal from a receiving antenna for satellite broadcast. The block 11 is a mixer for frequency-converting a desired QPSK modulation signal into a designated second IF signal. The block 12 is a bandpass filter for extracting only the designated second IF signal from the output of mixer 11. The block 16 is orthogonal detection means inputting the output of bandpass filter 12 and for obtaining base band signals of an in-phase component I and a quadrature component Q by orthogonal detection. The block 21 is

an A/D converter inputting the output of the orthogonal detection means 16 and for converting the I and Q base band signals into digital signals. The block 22 is a QPSK demodulator inputting the digitalized I and Q signals and for demodulating the inputted I and Q signals by QPSK. The block 23 is an error correction decoder. The block 24 is a transport demultiplexer for demultiplexing a transport stream in which band-compressed video and sound signals are multiplexed. The block 30 is a PLL synthesizer for generation a local oscillation signal necessary when the desired QPSK modulation signal is frequency-converted into a designated second IF signal at mixer 11. The block 17 is an orthogonal detection voltage-controlled oscillator for generating a local oscillation signal necessary for orthogonal detection. The block 50 is a microcomputer. The block 111 is a control bus from microcomputer 50 to PLL synthesizer 30. The block 112 is a control bus from microcomputer 50 to QPSK demodulator 22 and the like.

The function of a digital broadcast receiver composed like the above is explained below.

The first IF signal received through a receiving antenna for satellite broadcast is mixed with a local oscillation signal generated at PLL synthesizer 30 at mixer 11 and a desired QPSK modulation signal of the first IF signal is frequency-converted into a designated second IF signal. PLL synthesizer 30 is composed of a local oscillator 31, a prescaler 32, a programmable frequency divider 33, a phase frequency detector 34, a reference frequency signal divider 35, reference frequency signal generator 36 and a loop filter 37. The output of local oscillator 31 is inputted to programmable frequency divider 33 and frequency-divided after being frequency-divided at prescaler 32. The output of programmable frequency divider 33 is inputted to phase detector 34 and PLL synthesizer 30 is controlled so that the input signal to phase detector 34 coincides in frequency and phase with a reference frequency signal 40 obtained by dividing the output of a

reference frequency signal generator 36 at a reference frequency signal divider 35.

The local oscillation frequency F_{vco} is expressed by (eq. 4) as previously shown and a local oscillation frequency corresponding to a frequency of desired QPSK modulation signal can be obtained by varying a frequency dividing ratio N_p of programmable frequency divider 33 by microcomputer 50. The QPSK modulation signal frequency-converted into a designated second IF at mixer 11 is inputted to orthogonal detector 16 after being extracted at bandpass filter 12.

At orthogonal detector 16, an oscillation signal generated at orthogonal detection oscillator 17 with a designated second IF and a signal phase-shifted by 90 degrees from the oscillation signal are supplied to mixers 13 and 15, respectively and they are mixed with the output signal of bandpass filter 12 there and low band signals equivalent to an in-phase component I and a quadrature component Q of the QPSK modulation signal, respectively.

The low band signals equivalent to I and Q signals are converted to digital signals at an A/D converter 21 and are digitally demodulated at QPSK demodulator 22. QPSK demodulator 22 includes a carrier recovery and a clock recovery necessary for demodulation, an AGC detector and an AFC detector. The output of QPSK demodulator 22 does Viterbi decoding, deinterleaving, Reed-Solomon decoding or the like at error correction decoder 23 and corrects the error generated at a transmission route. The output signal from error correction decoder 23 is a transport stream signal multiplexed with video and sound signals encoded for band compression. Transport demultiplexer 24 demultiplexes and extracts video and sound signals encoded from the transport stream signal. The output of transport demultiplexer 24 is band expanded for each of video and sound signals and video and sound signals are reproduced.

To prevent deterioration of bit error rate due to a control signal from the microcomputer during reception, the control bus of microcomputer 50 is separated into a bus 111 to PLL synthesizer 30 and another bus 112 to QPSK demodulator 22, error correction decoder 23, etc.. Because frame synchronization at error correction decoder 23 becomes impossible when PLL synthesizer 30 malfunctions by a surge and the like due to a thunder during reception and a channel selection becomes impossible, microcomputer 50 checks a frame synchronization signal 114 from error correction decoder 23, renews the control data to PLL synthesizer 30 when error correction decoder 23 can not synchronize and makes a channel selection again.

It is obvious that a similar effect is obtained also when the circuit is composed so that microcomputer 50 checks the frame sync signal from error correction decoder 23 through control bus 112 of microcomputer 50.

Thus, it is possible to prevent deterioration of receiving quality due to deterioration of noise characteristic of a local oscillation signal during a reception.

(Sixth exemplary embodiment)

A sixth exemplary embodiment of the present invention is explained below, referring to FIG. 9.

FIG. 9 shows that an AFC function is added to prevent deterioration of bit error rate by a control bus from the microcomputer during reception in the fourth exemplary embodiment shown in FIG. 7. The blocks having the same reference numbers have similar functions to those in the fourth exemplary embodiment and their explanations are omitted.

A frequency drift occurs in the first IF signal inputted from a first IF signal input terminal 10 due to a frequency converter of a receiving antenna (not shown) for satellite

broadcast. The frequency drift of the first IF signal is generally ± 2.5 MHz and to compensate it, AFC is needed in a receiver.

Because if the AFC is done by varying a frequency dividing ratio of PLL synthesizer 30 through microcomputer 50 as shown in the prior art, the control data is sent to PLL synthesizer 30 during reception and it brings deterioration of bit error rate due to phase noise deterioration of local frequency oscillator 31, the AFC is made as follows in the sixth exemplary embodiment.

In QPSK demodulator 22, the frequency drift is detected from inputted I and Q base band signals and a frequency drift detection signal 120 is outputted as an analog voltage against the frequency drift. A voltage-controlled oscillator shown in FIG. 13 is used as an orthogonal detection oscillator 17, which is used for an orthogonal detector 16. The oscillation frequency is varied by varying the capacitance of a variable capacitance diode 302 shown in FIG. 13 through frequency drift detection signal 120 and the frequency drift of QPSK demodulator 22 is compensated.

Thus, because microcomputer 50 does not need to renew a frequency dividing ratio control signal to PLL synthesizer 30 against the frequency drift of QPSK modulated signal by doing AFC at orthogonal detector 16, it is possible to prevent deterioration of reception quality due to sending control data to PLL synthesizer 30 at AFC during reception.

(Seventh exemplary embodiment)

A seventh exemplary embodiment of the present invention is explained below, referring to FIG. 10.

FIG. 10 shows that an AFC function is added to prevent deterioration of bit error rate by a control bus from the microcomputer during reception in the fifth exemplary embodiment shown in FIG. 8. The blocks having the same reference numbers

have similar functions to those in the fifth exemplary embodiment and their explanations are omitted.

A frequency drift occurs in the first IF signal inputted from a first IF signal input terminal 10 due to a frequency converter of a receiving antenna (not shown) for satellite broadcast. The frequency drift of the first IF signal is generally ± 2.5 MHz and to compensate it, AFC is needed in a receiver.

Because if the AFC is done by varying a frequency dividing ratio of PLL synthesizer 30 through microcomputer 50 as shown in the prior art, the control data is sent to PLL synthesizer 30 during reception and it brings deterioration of bit error rate due to phase noise deterioration of local frequency oscillator 31, the AFC is made as follows in the seventh exemplary embodiment.

In QPSK demodulator 22, the frequency drift is detected from inputted I and Q base band signals and a frequency drift detection signal 120 is outputted as an analog voltage against the frequency drift. A voltage-controlled oscillator shown in FIG. 13 is used as an orthogonal detection oscillator 17, which is used for an orthogonal detector 16. The oscillation frequency is varied by varying the capacitance of a variable capacitance diode 302 shown in FIG. 13 through frequency drift detection signal 120 and the frequency drift of QPSK demodulator 22 is compensated.

Thus, because microcomputer 50 does not need to renew a frequency dividing ratio control signal to PLL synthesizer 30 against the frequency drift of QPSK modulated signal by doing AFC at orthogonal detector 16, it is possible to prevent deterioration of reception quality due to sending control data to PLL synthesizer 30 at AFC during reception.

(Eighth exemplary embodiment)

An eighth exemplary embodiment of the present invention is explained below, referring to FIG. 11.

FIG. 11 shows that an AFC function is added to prevent deterioration of bit error rate by a control bus from the microcomputer during reception in the fourth exemplary embodiment shown in FIG. 7. The blocks having the same reference numbers have similar functions to those in the fourth exemplary embodiment and their explanations are omitted.

A frequency drift occurs in the first IF signal inputted from a first IF signal input terminal 10 due to a frequency converter of a receiving antenna (not shown) for satellite broadcast. The frequency drift of the first IF signal is generally ± 2.5 MHz and to compensate it, AFC is needed in a receiver.

In the case in which the frequency drift of the first IF signal is smaller enough than the necessary bandwidth of the QPSK modulation signal (for example, the frequency drift is ± 2.5 MHz against the necessary bandwidth of 27 MHz of the QPSK modulation signal), there is no problem with only a control by orthogonal detection oscillator 17 as shown in the sixth exemplary embodiment but when the frequency drift of the first IF signal is going larger against the necessary bandwidth of the QPSK modulation signal, unless the AFC is made by PLL synthesizer 30, the bandwidth of the desired QPSK modulation signal is narrowed at a bandpass filter (SAW filter, surface acoustic wave filter) 12 for extracting a QPSK modulation signal and the reception becomes impossible. In such a case, an AFC by PLL synthesizer 30 is necessary. An AFC of the present invention is described below, which does not cause deterioration of bit error rate due to phase noise deterioration of local frequency oscillator 31 during reception even if AFC is done by varying the frequency dividing ratio of PLL synthesizer 30 by microcomputer 50.

Because synchronization of transport demultiplexer 24 becomes impossible when the frequency drift is large at channel selection and PLL synthesizer 30 malfunctions by a surge due to a thunder during reception and as a result, channel selection becomes impossible, microcomputer 50 checks a synchronization establishment signal 113 coming from transport demultiplexer 24 and control data for PLL synthesizer 30 is renewed only at this case and AFC is done at PLL synthesizer 30.

During reception, the frequency drift is detected from I and Q base band signals at QPSK demodulator 22 and a frequency drift detection signal 120 is outputted as an analogue voltage for a frequency drift. By using a voltage-controlled oscillator shown in FIG. 13 as an orthogonal detection oscillator 17 used in orthogonal detector 16 and varying the capacity of variable capacitance diode 302 shown in FIG. 13 by frequency drift detection signal 120, the oscillation frequency is varied and AFC is controlled.

Thus, because microcomputer 50 does not renew a control signal of the frequency dividing ratio for PLL synthesizer 30 during reception by doing AFC at PLL synthesizer 30 when transport demultiplexer 24 is not synchronized and by doing AFC at orthogonal detector 16 when transport demultiplexer 24 is synchronized, it becomes possible to prevent reception quality deterioration due to sending control data to PLL synthesizer 30 at AFC during reception.

A similar effect is obtained by doing AFC at PLL synthesizer 30 and orthogonal detector 16 when transport demultiplexer 24 is not synchronized and by doing AFC at only orthogonal detector 16 when transport demultiplexer 24 is synchronized,

It is obvious that a similar effect can be obtained also

when the apparatus is composed so that microcomputer 50 checks a synchronization establishment signal of transport demultiplexer 24 through control bus 112.

(Ninth exemplary embodiment)

A ninth exemplary embodiment of the present invention is explained below, referring to FIG. 12.

FIG. 12 shows that an AFC function is added to prevent deterioration of bit error rate by a control bus from the microcomputer during reception in the fifth exemplary embodiment shown in FIG. 8. The blocks having the same reference numbers have similar functions to those in the fifth exemplary embodiment and their explanations are omitted.

A frequency drift occurs in the first IF signal inputted from a first IF signal input terminal 10 due to a frequency converter of a receiving antenna (not shown) for satellite broadcast. The frequency drift of the first IF signal is generally ± 2.5 MHz and to compensate it, AFC is needed in a receiver.

In the case in which the frequency drift of the first IF signal is smaller enough than the necessary bandwidth of the QPSK modulation signal (for example, the frequency drift is ± 2.5 MHz against the necessary bandwidth of 27 MHz of the QPSK modulation signal), there is no problem with only a control by orthogonal detection oscillator 17 as shown in the seventh exemplary embodiment but when the frequency drift of the first IF signal is going larger against the necessary bandwidth of the QPSK modulation signal, unless the AFC is made by PLL synthesizer 30, the bandwidth of the desired QPSK modulation signal is narrowed at a bandpass filter 12 for extracting a QPSK modulation signal and the reception becomes impossible.

In such a case, an AFC by PLL synthesizer 30 is

necessary. An AFC of the present invention is described below, which does not cause any picture quality deterioration due to phase noise deterioration of local frequency oscillator 31 during reception even if an AFC is done by varying the frequency dividing ratio of PLL synthesizer 30 by microcomputer 50.

Because frame synchronization of error correction decoder 23 becomes impossible when PLL synthesizer 30 malfunctions by a surge due to a thunder during reception and as a result, channel selection becomes impossible, microcomputer 50 checks a frame sync signal 114 coming from error correction decoder 23 at channel selection and control data for PLL synthesizer 30 is renewed only at this case and AFC is done at PLL synthesizer 30.

During reception, the frequency drift is detected from I and Q base band signals at QPSK demodulator 22 and a frequency drift detection signal 120 is outputted as an analog voltage for a frequency drift. By using a voltage-controlled oscillator shown in FIG. 13 as an orthogonal detection oscillator 17 used in orthogonal detector 16 and varying the capacity of variable capacitance diode 302 shown in FIG. 13 by frequency drift detection signal 120, the oscillation frequency is varied and AFC is controlled.

Thus, because microcomputer 50 does not renew a control signal of the frequency dividing ratio for PLL synthesizer 30 during reception by doing AFC at PLL synthesizer 30 when error correction decoder 23 is not synchronized and by doing AFC at orthogonal detector 16 when error correction decoder 23 is synchronized, it becomes possible to prevent reception quality deterioration due to sending control data to PLL synthesizer 30 at AFC during reception.

A similar effect is obtained by doing AFC at PLL synthesizer 30 and orthogonal detector 16 when error correction decoder 23 is not synchronized and by doing AFC at only orthogonal

detector 16 when error correction decoder 23 is synchronized.

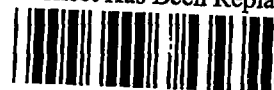
It is obvious that a similar effect can be obtained also when the apparatus is composed so that microcomputer 50 checks a frame synchronization establishment signal of error correction decoder 23 through control bus 112.

According to a digital broadcast receiver in accordance with the first to third exemplary embodiments of the present invention, because the phase noise characteristic of a local oscillation signal is improved, keeping an AFC accuracy, the bit error rate characteristic as a receiver can be kept good.

According to a digital broadcast receiver in accordance with the fourth to ninth exemplary embodiments of the present invention, it is possible to prevent deterioration of a bit error rate and a reception quality by that the noise characteristic of a local oscillation signal deteriorates due to control data coming from a microcomputer during reception.

The invention may be embodied in other specific form without departing from the spirit or essential characteristics thereof. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

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**What is Claimed:**

1. A digital broadcast receiver for receiving a digital modulation signal comprising:

channel selection means inputting said digital modulation signal of a radio frequency band and for frequency converting a desired digital modulation signal into a signal having a designated intermediate frequency;

oscillation means for generating a local oscillation signal used for a frequency conversion at said channel selection means;

oscillation frequency control means for controlling a frequency of the local oscillation signal of said oscillation means;

phase noise characteristic control means for improving a phase noise characteristic of the local oscillation signal generated at said oscillation means;

filter means for extracting said intermediate frequency signal produced at said channel selection means;

orthogonal detection means for orthogonally detecting the intermediate frequency signal extracted at said filter means;

A/D conversion means for converting the analog output of said orthogonal detection means into a digital signal; and

digital demodulation means for digitally demodulating the output of said A/D conversion means.

2. A digital broadcast receiver as recited in claim 1, wherein

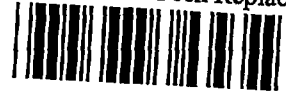
said phase noise characteristic control means does AFC (automatic frequency control) continuously by an automatic frequency control signal expressing the frequency drift of the receiving signal detected at said digital demodulation means and the reference frequency of phase detection of the PLL synthesizer comprising said oscillation means and said oscillation frequency control means is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced by making an open loop gain of PLL (phase locked loop) synthesizer



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means large.

3. A digital broadcast receiver as recited in claim 1, wherein

said phase noise characteristic control means employs an exclusive control bus as a control bus in which a control signal of said oscillation frequency control means is transmitted and said exclusive control bus is separated from a control bus in which a control signal for the other devices including said digital decoding means is transmitted.

4. A digital broadcast receiver as recited in claim 1, wherein

the control by said oscillation frequency control means is restricted only when a channel is selected or a demodulation signal is not synchronized.

5. A digital broadcast receiver comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK (quaternary phase-shift keying) modulation signal; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

AFC is continuously done at said orthogonal detection means; and

a reference frequency for comparison of a phase detection at said PLL synthesizer means is increased as high as the phase noise near an oscillation frequency of a local oscillation signal can be reduced.

6. A digital broadcast receiver comprising:

frequency conversion means inputting QPSK modulation signals in a radio frequency band and for frequency-converting a desired QPSK modulation signal included in the QPSK modulation signals into a designated intermediate frequency signal;

bandpass filter means for extracting said designated



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intermediate frequency signal;

orthogonal detection means inputting the output of said bandpass filter means, obtaining base band signals of an in-phase component I and a quadrature component Q by an orthogonal detection, and having an AFC function continuously compensating a frequency drift of the receiving signal;

A/D converter means inputting an output of said orthogonal detection means and for converting analog base band signals of I and Q components to digital signals;

QPSK demodulation means for doing QPSK demodulation digitally; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

a reference frequency for comparison of the phase detection of said PLL synthesizer means is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

7. A digital broadcast receiver comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for generating a local oscillation signal for channel selection; and

QPSK demodulation means for digitally doing QPSK demodulation; and wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of the phase detection of said PLL synthesizer means is obtained by frequency dividing a clock signal recovered at said QPSK demodulation means; and

the comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

8. A digital broadcast receiver comprising:



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frequency conversion means inputting QPSK modulation signals in a radio frequency band and for frequency-converting a desired QPSK modulation signal included in the QPSK modulation signals into a designated intermediate frequency signal;

bandpass filter means for extracting said designated intermediate frequency signal;

orthogonal detection means inputting the output of said bandpass filter means, obtaining base band signals of an in-phase component I and a quadrature component Q by an orthogonal detection, and having an AFC function continuously compensating a frequency drift of the receiving signal;

A/D converter means inputting an output of said orthogonal detection means and for converting analog base band signals of I and Q components to digital signals;

QPSK demodulation means for doing QPSK demodulation digitally; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

a comparison reference frequency signal for phase detection of said PLL synthesizer means is obtained by frequency dividing a clock signal recovered at said QPSK demodulation means; and

the comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

9. A digital broadcast receiver comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for generating a local oscillation signal for channel selection;

QPSK demodulation means for digitally doing QPSK demodulation;

demultiplex means for demultiplexing encoded and multiplexed video and sound signals; and wherein

continuous AFC is done at said orthogonal detection





means;

a comparison reference frequency signal of the phase detection of said PLL synthesizer means is obtained by frequency dividing a system clock signal of said demultiplex means; and

the comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

10. A digital broadcast receiver comprising:

frequency conversion means inputting QPSK modulation signals in a radio frequency band and for frequency-converting a desired QPSK modulation signal included in the QPSK modulation signals into a designated intermediate frequency signal;

bandpass filter means for extracting said designated intermediate frequency signal;

orthogonal detection means inputting the output of said bandpass filter means, obtaining base band signals of an in-phase component I and a quadrature component Q by a orthogonal detection, and having an AFC function continuously compensating a frequency drift of the receiving signal;

A/D converter means inputting an output of said orthogonal detection means and for converting analog base band signals of I and Q components to digital signals;

QPSK demodulation means for doing QPSK demodulation digitally;

error correction means inputting the output of said QPSK demodulation means and for correcting an error generated on a transmission route;

demultiplex means inputting the output of said error correction means and for demultiplexing encoded and multiplexed video and sound signals; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

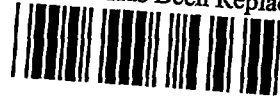
a comparison reference frequency signal of the phase



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detection of said PLL synthesizer means is obtained by frequency dividing a system clock signal of said demultiplex means; and the comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

11. A digital broadcast receiver for receiving a QPSK modulation signal comprising:

channel selection means selecting a desired QPSK modulation signal;

microcomputer means for controlling said channel selection means; and wherein

renewal of the channel selection data transmitted from said microcomputer means to said channel selection means is done only when a channel selection is requested and when a synchronization of demultiplex means for demultiplexing encoded and multiplexed video and sound signals is established, using an exclusive control bus as a control bus which a control signal is transmitted from said microcomputer means to said channel selection means and separating from the other control buses which the other control signals for the other devices including digital demodulating means are transmitted.

12. A digital broadcast receiver comprising:

frequency conversion means inputting QPSK modulation signals in a radio frequency band and for frequency-converting a desired QPSK modulation signal into a designated intermediate frequency signal;

bandpass filter means for extracting said designated intermediate frequency signal;

orthogonal detection means inputting the output of said bandpass filter means, obtaining base band signals of an in-phase component I and a quadrature component Q by an orthogonal detection, and having an AFC function continuously compensating a frequency drift of the receiving signal;



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A/D converter means inputting an output of said orthogonal detection means and for converting analog base band signals of I and Q components to digital signals;

QPSK demodulation means for doing QPSK demodulation digitally;

error correction decoding means inputting the output of said QPSK demodulation means and for correcting error generated on the transmission route;

demultiplex means inputting the output of said error correction decoding means and for demultiplexing encoded and multiplexed video and sound signals; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

renewal of the channel selection data transmitted from said microcomputer means to said PLL synthesizer means is done only when a channel selection is required and when a synchronization of demultiplex means for demultiplexing encoded and multiplexed video and sound signals is not established, using an exclusive control bus as a control bus which a control signal is transmitted from said microcomputer means to said PLL synthesizer means and separating from the other control buses which the other control signals for the other devices including digital demodulating means are transmitted.

13. A digital broadcast receiver for receiving a QPSK modulation signal comprising:

channel selection means selecting a desired QPSK modulation signal;

microcomputer means for controlling said channel selection means; and wherein

renewal of the channel selection data transmitted from said microcomputer means to said channel selection means is done only when a channel selection is requested and when a synchronization of error correction means for correcting a bit error generated on a transmission route is not established, using an exclusive control bus as a control bus which a control

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signal is transmitted from said microcomputer means to said channel selection means and separating from the other control buses which the other control signals for the other devices including digital demodulating means are transmitted.

14. A digital broadcast receiver comprising:

frequency conversion means inputting QPSK modulation signals in a radio frequency band and for frequency-converting a desired QPSK modulation signal into a designated intermediate frequency signal;

bandpass filter means for extracting said designated intermediate frequency signal;

orthogonal detection means inputting the output of said bandpass filter means, obtaining base band signals of an in-phase component I and a quadrature component Q by a orthogonal detection, and having an AFC function continuously compensating a frequency drift of the receiving signal;

A/D converter means inputting an output of said orthogonal detection means and for converting analog base band signals of I and Q components to digital signals;

QPSK demodulation means for doing QPSK demodulation digitally;

error correction decoding means inputting the output of said QPSK demodulation means and for correcting error generated on the transmission route;

demultiplex means inputting the output of said error correction decoding means and for demultiplexing encoded and multiplexed video and sound signals; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

renewal of the channel selection data transmitted from said microcomputer means to said PLL synthesizer means is done only when a channel selection is requested and when a synchronization of said error correction means is not established, using an exclusive control bus as a control bus which a control signal is transmitted from said microcomputer means to said PLL





synthesizer means and separating from the other control buses which the other control signals for the other devices including digital demodulating means are transmitted.

15. A digital broadcast receiver as recited in claim 11 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

continuous AFC is done at said orthogonal detection means and

a comparison reference frequency of phase detection at said PLL synthesizer means is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

16. A digital broadcast receiver as recited in claim 12, wherein

continuous AFC is done at said orthogonal detection means and

a comparison reference frequency of phase detection at said PLL synthesizer means for channel selection is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

17. A digital broadcast receiver as recited in claim 13 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal; and

PLL synthesizer means for generating a local oscillation signal for channel selection; and wherein

continuous AFC is done at said orthogonal detection means and

a comparison reference frequency of phase detection at said PLL synthesizer means is made as high as the phase noise near



the oscillation frequency of a local oscillation signal can be reduced.

18. A digital broadcast receiver as recited in claim 14 wherein

continuous AFC is done at said orthogonal detection means and

a comparison reference frequency of phase detection at said PLL synthesizer means for channel selection is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

19. A digital broadcast receiver as recited in claim 11 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for generating a local oscillation signal for channel selection; and

QPSK demodulation means for digitally doing QPSK demodulation; and wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of the phase detection at said PLL synthesizer means is obtained by frequency dividing a clock signal reproduced at said QPSK demodulation means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

20. A digital broadcast receiver as recited in claim 12, wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of the phase



detection at said PLL synthesizer means for channel selection is obtained by frequency dividing a clock signal reproduced at said QPSK demodulation means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

21. A digital broadcast receiver as recited in claim 13 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for generating a local oscillation signal for channel selection; and

QPSK demodulation means for digitally doing QPSK demodulation; and wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of phase detection at said PLL synthesizer means is obtained by frequency dividing a clock signal recovered at said QPSK demodulation means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

22. A digital broadcast receiver as recited in claim 14, wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of phase detection at said PLL synthesizer means for channel selection is obtained by frequency dividing a clock signal recovered at said QPSK demodulation means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.



23. A digital broadcast receiver as recited in claim 11 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for generating a local oscillation signal for channel selection;

QPSK demodulation means for digitally doing QPSK demodulation; and

demultiplex means for demultiplexing encoded and multiplexed video and sound signals; and wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of phase detection at said PLL synthesizer means is obtained by frequency dividing a system clock signal of said demultiplex means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

24. A digital broadcast receiver as recited in claim 12, wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of phase detection at said PLL synthesizer means for channel selection is obtained by frequency dividing a system clock signal of said demultiplex means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

25. A digital broadcast receiver as recited in claim 13 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;



PLL synthesizer means for generating a local oscillation signal for channel selection;

QPSK demodulation means for digitally doing QPSK demodulation; and

demultiplex means for demultiplexing encoded and multiplexed video and sound signals; and wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of phase detection at said PLL synthesizer means is obtained by frequency dividing a system clock signal of said demultiplex means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

26. A digital broadcast receiver as recited in claim 14, wherein

continuous AFC is done at said orthogonal detection means;

a comparison reference frequency signal of phase detection at said PLL synthesizer means for channel selection is obtained by frequency dividing a system clock signal of said demultiplex means; and

said comparison reference frequency is made as high as the phase noise near the oscillation frequency of a local oscillation signal can be reduced.

27. A digital broadcast receiver as recited in claim 11 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for generating a local oscillation signal for channel selection; and

demultiplex means for demultiplexing encoded and multiplexed video and sound signals; and wherein

AFC is done at said PLL synthesizer means and said



orthogonal detection means when synchronization of said demultiplex means is not established; and

continuous AFC is done at said orthogonal detection means when synchronization of said demultiplex means is established.

28. A digital broadcast receiver as recited in claim 12, wherein

AFC is done at said PLL synthesizer means for a channel selection and said orthogonal detection means when synchronization of said demultiplex means is not established; and

AFC is done at said orthogonal detection means when synchronization of said demultiplex means is established.

29. A digital broadcast receiver as recited in claim 13 further comprising:

orthogonal detection means for orthogonally detecting a channel selected QPSK modulation signal;

PLL synthesizer means for channel selection; and

error correction decoding means for correcting error generated on a transmission route; and wherein

AFC is done at said PLL synthesizer means and said orthogonal detection means when synchronization of said error correction decoding means is not established; and

AFC is done at said orthogonal detection means when synchronization of said error correction decoding means is established.

30. A digital broadcast receiver as recited in claim 14, wherein

AFC is done at said PLL synthesizer means for a channel selection and said orthogonal detection means when synchronization of said error correction decoding means is not established; and

AFC is done at said orthogonal detection means when synchronization of said error correction decoding means is established.

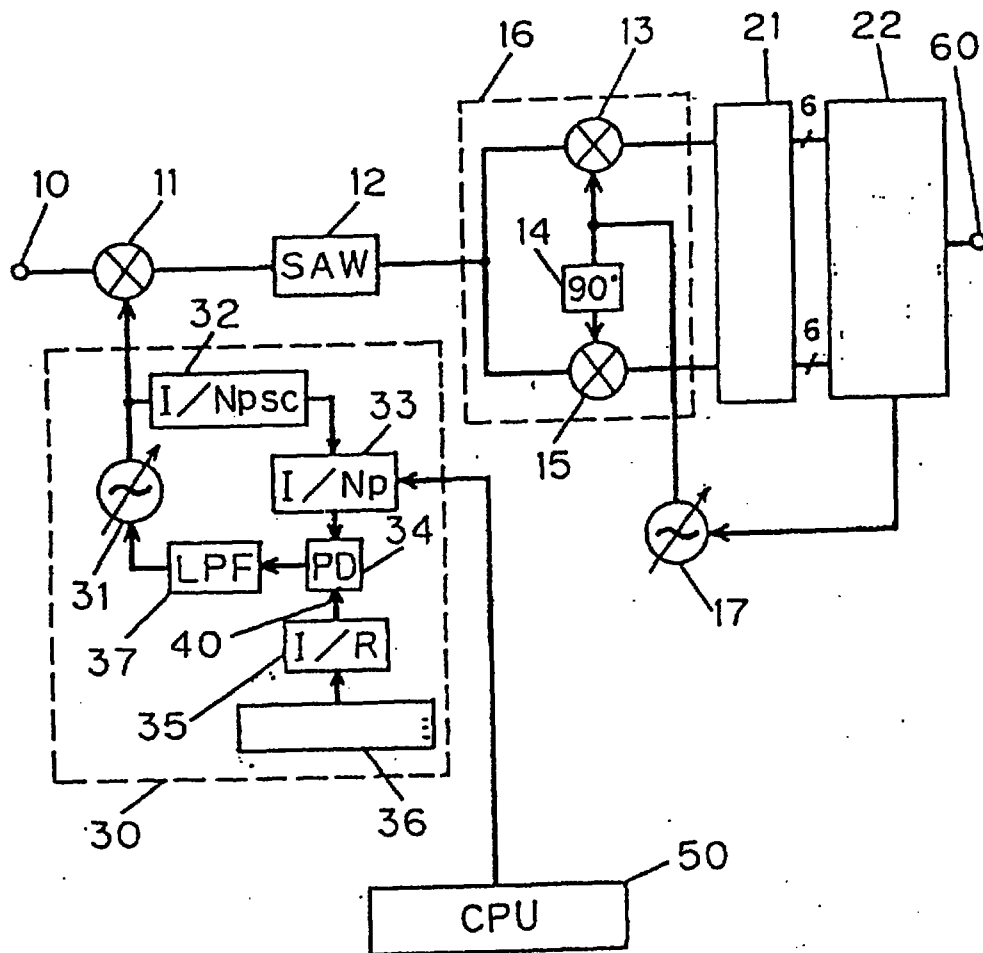
ABSTRACT

TITLE OF INVENTION: DIGITAL BROADCAST RECEIVER

A digital broadcast receiver for receiving a digital modulation signal of the present invention includes channel selection means inputting a digital modulation signal of a radio frequency band and frequency converting a desired digital modulation signal into a designated intermediate frequency signal; oscillation means for generating a local oscillation signal used for frequency conversion at the channel selection means; oscillation frequency control means for controlling a frequency of the local oscillation signal at the oscillation means; phase noise characteristic control means for improving a phase noise characteristic of the local oscillation signal generated at the oscillation means; filter means for extracting the intermediate frequency signal selected at channel selection means; orthogonal detection means for orthogonally detecting the intermediate frequency signal extracted at the filter means; A/D converter means for converting the analog output of the orthogonal detection means into a digital signal; and digital demodulation means for digitally demodulating the output of the A/D converter means; and makes a high performance digital reception possible which can improve an AFC function by the channel selection means and can improve a bit error rate at the same time.

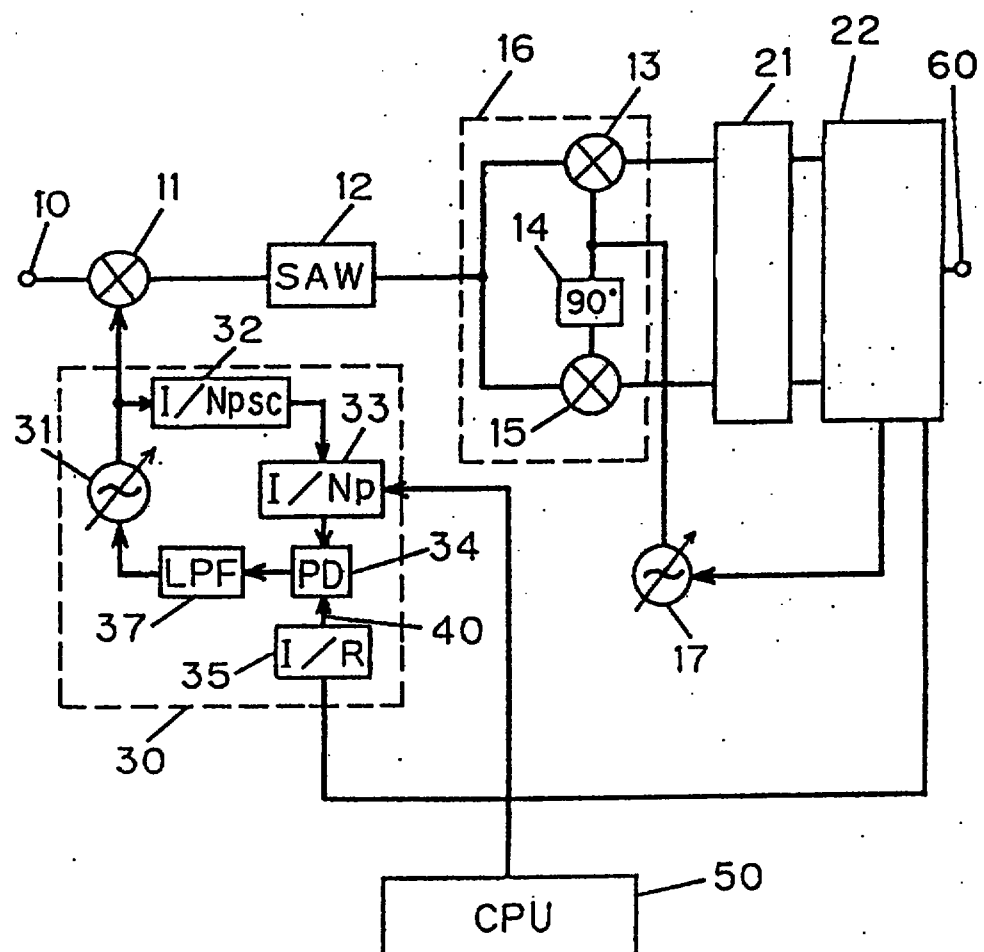
Figure 1.

[FIG. 1]

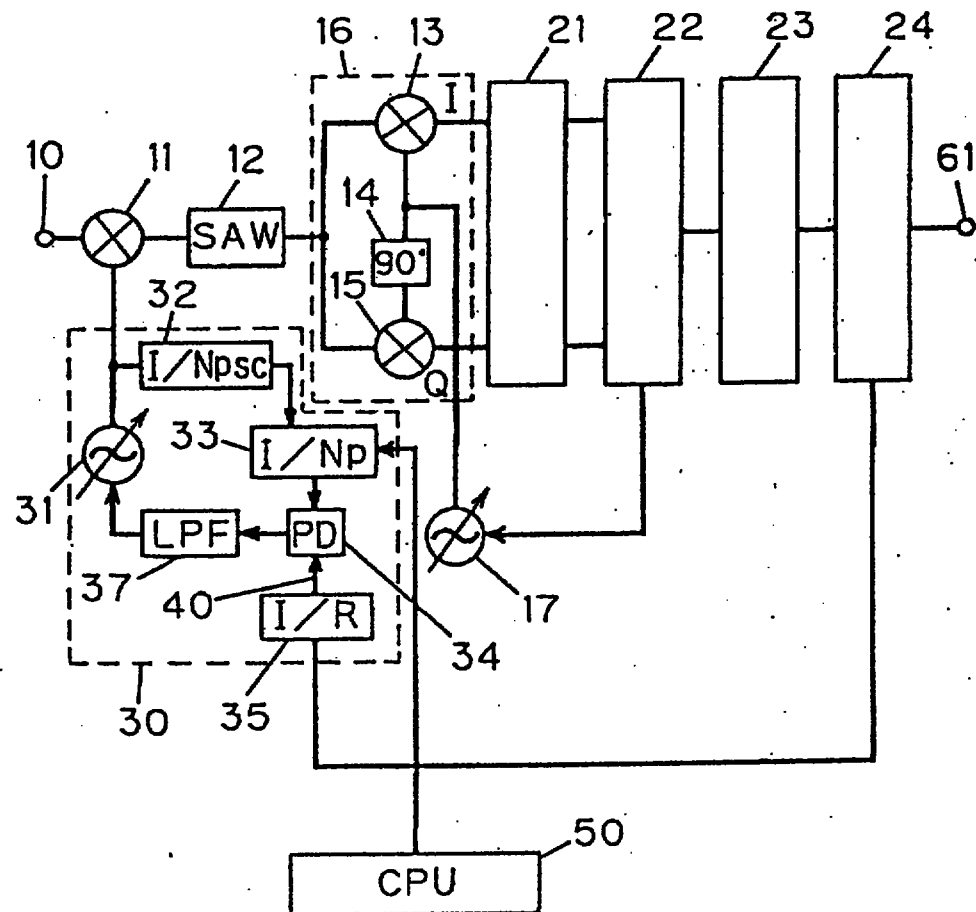


- 10...first IF signal input terminal
- 11...mixer
- 12...bandpass filter
- 13, 15...mixer
- 14...90 degree phase shifter
- 16...orthogonal detector
- 17...orthogonal detection (voltage-controlled) oscillator
- 21...A/D converter
- 22...QPSK demodulator
- 50...microcomputer (CPU)
- 60...QPSK demodulator output terminal
- 30...PLL synthesizer
- 31...local oscillator
- 32...prescaler
- 33...programmable frequency divider
- 34...phase detector
- 35...reference frequency divider
- 36...reference frequency signal generator
- 37...loop filter

[FIG. 2]

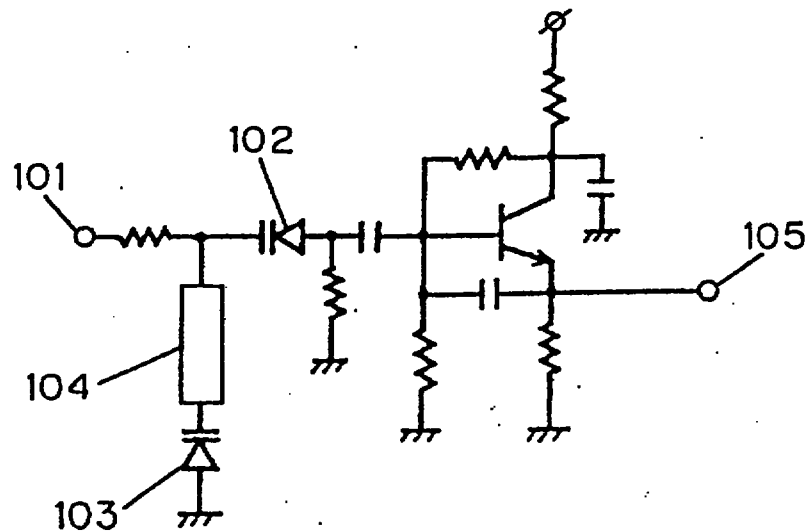


[FIG. 3]



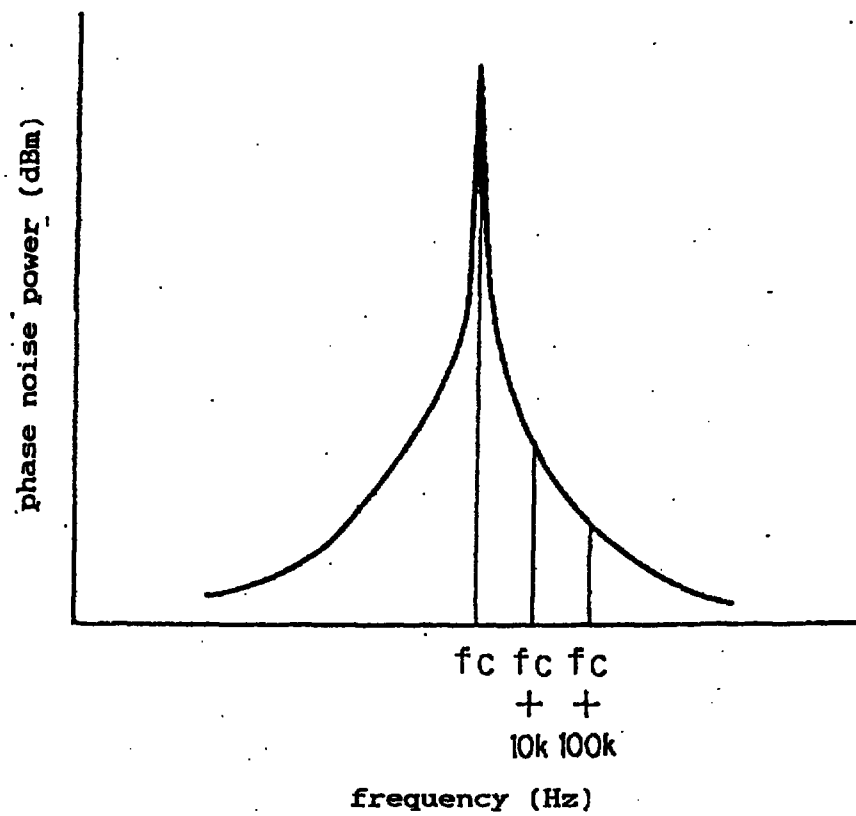
- 23...error correction decoder
- 24...demultiplexer
- 61...transport stream output terminal

[FIG. 4]

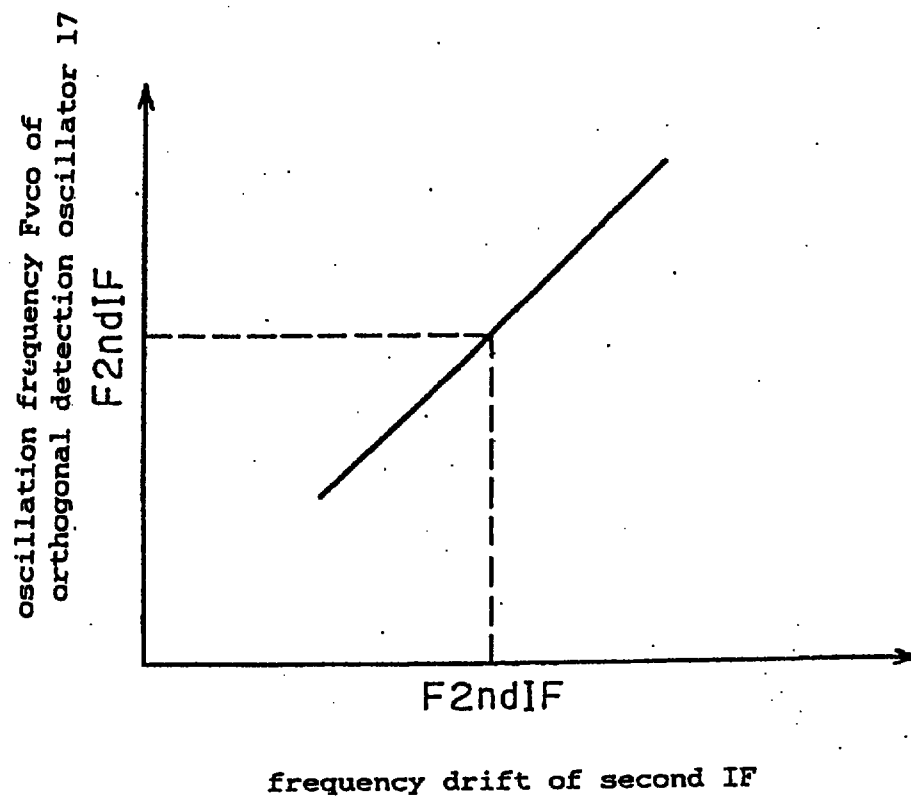


- 101...control voltage input terminal
- 102, 103...variable capacitance diode
- 104...microstrip line
- 105...local oscillation signal output terminal

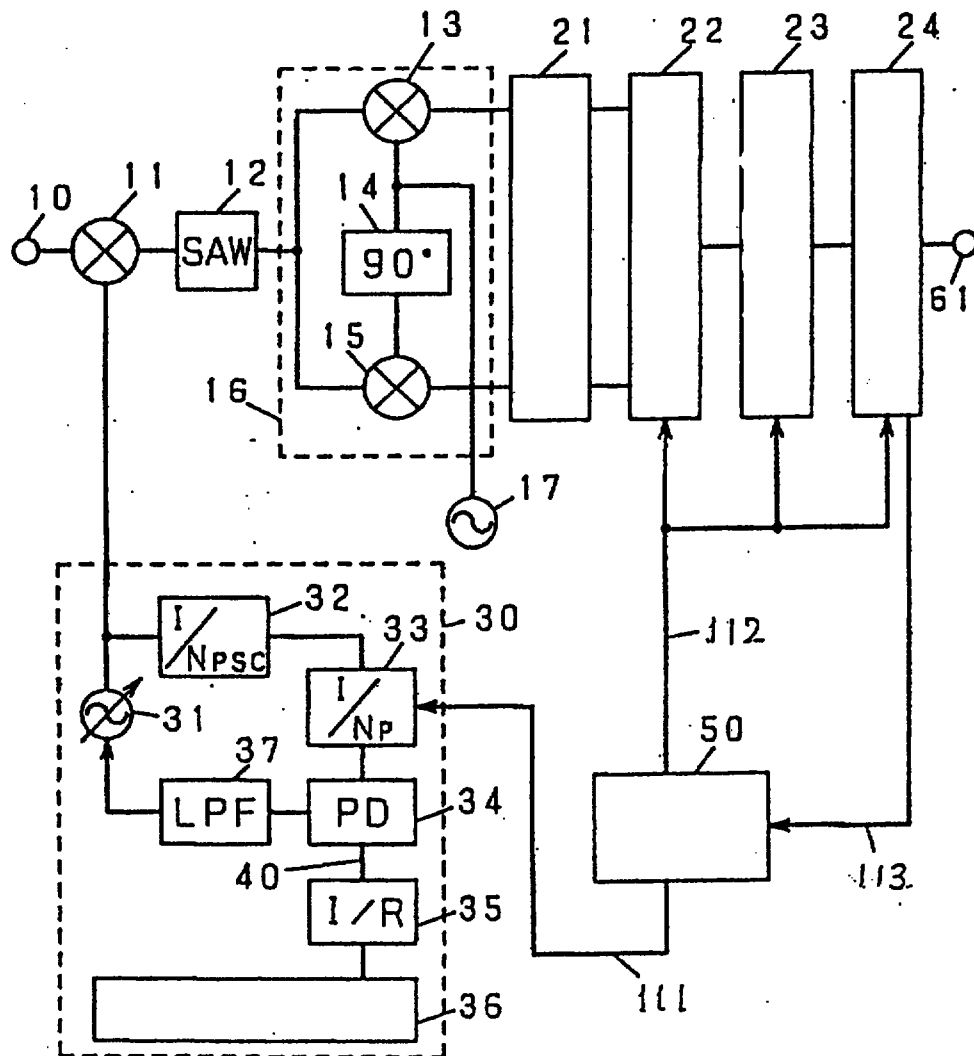
[FIG. 5]



[FIG. 6]



[FIG. 7]

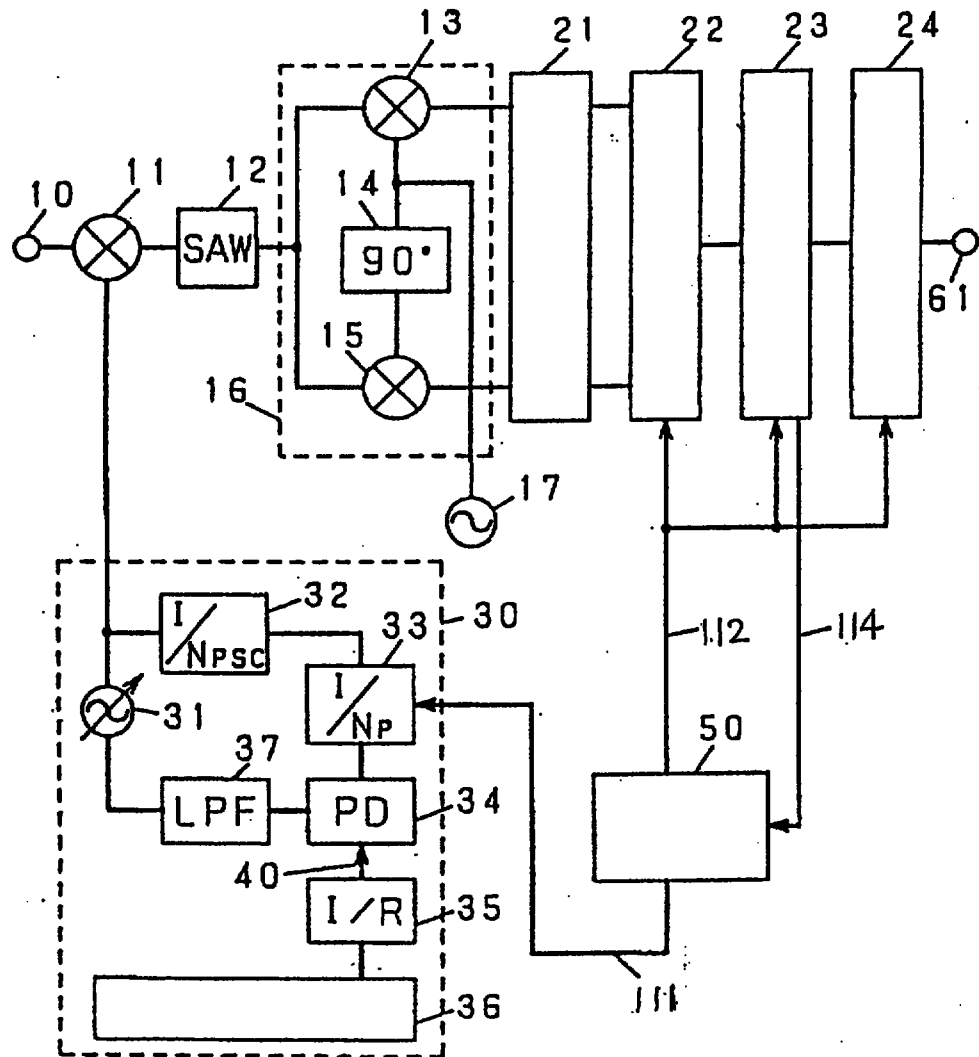


24...transport demultiplexer

111, 112...control bus

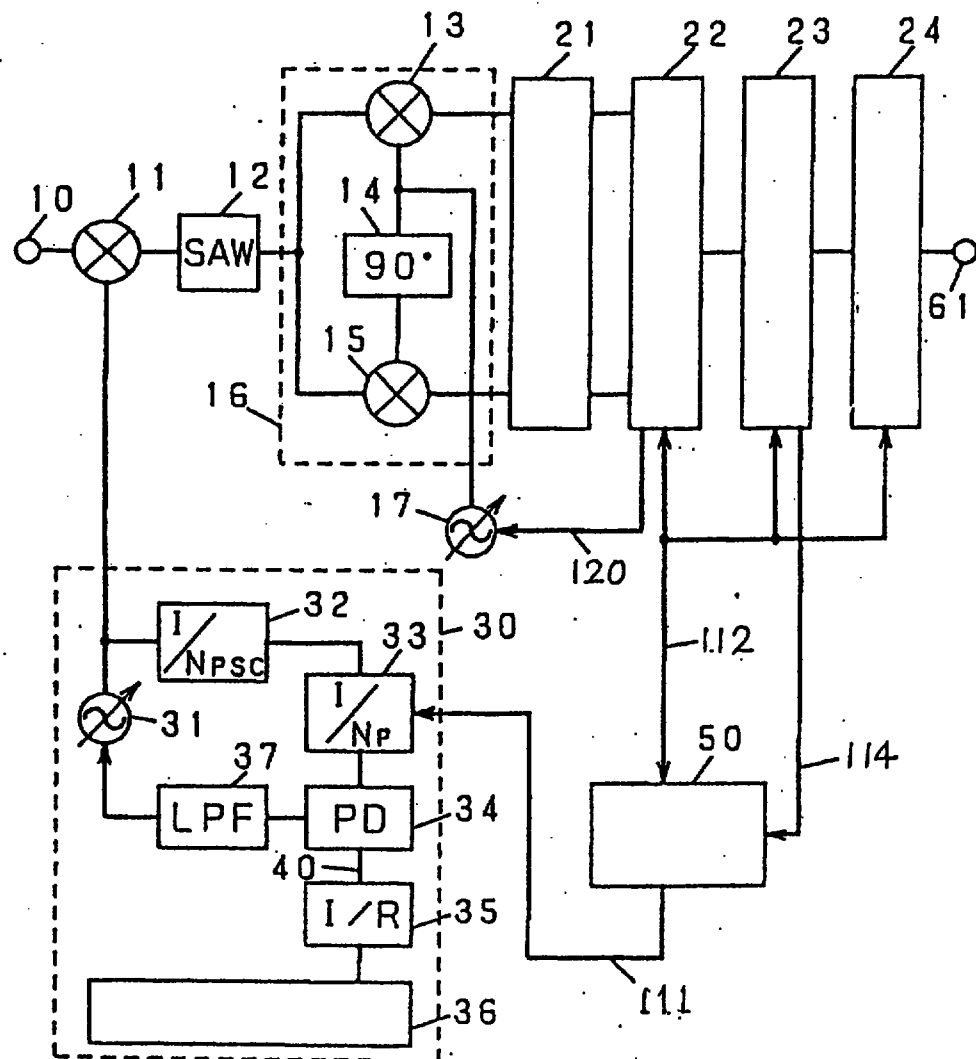
113...synchronization establishment signal

[FIG. 8]

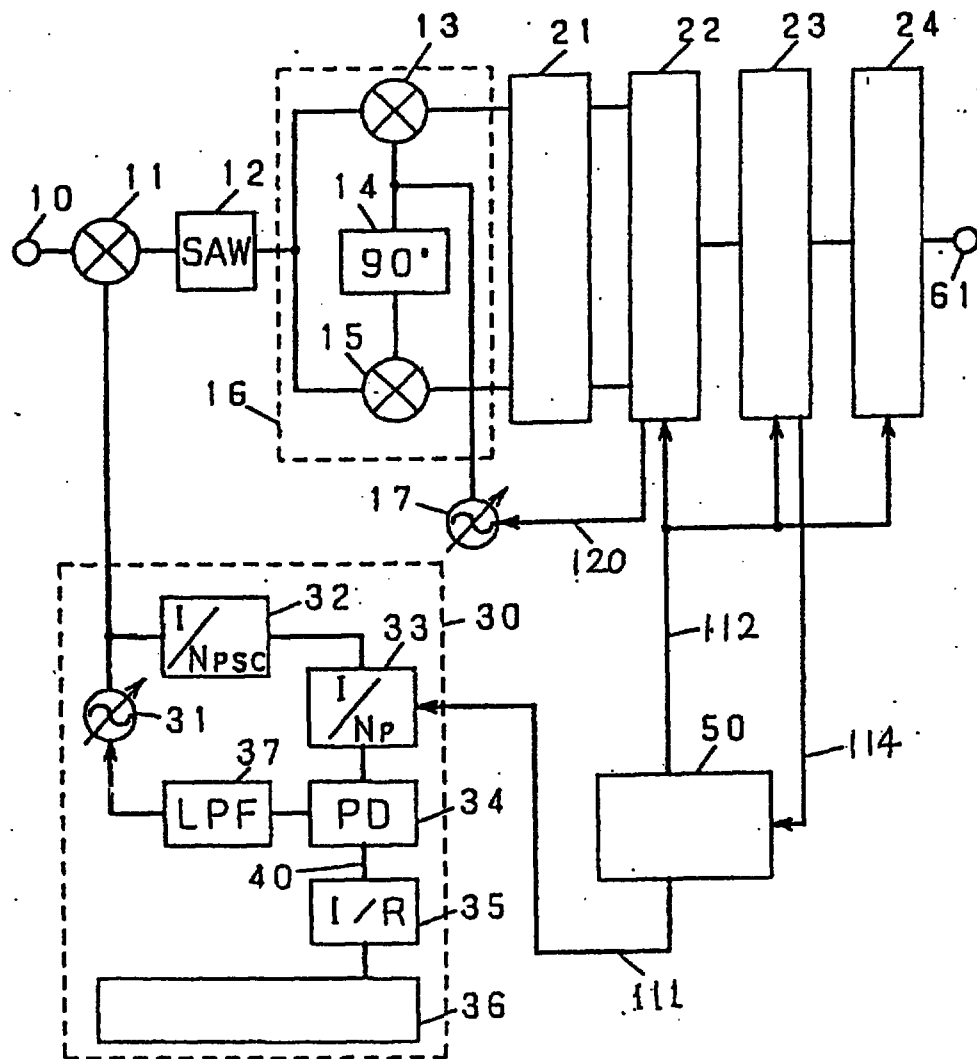


114...frame sync signal

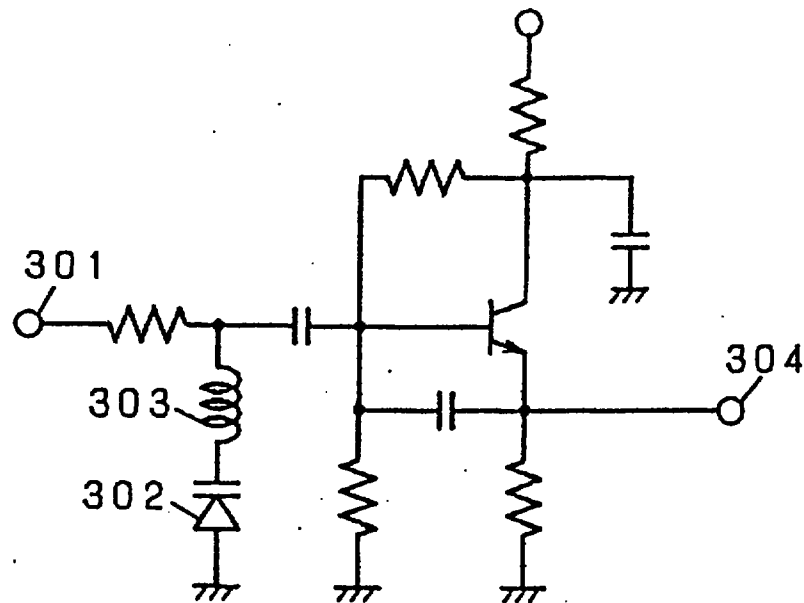
[FIG. 10]



[FIG. 12]



[FIG. 13]



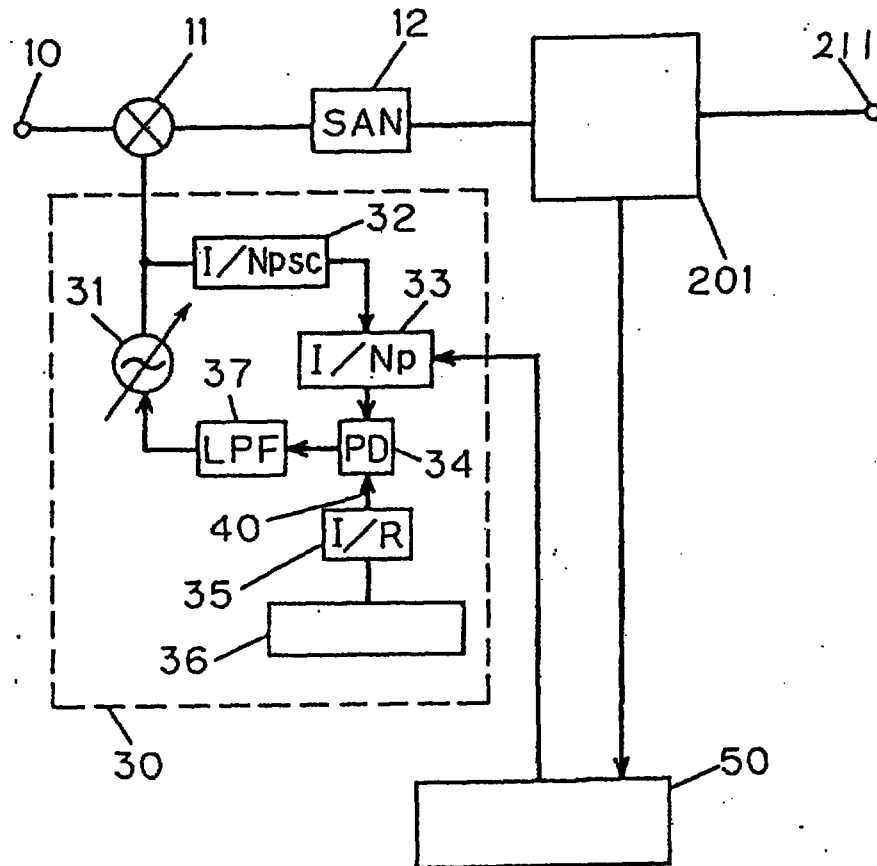
310...frequency drift detection signal input terminal

302...variable capacitance diode

303...inductance

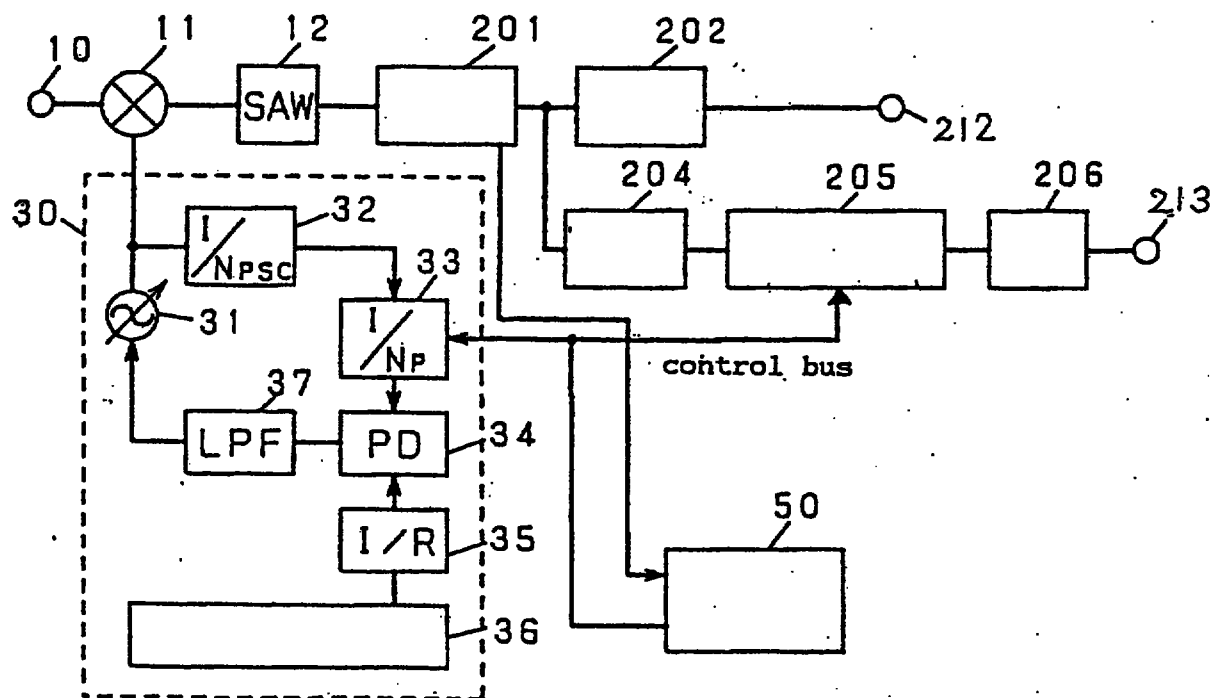
304...orthogonal detection oscillation signal output terminal

[FIG. 14]

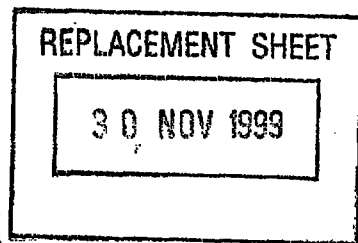
PRIOR ART

- 10...first IF signal input terminal
- 11...mixer
- 12...bandpass filter
- 50...CPU
- 201...FM demodulator
- 211...FM demodulator output terminal
- 30...PLL synthesizer
- 31...local oscillator
- 32...prescaler
- 33...programmable frequency divider
- 34...phase detector
- 35...reference frequency divider
- 36...reference frequency signal generator
- 37...loop filter
- 40...reference frequency signal

[FIG. 15]

PRIOR ART

- 201...FM demodulator
- 202...video signal processor
- 204...QPSK demodulator
- 205...PCM sound signal processor
- 206...D/A converter
- 212...video output terminal
- 213...sound output terminal



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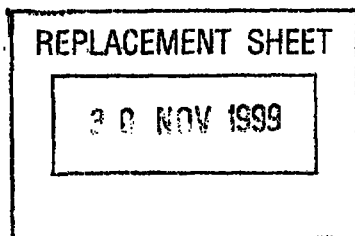
such as making a reference frequency $f_{r/R}$ of the PLL synthesizer for phase frequency detection large.

In the case of a receiver receiving a digitally modulated signal such as QPSK modulation, when a control data is inputted from a microcomputer to a PLL synthesizer, the control data gives an interference to the local oscillator circuit for channel selection and the noise characteristic of the local oscillation signal rapidly deteriorates. Thus, the noise characteristic of the local oscillation signal gives an influence to the bit error rate.

10 By using a control bus from the microcomputer to the PLL synthesizer in common with a control bus of the other signal processing LSIs, when the other signal processing LSIs are controlled during reception, the control data is inputted also to the PLL synthesizer and whenever AFC during reception is made in the PLL synthesizer or the control data is periodically renewed against malfunction of the PLL synthesizer due to a surge or the like,
15 noise in the local oscillation signal becomes big and deteriorates the bit error rate and the quality of reception. This is a problem.

Summary of the Invention

20 In accordance with the present invention, there is provided a receiver for receiving a first modulated digital signal, the receiver comprising:
a first local oscillator for generating a first local oscillation signal;
a mixer for converting the first modulated digital signal into a second modulated digital signal having a predetermined intermediate frequency based on the first local
25 oscillation signal;
a filter for extracting an intermediate frequency signal from the second modulated digital signal;
a second local oscillator, responsive to an AFC (Automatic Frequency Control) signal, for generating a second local oscillation signal having an oscillation frequency;
30 an orthogonal detector for detecting a signal component based on the second local oscillation signal;
an A/D (analogue-to-digital) converter for converting the signal component into a



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digital signal; and

a digital demodulator, having an AFC (Automatic Frequency Control) detector, for digitally demodulating the digital signal, and for producing the AFC signal.

5 In another aspect, there is provided a digital receiver comprising:

an orthogonal detector, having an oscillator, for orthogonally detecting a selected QPSK (quaternary phase-shift keying) modulated signal; and

a PLL (phase-locked loop) for selecting a modulated signal by generating a local oscillation signal based on phase detection and comparison with a reference frequency signal,

10 wherein AFC (automatic frequency control) of the oscillator is continuously performed at said orthogonal detector.

In another aspect, there is provided a digital receiver comprising:

a PLL for generating a local oscillation signal based on phase detection and
15 comparison with a reference frequency signal;

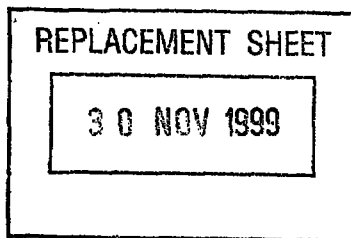
a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into a first intermediate frequency signal based on the local oscillation signal;

a bandpass filter for extracting a second intermediate frequency signal from the first intermediate frequency signal;

20 an orthogonal detector, responsive to an AFC (Automatic Frequency Control) signal, for detecting an in-phase component signal I and a quadrature component signal Q of the second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;

an A/D converter for converting the in-phase component signal I and the quadrature
25 component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal; and

a QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal, and for producing the AFC (Automatic Frequency Control).



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In another aspect, there is provided a digital receiver comprising:

a PLL for generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;

a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into
5 a first intermediate frequency signal based on the local oscillation signal;

a bandpass filter for extracting a second intermediate frequency signal from the first intermediate frequency signal;

orthogonal detector for detecting an in-phase component I and a quadrature component Q of the second intermediate frequency signal and for continuously compensating a frequency
10 drift of the second intermediate frequency signal;

an A/D converter for converting the in-phase component signal I and the quadrature component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal;

QPSK demodulator for digitally demodulating the digital in-phase component signal
15 and the digital quadrature component signal and for producing an encoded and multiplexed signal;

error correction means for correcting transmission errors of the encoded and multiplexed signal; and

a demultiplexer for demultiplexing the output of said error correction means and for
20 producing a system clock signal, wherein the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the system clock signal produced by said demultiplexer.

In another aspect, there is provided a digital receiver comprising:

25 a PLL for generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;

a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into a first intermediate frequency signal based on the local oscillation signal;

a bandpass filter for extracting a second intermediate frequency signal from the first
30 intermediate frequency signal;

orthogonal detector for detecting an in-phase component I and a quadrature component Q of the second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;

an A/D converter for converting the in-phase component signal I and the quadrature component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal;

QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal and for producing an encoded and multiplexed signal;

10 error correction means for correcting transmission errors of the encoded and multiplexed signal;

a demultiplexer for demultiplexing the output of said error correction means and for generating a synchronization signal;

a microcomputer for controlling the PLL based on the synchronization signal; and

15 a control bus for relaying a control signal from the microcomputer to the PLL,

wherein the microcomputer resets the PLL by relaying the control signal via the control bus when the demultiplexer indicates a loss of synchronization via the synchronization signal.

20 In another aspect, there is provided a digital receiver comprising:

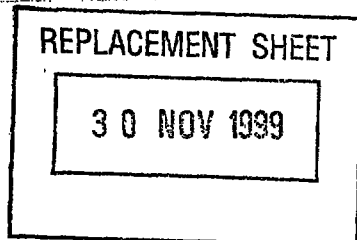
a PLL for generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;

a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into a first intermediate frequency signal based on the local oscillation signal;

25 a bandpass filter for extracting a second intermediate frequency signal from the first intermediate frequency signal;

orthogonal detector for detecting an in-phase component I and a quadrature component Q of the second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;

30 an A/D converter for converting the in-phase component signal I and the quadrature



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component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal;

QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal and for producing an encoded and multiplexed
5 signal;

error correction means for correcting transmission errors of the encoded and multiplexed signal, for outputting a corrected multiplexed signal, and for generating a synchronization signal;

a demultiplexer for demultiplexing the corrected multiplexed signal of said error
10 correction means;

a microcomputer for controlling the PLL based on the synchronization signal; and

a control bus for relaying a control signal from the microcomputer to the PLL,

wherein the microcomputer resets the PLL by relaying the control signal via the control bus when the error correction means indicates a loss of synchronization via the
15 synchronization signal.

In another aspect, there is provided a receiver for receiving a QPSK modulated signal, the receiver comprising:

a demodulator for demodulating the QPSK modulated signal and producing an encoded
20 and multiplexed signal;

a demultiplexer for demultiplexing the encoded and multiplexed signal and for generating a synchronization signal;

a microcomputer for controlling the demodulator based on the synchronization signal;

a control bus for relating a control signal from the microcomputer to the demodulator,
25 wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the demultiplexer indicates a loss of synchronization via the synchronization signal,

an orthogonal detector, having an oscillator, for detecting a signal component of the QPSK modulated signal and for continuously performing AFC (automatic frequency control)
30 of the oscillator; and

a PLL (phase-locked loop) for selecting the QPSK modulated signal by generating a

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local oscillation signal based on phase detection and comparison with a reference frequency signal.

In another aspect, there is provided a receiver for receiving a QPSK modulated signal,
5 the receiver comprising:

a demodulator for demodulating the QPSK modulated signal and producing a demodulated signal;

error correction means for correcting transmission errors in the demodulated signal and for generating a synchronization signal;

10 a microcomputer for controlling the demodulator based on the synchronization signal; and

a control bus for relaying a control signal from the microcomputer to the demodulator, wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the error correction means indicates a loss of synchronization via the
15 synchronization signal,

an orthogonal detector, having an oscillator, for detecting a signal component of the QPSK modulated signal and for continuously performing AFC (automatic frequency control) of the oscillator; and

a PLL (phase-locked loop) for selecting the QPSK modulated signal by generating a
20 local oscillation signal based on phase detection and comparison with a reference frequency signal.

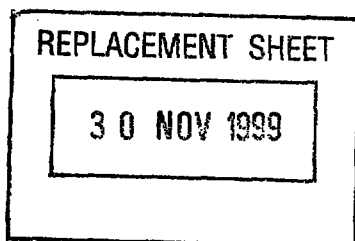
In another aspect, there is provided a receiver, comprising:

a PLL (phase-locked loop) for selecting a QPSK modulated signal by generating a
25 local oscillation signal based on phase detection and comparison with a reference frequency signal;

a demodulator for demodulating the selected QPSK modulated signal and producing a demodulated signal;

error correction means for correcting transmission errors in the demodulated signal
30 and for generating a synchronization signal;

a microcomputer for controlling the demodulator based on the synchronization signal;



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a control bus for relaying a control signal from the microcomputer to the demodulator, wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the error correction means indicates a loss of synchronization via the synchronization signal,

- 5 an orthogonal detector for detecting a signal component of the selected QPSK modulated signal and for continuously performing AFC (automatic frequency control), the orthogonal detector processing the selected QPSK modulated signal prior to demodulation by the demodulator; and

- a demultiplexer for demultiplexing the output of said error correction means; wherein
10 the demultiplexer produces a system clock signal and the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the frequency of the system clock signal.

- In another aspect, there is provided a receiver for receiving a QPSK modulated signal,
15 the receiver comprising:

PLL synthesizer means for generating a local oscillation signal;

orthogonal detection means for orthogonally detecting said QPSK modulated signal which is selected using said local oscillation signal;

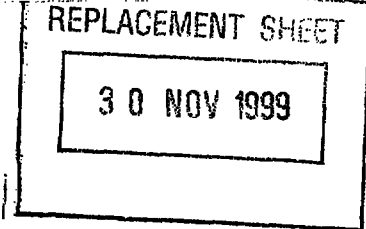
- a demodulator for demodulating the selected QPSK modulated signal and producing
20 an encoded and multiplexed signal;

a demultiplexer for demultiplexing the encoded and multiplexed signal and for generating a synchronization signal;

a microcomputer for controlling the demodulator based on the synchronization signal;

- a control bus for relaying a control signal from the microcomputer to the demodulator,
25 wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the demultiplexer indicates a loss of synchronization via the synchronization signal,

- wherein AFC (automatic frequency control) is performed at said PLL synthesizer means and said orthogonal detection means when synchronization of said demultiplexer means
30 is not established; and



continuous AFC is performed at said orthogonal detection means when synchronization of said demultiplexer means is established.

BRIEF DESCRIPTION OF THE DRAWINGS

5

FIG. 1 is a block diagram of a digital satellite broadcast receiver in accordance with a first exemplary embodiment of the present invention.

FIG. 2 is a block diagram of a digital satellite broadcast receiver in accordance with a second exemplary embodiment of the present invention.

10 FIG. 3 is a block diagram of a digital satellite broadcast receiver in accordance with a third exemplary embodiment of the present invention.

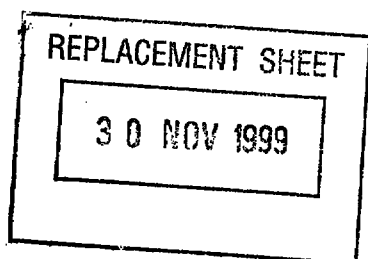
FIG. 4 is a circuit diagram of a voltage controlled oscillator composing a PLL synthesizer for channel selection.

15 FIG. 5 is a phase noise characteristic of a voltage controlled oscillator composing a PLL synthesizer for channel selection.

FIG. 6 is an AFC characteristic of an orthogonal detection voltage controlled oscillator.

FIG. 7 is a block diagram of a digital satellite broadcast receiver in accordance with a fourth exemplary embodiment of the present invention.

20 FIG. 8 is a block diagram of a digital satellite



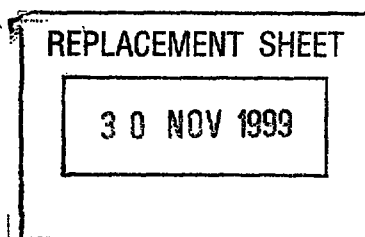
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What is claimed is:



1. A receiver for receiving a first modulated digital signal, the receiver comprising:
 - a first local oscillator for generating a first local oscillation signal;
 - 5 a mixer for converting the first modulated digital signal into a second modulated digital signal having a predetermined intermediate frequency based on the first local oscillation signal;
 - a filter for extracting an intermediate frequency signal from the second modulated digital signal;
 - 10 a second local oscillator, responsive to an AFC (Automatic Frequency Control) signal, for generating a second local oscillation signal having an oscillation frequency;
 - an orthogonal detector for detecting a signal component based on the second local oscillation signal;
 - an A/D (analogue-to-digital) converter for converting the signal component into a
 - 15 digital signal; and
 - a digital demodulator, having an AFC (Automatic Frequency Control) detector, for digitally demodulating the digital signal, and for producing the AFC signal.
2. A receiver as recited in claim 1, further comprising:
 - 20 a computer for controlling the first local oscillation signal; and
 - a control bus for relaying a control signal from the computer to the first local oscillator.
3. A digital receiver comprising:
 - 25 an orthogonal detector, having an oscillator, for orthogonally detecting a selected QPSK (quaternary phase-shift keying) modulated signal; and
 - a PLL (phase-locked loop) for selecting a modulated signal by generating a local oscillation signal based on phase detection and comparison with a reference frequency signal, wherein AFC (automatic frequency control) of the oscillator is continuously performed
 - 30 at said orthogonal detector.

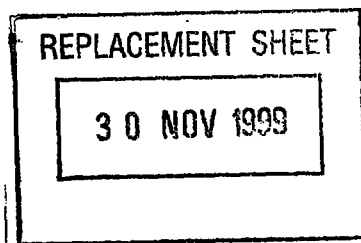


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4. A digital receiver comprising:
- a PLL for generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;
 - a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into
- 5 a first intermediate frequency signal based on the local oscillation signal;
- a bandpass filter for extracting a second intermediate frequency signal from the first intermediate frequency signal;
 - an orthogonal detector, responsive to an AFC (Automatic Frequency Control) signal, for detecting an in-phase component signal I and a quadrature component signal Q of the
- 10 second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;
- an A/D converter for converting the in-phase component signal I and the quadrature component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal; and
- 15 a QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal, and for producing the AFC (Automatic Frequency Control).
5. A digital receiver comprising:
- 20 a PLL for generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;
- a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into a first intermediate frequency signal based on the local oscillation signal;
 - a bandpass filter for extracting a second intermediate frequency signal from the first
- 25 intermediate frequency signal;
- orthogonal detector for detecting an in-phase component I and a quadrature component Q of the second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;
 - an A/D converter for converting the in-phase component signal I and the quadrature
- 30 component signal Q of the second intermediate frequency signal to a digital in-phase



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component signal and a digital quadrature component signal;

QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal and for producing an encoded and multiplexed signal;

- 5 error correction means for correcting transmission errors of the encoded and multiplexed signal; and

a demultiplexer for demultiplexing the output of said error correction means and for producing a system clock signal, wherein the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the system clock signal produced by
10 said demultiplexer.

6. A digital receiver comprising:

a PLL for generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;

- 15 a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into a first intermediate frequency signal based on the local oscillation signal;

a bandpass filter for extracting a second intermediate frequency signal from the first intermediate frequency signal;

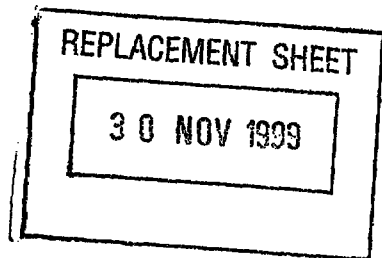
- orthogonal detector for detecting an in-phase component I and a quadrature component
20 Q of the second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;

an A/D converter for converting the in-phase component signal I and the quadrature component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal;

- 25 QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal and for producing an encoded and multiplexed signal;

error correction means for correcting transmission errors of the encoded and multiplexed signal;

- 30 a demultiplexer for demultiplexing the output of said error correction means and for



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generating a synchronization signal;

a microcomputer for controlling the PLL based on the synchronization signal; and

a control bus for relaying a control signal from the microcomputer to the PLL,

wherein the microcomputer resets the PLL by relaying the control signal via the

5 control bus when the demultiplexer indicates a loss of synchronization via the synchronization signal.

7. A digital receiver comprising:

a PLL for generating a local oscillation signal based on phase detection and

10 comparison with a reference frequency signal;

a mixer for converting a QPSK (quaternary phase-shift keying) modulated signal into a first intermediate frequency signal based on the local oscillation signal;

a bandpass filter for extracting a second intermediate frequency signal from the first intermediate frequency signal;

15 orthogonal detector for detecting an in-phase component I and a quadrature component Q of the second intermediate frequency signal and for continuously compensating a frequency drift of the second intermediate frequency signal;

an A/D converter for converting the in-phase component signal I and the quadrature component signal Q of the second intermediate frequency signal to a digital in-phase component signal and a digital quadrature component signal;

20 QPSK demodulator for digitally demodulating the digital in-phase component signal and the digital quadrature component signal and for producing an encoded and multiplexed signal;

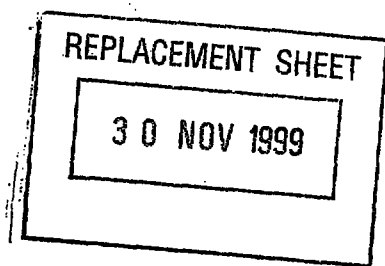
error correction means for correcting transmission errors of the encoded and multiplexed signal, for outputting a corrected multiplexed signal, and for generating a

25 synchronization signal;

a demultiplexer for demultiplexing the corrected multiplexed signal of said error correction means;

a microcomputer for controlling the PLL based on the synchronization signal; and

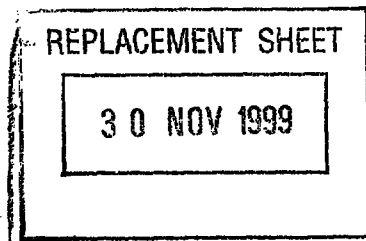
30 a control bus for relaying a control signal from the microcomputer to the PLL,



wherein the microcomputer resets the PLL by relaying the control signal via the control bus when the error correction means indicates a loss of synchronization via the synchronization signal.

- 5 8. A receiver for receiving a QPSK modulated signal, the receiver comprising:
a demodulator for demodulating the QPSK modulated signal and producing an encoded and multiplexed signal;
a demultiplexer for demultiplexing the encoded and multiplexed signal and for generating a synchronization signal;
- 10 a microcomputer for controlling the demodulator based on the synchronization signal;
a control bus for relating a control signal from the microcomputer to the demodulator, wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the demultiplexer indicates a loss of synchronization via the synchronization signal,
- 15 an orthogonal detector, having an oscillator, for detecting a signal component of the QPSK modulated signal and for continuously performing AFC (automatic frequency control) of the oscillator; and
a PLL (phase-locked loop) for selecting the QPSK modulated signal by generating a local oscillation signal based on phase detection and comparison with a reference frequency
- 20 signal.
9. A receiver for receiving a QPSK modulated signal, the receiver comprising:
a demodulator for demodulating the QPSK modulated signal and producing a demodulated signal;
- 25 error correction means for correcting transmission errors in the demodulated signal and for generating a synchronization signal;
a microcomputer for controlling the demodulator based on the synchronization signal; and
a control bus for relaying a control signal from the microcomputer to the demodulator,
- 30 wherein the microcomputer resets the demodulator by relaying the control signal via the





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control bus when the error correction means indicates a loss of synchronization via the synchronization signal,

an orthogonal detector, having an oscillator, for detecting a signal component of the QPSK modulated signal and for continuously performing AFC (automatic frequency control) of the oscillator; and

a PLL (phase-locked loop) for selecting the QPSK modulated signal by generating a local oscillation signal based on phase detection and comparison with a reference frequency signal.

10 10. A digital receiver as recited in claim 6, wherein
the QPSK demodulator recovers a clock signal and the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the frequency of the clock signal.

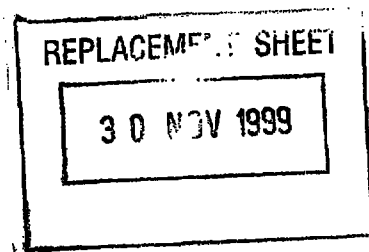
15 11. A digital receiver as recited in claim 7, wherein
the QPSK demodulator recovers a clock signal and the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the frequency of the clock signal.

20 12. A digital receiver as recited in claim 6, wherein
the multiplexer produces a system clock signal and the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the frequency of the system clock signal.



25 13. A receiver, comprising:
a PLL (phase-locked loop) for selecting a QPSK modulated signal by generating a local oscillation signal based on phase detection and comparison with a reference frequency signal;

a demodulator for demodulating the selected QPSK modulated signal and producing
30 a demodulated signal;



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error correction means for correcting transmission errors in the demodulated signal and for generating a synchronization signal;

a microcomputer for controlling the demodulator based on the synchronization signal;

a control bus for relaying a control signal from the microcomputer to the demodulator,

5 wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the error correction means indicates a loss of synchronization via the synchronization signal,

an orthogonal detector for detecting a signal component of the selected QPSK modulated signal and for continuously performing AFC (automatic frequency control), the
10 orthogonal detector processing the selected QPSK modulated signal prior to demodulation by the demodulator; and

a demultiplexer for demultiplexing the output of said error correction means; wherein the demultiplexer produces a system clock signal and the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the frequency of the system
15 clock signal.



14. A digital receiver as recited in claim 7, wherein
the demultiplexer produces a system clock signal and the reference frequency signal for phase detection and comparison by said PLL is calculated by dividing the frequency of
20 the system clock signal.

15. A receiver for receiving a QPSK modulated signal, the receiver comprising:
PLL synthesizer means for generating a local oscillation signal;
orthogonal detection means for orthogonally detecting said QPSK modulated signal
25 which is selected using said local oscillation signal;

a demodulator for demodulating the selected QPSK modulated signal and producing an encoded and multiplexed signal;

a demultiplexer for demultiplexing the encoded and multiplexed signal and for generating a synchronization signal;

30 a microcomputer for controlling the demodulator based on the synchronization signal;

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a control bus for relaying a control signal from the microcomputer to the demodulator, wherein the microcomputer resets the demodulator by relaying the control signal via the control bus when the demultiplexer indicates a loss of synchronization via the synchronization signal,

- 5 wherein AFC (automatic frequency control) is performed at said PLL synthesizer means and said orthogonal detection means when synchronization of said demultiplexer means is not established; and

continuous AFC is performed at said orthogonal detection means when synchronization of said demultiplexer means is established.

