Abstract

SOLDER BUMP WITH INNER CORE PILLAR IN SEMICONDUCTOR PACKAGE

A flip chip semiconductor package has a substrate with a plurality of active devices. A contact pad is formed on the substrate in electrical contact with the plurality of active devices. A passivation layer, second barrier layer, and adhesion layer are formed between the substrate and an intermediate conductive layer. The intermediate conductive layer is in electrical contact with the contact pad. A copper inner core pillar is formed by plating over the intermediate conductive layer. The inner core pillar has a rectangular, cylindrical, toroidal, or hollow cylinder form factor. A solder bump is formed around the inner core pillar by plating solder material and reflowing the solder material to form the solder bump. A first barrier layer and wetting layer are formed between the inner core pillar and solder bump. The solder bump is in electrical contact with the intermediate conductive layer. (Fig. 3b)