(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 October 2010 (28.10.2010)

PCT

(10) International Publication Number
WO 2010/122023 A2

(51) International Patent Classification:
H01L 21/306 (2006.01) *H01L 21/18* (2006.01)
H01L 21/762 (2006.01)

(21) International Application Number:
PCT/EP2010/055198

(22) International Filing Date:
20 April 2010 (20.04.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0952581 21 April 2009 (21.04.2009) FR

(71) Applicant *(for all designated States except US)*: **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique des Fontaines, Chemin des Franques, F-38190 Bernin (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **REYNAUD, Patrick** [FR/FR]; 20, rue Flora Tristan, F-38400 Saint Martin d'Hères (FR). **ECARNOT, Ludovic** [FR/FR]; 14 rue Jean-Pierre Guingat, F-38450 Vif (FR). **RADOUANE, Khalid** [FR/FR]; 115 Allée Fantin Latour, F-38330 Montbonnot Saint Martin (FR).

(74) Agents: **WARCOIN, AHNER, TEXIER, LE FORESTIER, CALLON DE LAMARCK, COLLIN, TETAZ, FAIVRE PETIT** et al.; Cabinet Régimbeau, 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

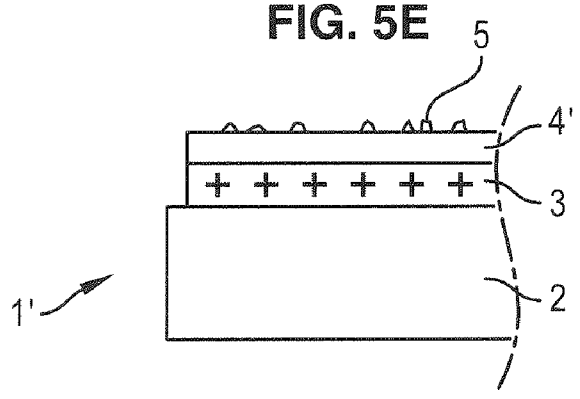
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

— *of inventorship (Rule 4.17(iv))*

[Continued on next page]

(54) **Title**: METHOD TO THIN A SILICON-ON-INSULATOR SUBSTRATE

FIG. 5E



(57) **Abstract**: The invention concerns a method to thin an initial silicon-on-insulator SOI substrate, comprising a layer (3) of silicon oxide SiO_2 buried between a silicon carrier substrate (2) and a silicon surface layer. This method is noteworthy in that it comprises the following successive steps consisting of conducting: -thermal oxidation treatment of said initial substrate, to oxidize part of said silicon surface layer, -a first, then a second cycle of etching and cleaning, the first cycle etching being performed so as fully to remove the formed thermal oxide and to lift off all the unstable parts of the edge of said initial substrate, the second cycle etch being conducted to remove from the surface of said thinned substrate the formed polluting particles (5) deposited thereupon, so as to obtain a final SOI substrate(1') whose thinned surface layer (4') forms an active layer.

WO 2010/122023 A2

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*