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ABSTRACT

BUS ARCHITECTURE FOR INTEGRATED DATA
AND VIDEO MEMORY

A bus architecture and protocol for integrated data and video memory. A high speed dedicated memory bus is coupled to a memory controller. The
5 memory controller is in turn coupled to a multiple processor bus
interconnecting one or more processors. Single in-line memory modules
(SIMMs) incorporating dynamic random access memory (DRAM), video RAM
(VRAM), and static nonvolatile RAM (SRAM) are coupled to the memory bus.
Bus control signals forming a bus protocol, and address and data lines from the
10 memory controller are shared by all memory modules operating on the
memory bus. Certain control signals invoke specific operations on memory
modules or are ignored, depending on the type of memory module receiving
the control signal. The memory modules incorporate the consistent protocol
by virtue of a consistent control signal pin out. The SIMMs further incorporate
15 buffering and conversion functions, thereby relieving the memory controller
of service overhead associated with these functions. Integrating all forms of
memory into a single data and video memory architecture permits a highly
functional dedicated memory bus to be connected to the computer system.

