## ABSTRACT

# MEMORY DEVICE, OPERATING METHOD THEREOF AND PAGE BUFFER

A memory device having an improved operation speed includes: a memory cell; a page buffer connected to the memory cell through a bit line; and a program operation controller for controlling an operation of the page buffer. The page buffer includes: a bit line voltage supply for providing a precharge voltage to the bit line; a sensing node voltage supply for providing a sensing node precharge voltage to a sensing node connected to the bit line; a first latch for storing first verify data; a sensing node connector for releasing connection between the bit line and the sensing node, after the first verify data is stored; and a second latch for storing second verify data determined according to the voltage of the sensing node, after the connection between the bit line and the sensing node is released.

FIG. 1