

## CLAIMS

1. A method of forming a semiconductor packaging structure, the method comprising:  
forming a first semiconductor package, a second semiconductor package, a third semiconductor package, and a fourth semiconductor package, each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package comprising a semiconductor die, a mold encapsulation structure covering at least a portion of the semiconductor die, and a redistribution layer over the semiconductor die;  
arranging the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package to form a vertical stacked arrangement with a mold portion comprising a plurality of mold encapsulation structures, the mold portion extending from a first side of the vertical stacked arrangement to a second side of the vertical stacked arrangement opposite the first side; wherein a first adhesive layer in contact with a bottom side of the second semiconductor package is also in contact with the redistribution layer of the first semiconductor package so that the first adhesive layer adheres the first semiconductor package to the second semiconductor package; wherein a second adhesive layer in contact with a bottom side of the third semiconductor package is also in contact with the redistribution layer of the second semiconductor package so that the second adhesive layer adheres the second semiconductor package to the third semiconductor package; and wherein a third adhesive layer in contact with a bottom side of the fourth semiconductor package is also in contact with the redistribution layer of the third semiconductor package so that the third adhesive layer adheres the third semiconductor package to the fourth semiconductor package;

forming a first via on the mold portion at the first side of the vertical stacked arrangement after the vertical stacked arrangement is formed;

forming a second via on the mold portion at the second side of the vertical stacked arrangement after forming the first via, the second via meeting the first via to form a continuous through mold via; and

forming an electrically conductive filled via extending through the mold portion from the first side of the vertical stacked arrangement to the second side of the vertical stacked arrangement by depositing a suitable electrically conductive material in the first via and in the second via;

wherein a diameter of the electrically conductive filled via at the first side of the vertical stacked arrangement is greater than a diameter of the electrically conductive filled via along an intervening plane of the vertical stacked arrangement, the intervening plane between the first side of the vertical stacked arrangement and the second side of the vertical stacked arrangement; and

wherein a diameter of the electrically conductive filled via at the second side of the vertical stacked arrangement is greater than the diameter of the electrically conductive filled via along the intervening plane of the vertical stacked arrangement.

2. The method according to claim 1,  
wherein the redistribution layer of each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package extends from over the semiconductor die to over the mold encapsulation structure.
3. The method according to claim 1,  
wherein the redistribution layer of each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package comprises one or more electrically conductive lines.

4. The method according to claim 1,  
wherein the one or more electrically conductive lines of each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package are in electrical connection with the electrically conductive filled via.
5. The method according to claim 1,  
wherein forming the first via comprises laser drilling the mold portion at the first side of the vertical stacked arrangement.
6. The method according to claim 1,  
wherein forming the second via comprises laser drilling the mold portion at the second side of the vertical stacked arrangement.
7. The method according to claim 1,  
wherein the electrically conductive filled via comprises a first tapered portion extending from the first side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement; and  
wherein the electrically conductive filled via comprises a second tapered portion extending from the second side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement.
8. The method according to claim 1,  
wherein the suitable electrically conductive material is deposited in the first via and the second via by electroplating.
9. A semiconductor packaging structure comprising:  
a vertical stacked arrangement comprising a first semiconductor package, a second semiconductor package, a third semiconductor package, and a fourth semiconductor package, each of the first semiconductor package, the second

semiconductor package, the third semiconductor package, and the fourth semiconductor package comprising a semiconductor die, a mold encapsulation structure covering at least a portion of the semiconductor die, and a redistribution layer over the semiconductor die;

a first adhesive layer in contact with a bottom side of the second semiconductor package and also in contact with the redistribution layer of the first semiconductor package so that the first adhesive layer adheres the first semiconductor package to the second semiconductor package;

a second adhesive layer in contact with a bottom side of the third semiconductor package and also in contact with the redistribution layer of the second semiconductor package so that the second adhesive layer adheres the second semiconductor package to the third semiconductor package; and

a third adhesive layer in contact with a bottom side of the fourth semiconductor package and also in contact with the redistribution layer of the third semiconductor package so that the third adhesive layer adheres the third semiconductor package to the fourth semiconductor package;

wherein the vertical stacked arrangement comprises a mold portion comprising a plurality of mold encapsulation structures, the mold portion extending from a first side of the vertical stacked arrangement to a second side of the vertical stacked arrangement opposite the first side;

wherein the mold portion comprises an electrically conductive filled via extending through the mold portion from the first side of the vertical stacked arrangement to the second side of the vertical stacked arrangement, the electrically conductive filled via comprising a suitable electrically conductive material in a first via and a second via, the second via meeting the first via to form a continuous through mold via;

wherein a diameter of the electrically conductive filled via at the first side of the vertical stacked arrangement is greater than a diameter of the electrically conductive filled via along an intervening plane of the vertical stacked arrangement, the intervening plane between the first side of the vertical

stacked arrangement and the second side of the vertical stacked arrangement;  
and

wherein a diameter of the electrically conductive filled via at the second side of the vertical stacked arrangement is greater than the diameter of the electrically conductive filled via along the intervening plane of the vertical stacked arrangement.

10. The semiconductor packaging structure according to claim 9,  
wherein the redistribution layer of each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package extends from over the semiconductor die to over the mold encapsulation structure.
11. The semiconductor packaging structure according to claim 9,  
wherein the redistribution layer of each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package comprises one or more electrically conductive lines.
12. The semiconductor packaging structure according to claim 9,  
wherein the one or more electrically conductive lines of each of the first semiconductor package, the second semiconductor package, the third semiconductor package, and the fourth semiconductor package are in electrical connection with the electrically conductive filled via.
13. The semiconductor packaging structure according to claim 9,  
wherein the intervening plane of the vertical stacked arrangement, the first side of the vertical stacked arrangement, and the second side of the vertical stacked arrangement are substantially parallel to one another.
14. The semiconductor packaging structure according to claim 9,

wherein the electrically conductive filled via comprises a first tapered portion extending from the first side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement; and  
wherein the electrically conductive filled via comprises a second tapered portion extending from the second side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement.

15. The semiconductor packaging structure according to claim 9,  
wherein the suitable electrically conductive material is copper.