



(51) International Patent Classification:
G06F 12/10 (2006.01)

(21) International Application Number:

PCT/IB2012/056736

(22) International Filing Date:

26 November 2012 (26.11.2012)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

13/524,468

15 June 2012 (15.06.2012)

US

(71) **Applicant:** INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(71) **Applicant (for MG only): IBM UNITED KINGDOM LIMITED** [GB/GB]; PO Box 41, North Harbour, Portsmouth, Hampshire, PO6 3AU (GB).

(72) **Inventors:** **GREINER, Dan**; IBM Corporation, SVL/090/F374, 555 Bailey Avenue, San Jose, California 95141 (US). **ROGERS, Robert**; IBM Corporation, P328, 2455 South Road, Poughkeepsie, New York 12601 (US).

(74) **Agent: WILLIAMS, Julian**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester, Hampshire, SO21 2JN (GB).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: COMPARE AND REPLACE DAT TABLE ENTRY

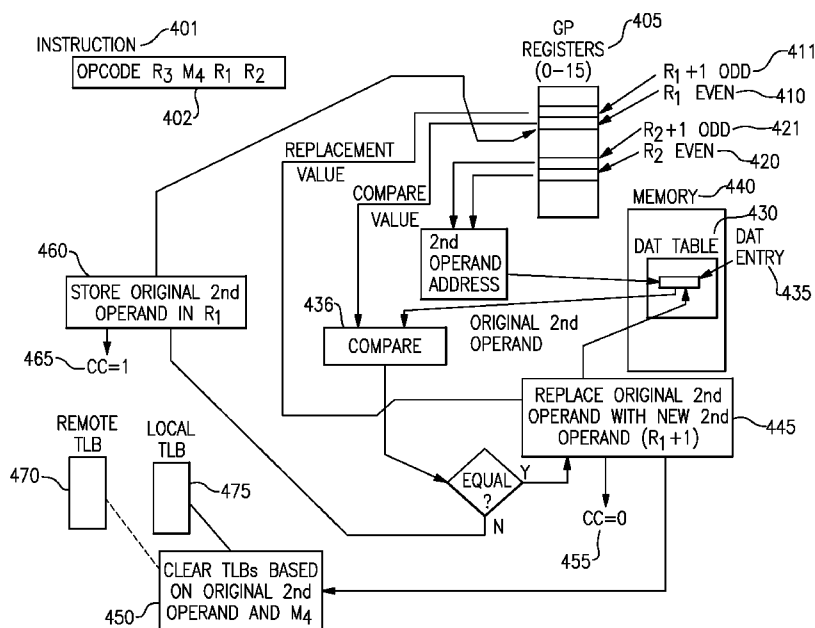


FIG.4

(57) Abstract: A first and a second operand are compared. If they are equal, the contents of register $R_1 + 1$ are stored at the second-operand location, and the specified CPU or CPUs in the configuration are cleared of all TLB table entries of the designated type formed through the use of the replaced entry in storage, and all lower-level TLB table entries formed through the use of the cleared higher-level TLB table entries. A valid DAT table entry is replaced with a new entry, and the Translation Lookaside Buffer (TLB) is purged of any copies of (at least) the single entry on all CPUs in the configuration. If the first and second operands are unequal, the second operand is loaded at the first-operand location. The comparison result is indicated by the condition code. A method, system and a computer program product are provided.



Published:

- *without international search report and to be republished
upon receipt of that report (Rule 48.2(g))*