FIG. 1A

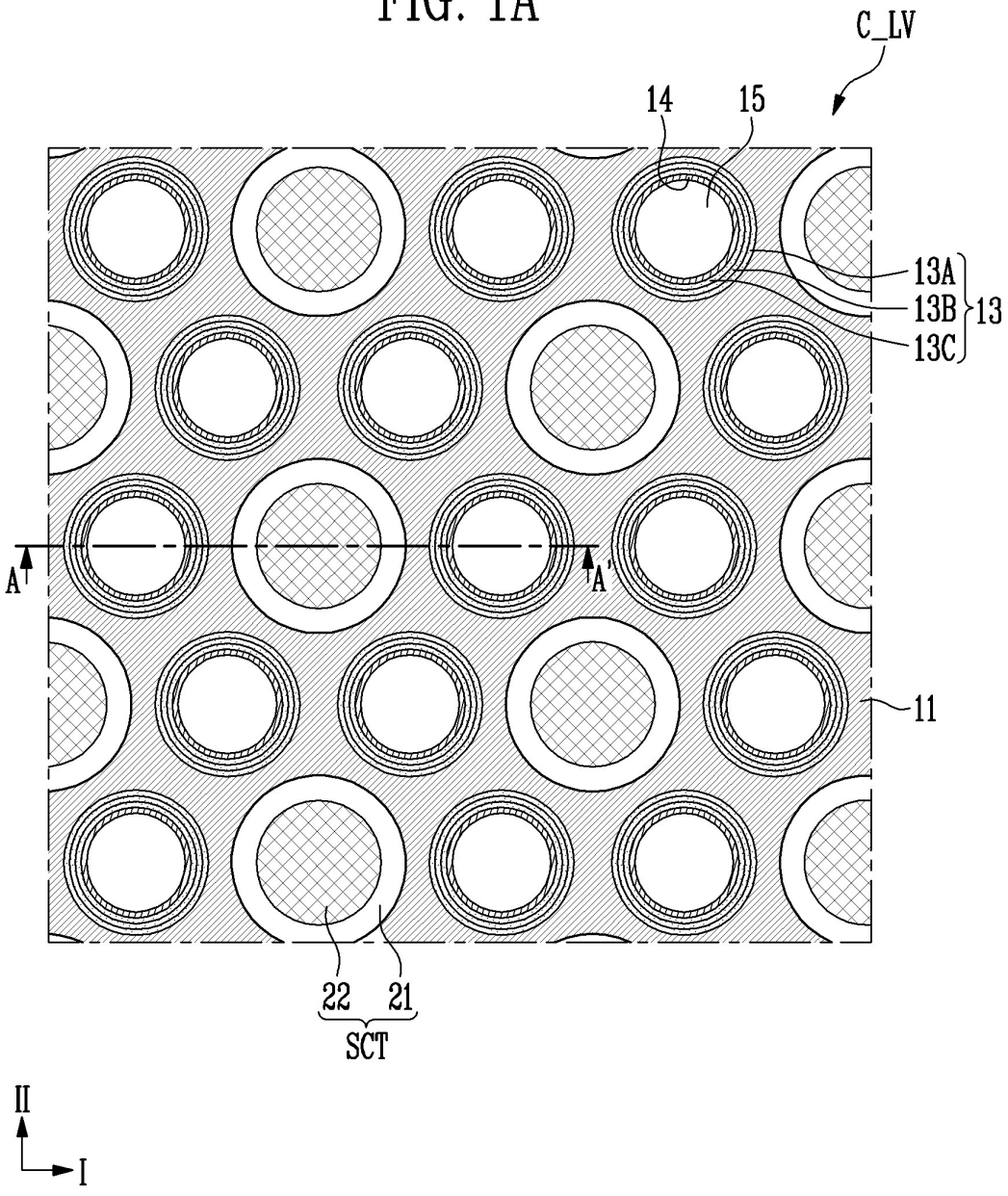


FIG. 1B

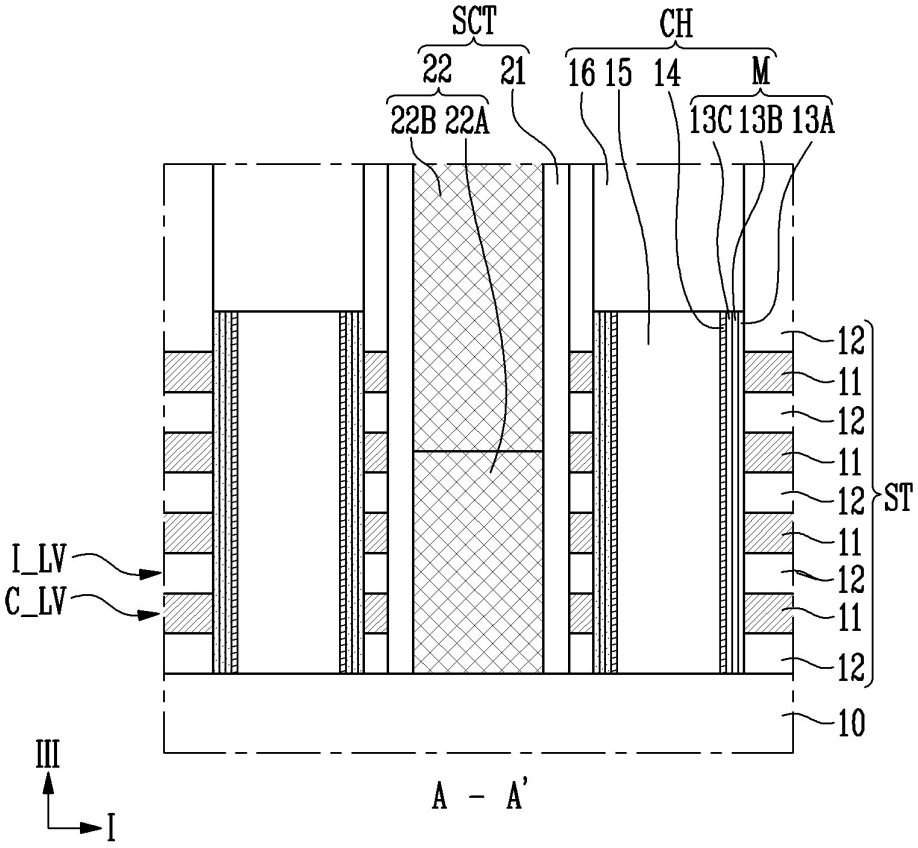

SCT
CH
22
21
16
15
14
M
22B
22A
13C
13B
13A
12
11
12
11
12
11
12
11
12
ST
I_LV
C_LV
10
III
I
A - A'

FIG. 2A

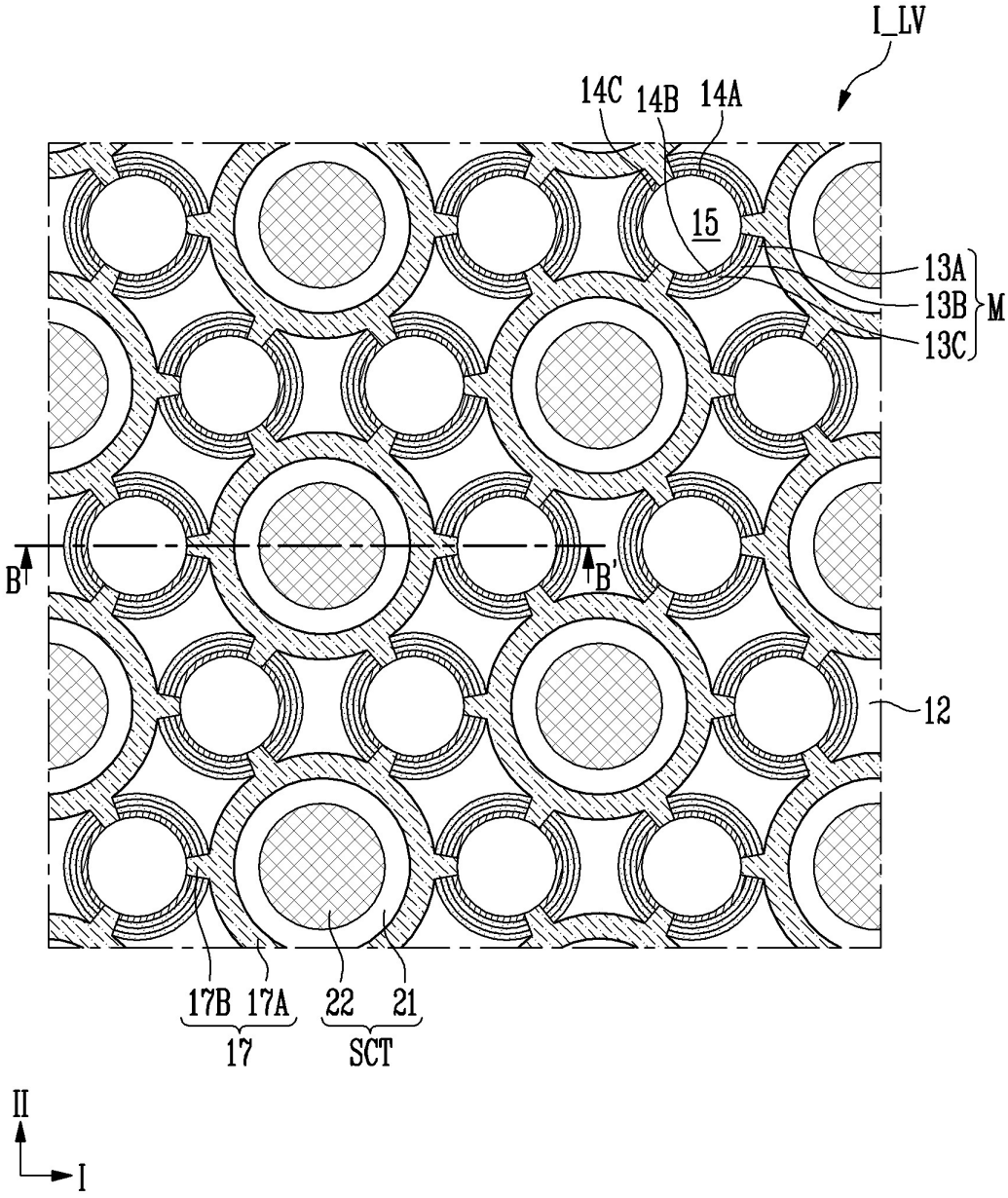


FIG. 2B

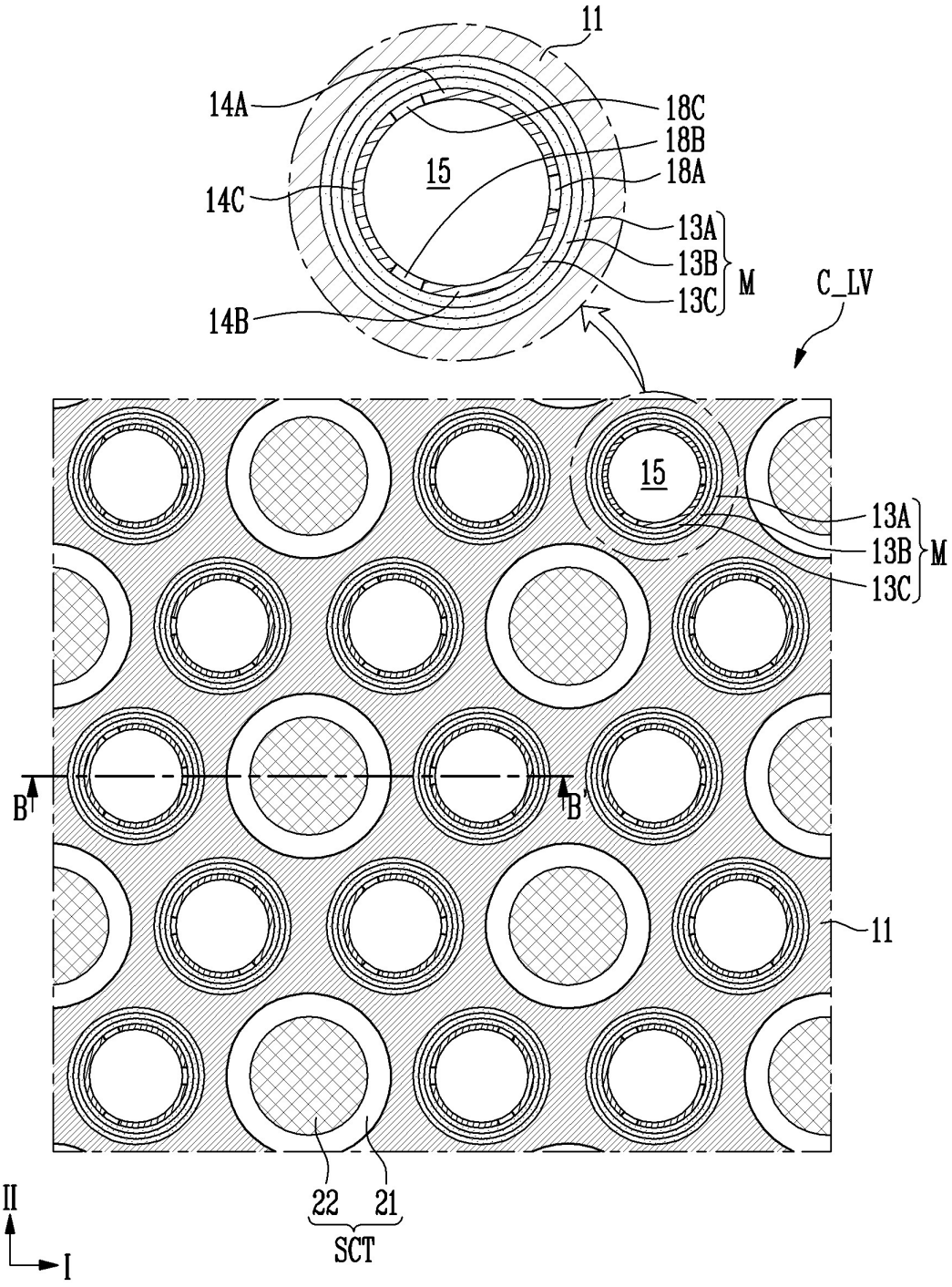

11
14A
18C
18B
18A
15
14C
13A
13B
13C
M
C_LV
14B
15
13A
13B
13C
M
B
B'
11
22
21
SCT
II
I

FIG. 2C

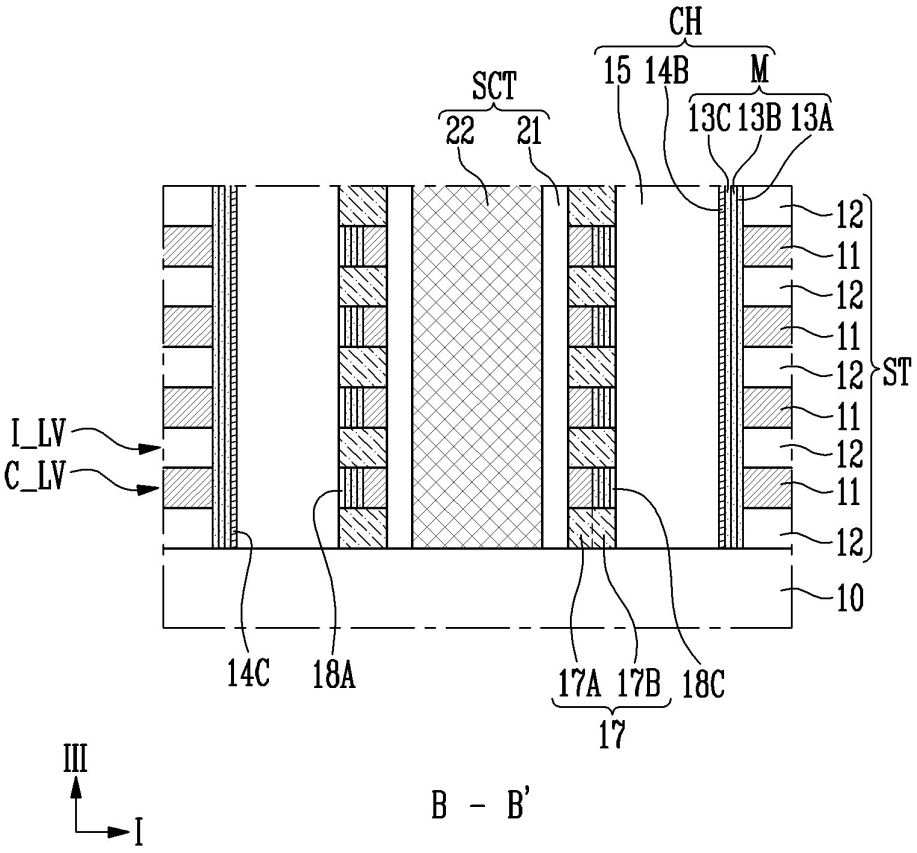

CH
15
14B
M
SCT
22
21
13C
13B
13A
12
11
12
11
12
11
12
11
12
ST
I_LV
C_LV
10
14C
18A
17A
17B
18C
17
III
I
B - B'

FIG. 2D

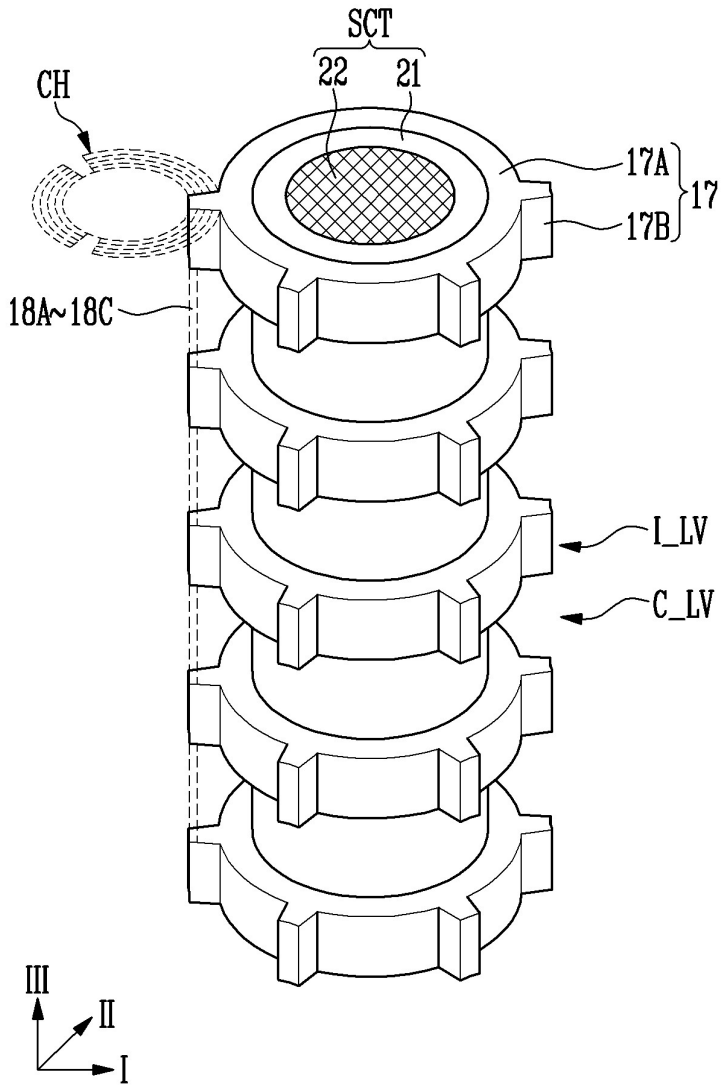


FIG. 2E

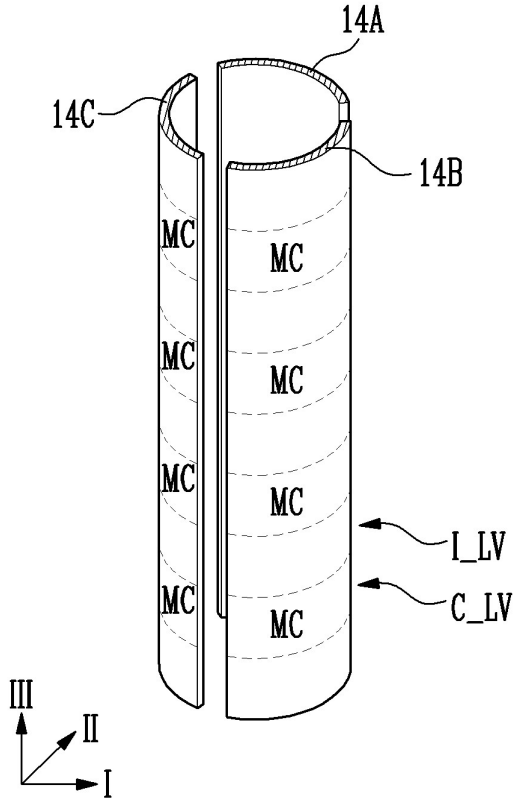

14A
14C
14B
MC
MC
MC
MC
MC
MC
MC
MC
MC
I_LV
C_LV
III
II
I

FIG. 2F

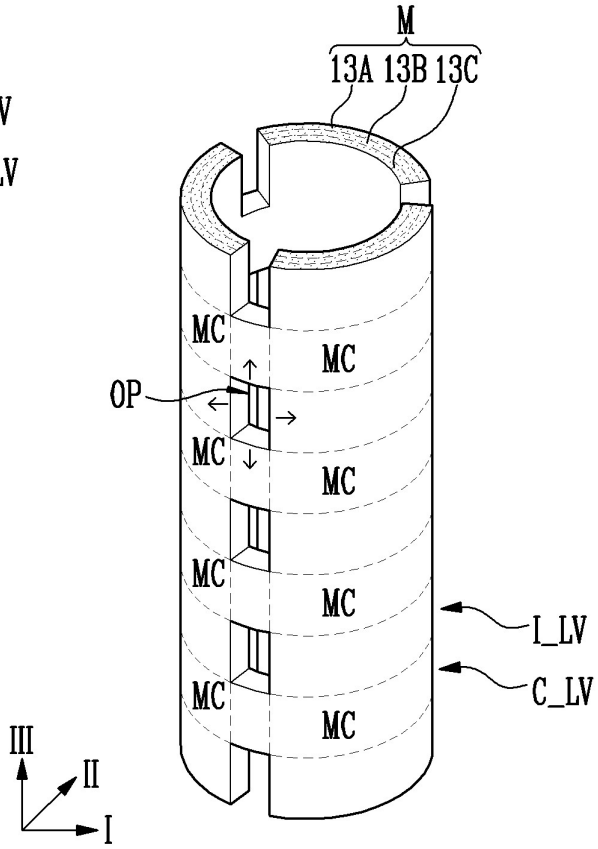

M
13A 13B 13C
OP
MC
MC
MC
MC
MC
MC
MC
MC
MC
I_LV
C_LV
III
II
I

FIG. 3A

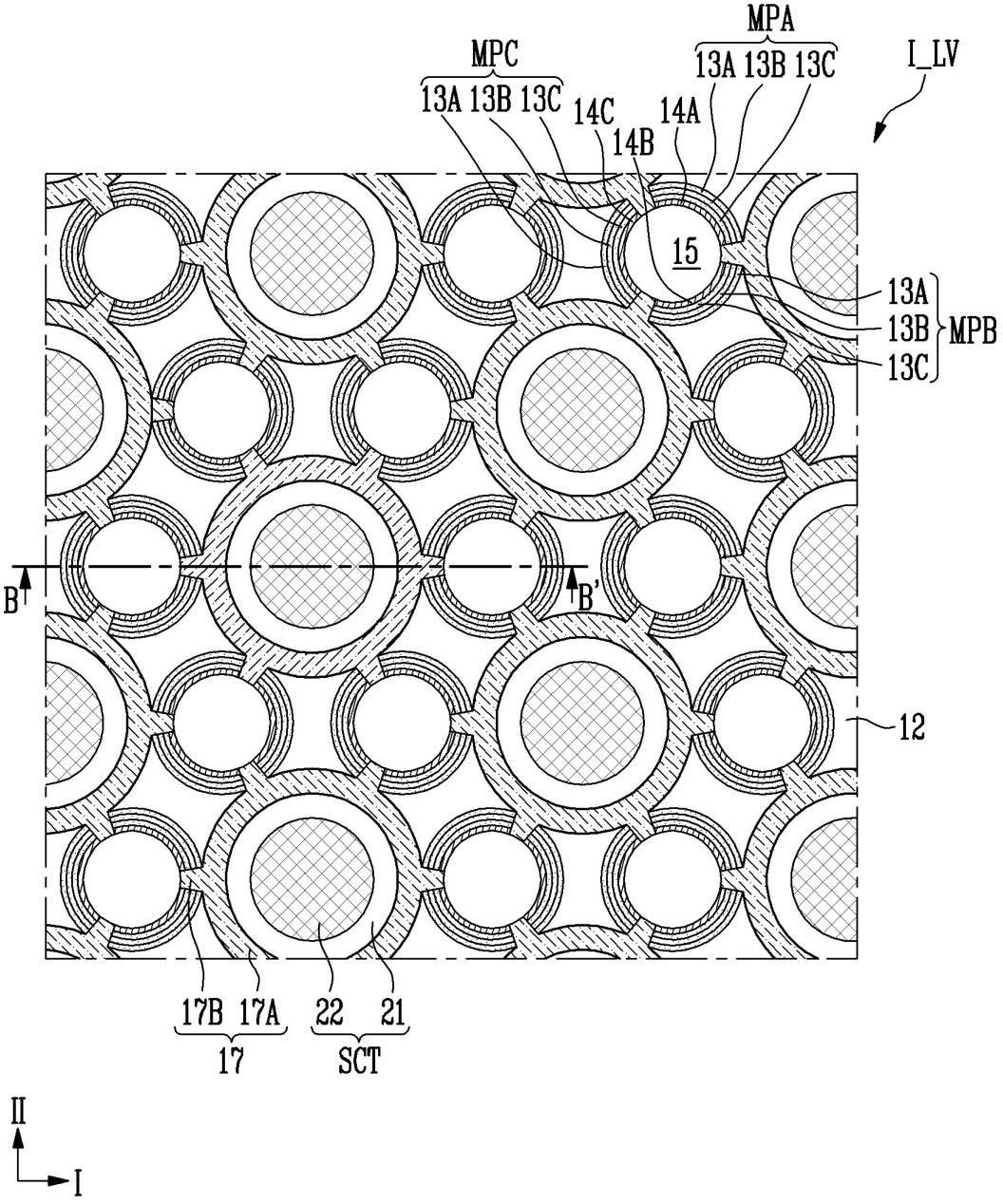

MPA
MPC
13A 13B 13C
13A 13B 13C
I_LV
14C
14A
14B
15
13A
13B
MPB
13C
B
B'
12
17B 17A
22 21
17
SCT
II
I

FIG. 3B

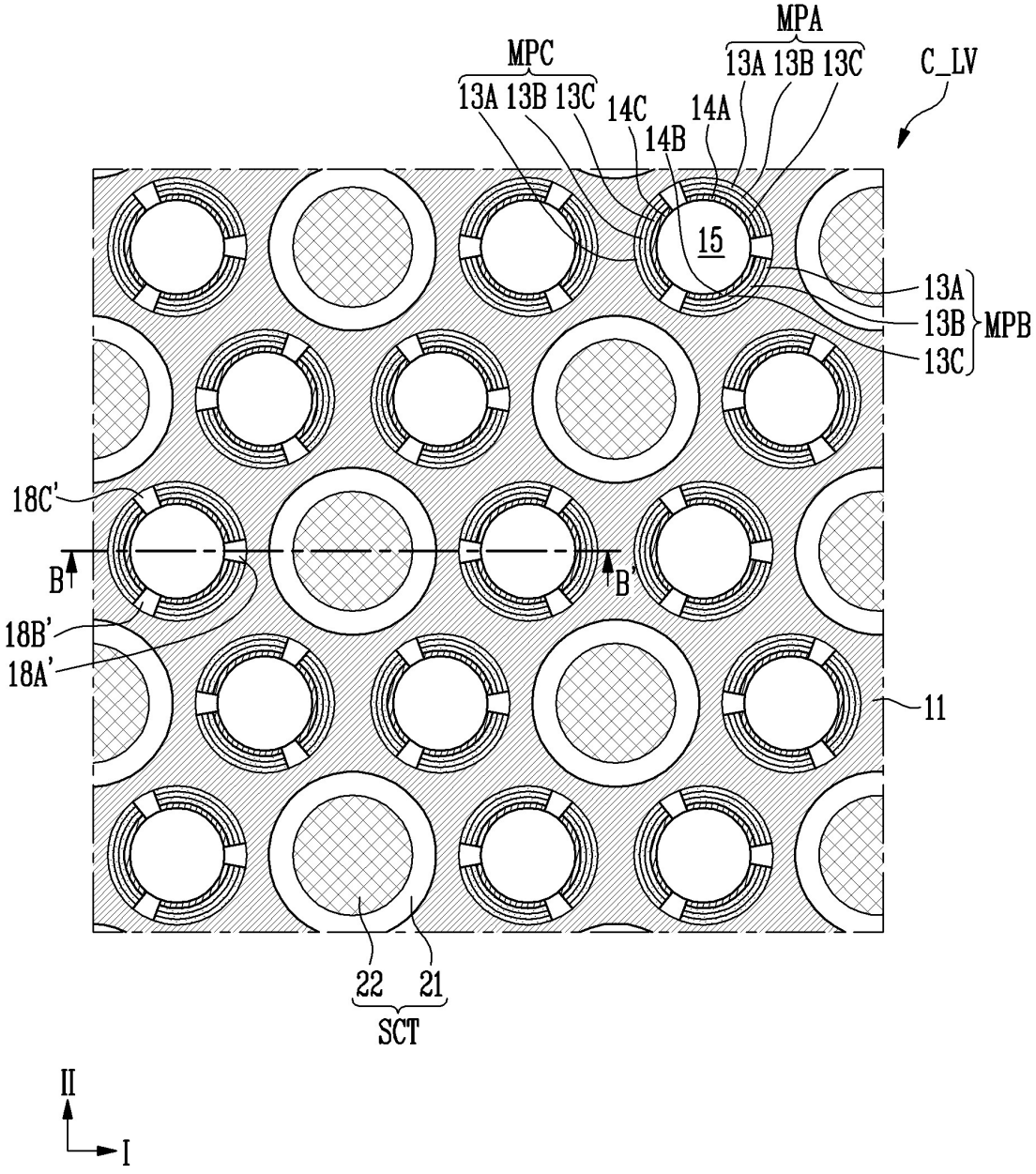

MPA
MPC
13A 13B 13C
13A 13B 13C
C_LV
14C
14A
14B
15
13A
13B
13C
MPB
18C'
B
B'
18B'
18A'
11
22
21
SCT
II
I

FIG. 3C

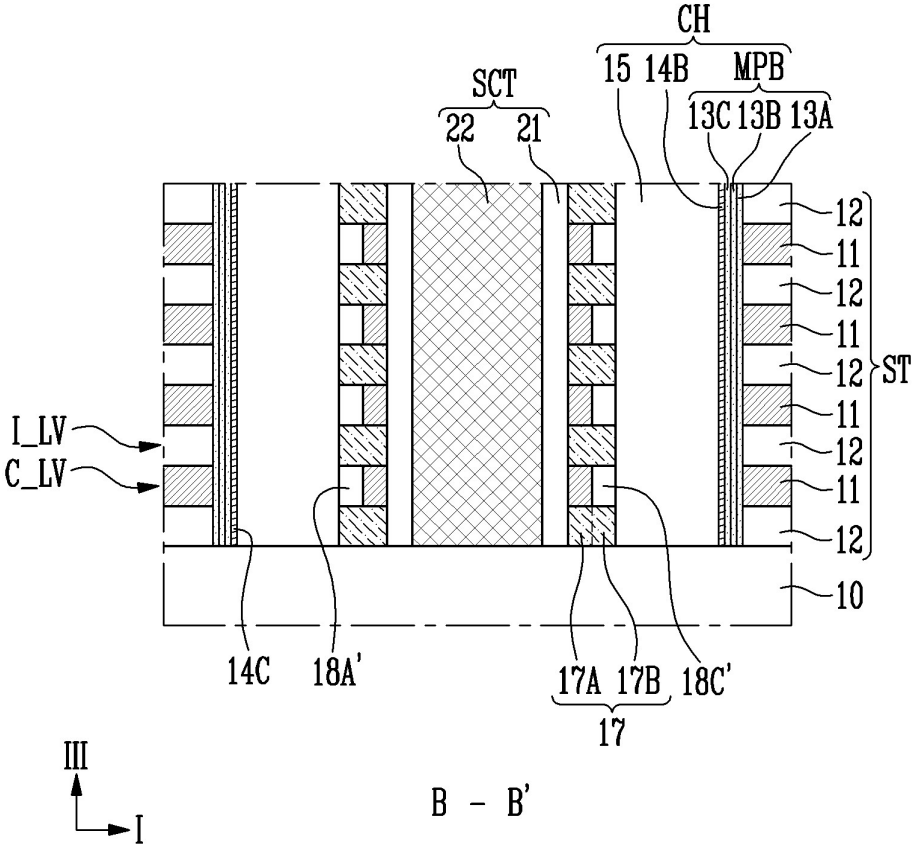

CH
15 14B MPB
SCT
22 21
13C 13B 13A
12
11
12
11
12
11
12
11
12
ST
I_LV
C_LV
10
14C
18A'
17A 17B 18C'
17
III
I
B - B'

FIG. 3D

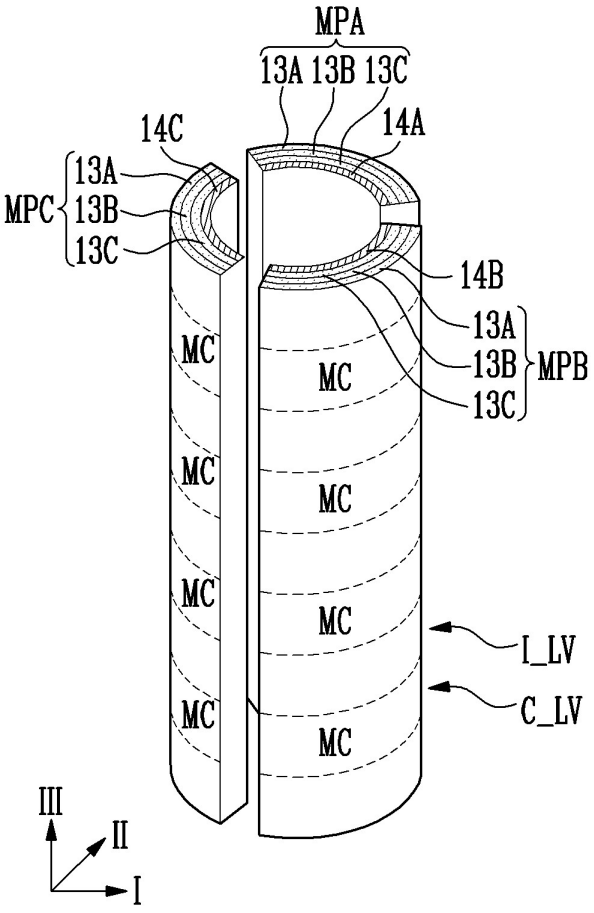

MPA
13A 13B 13C
14C
14A
MPC
13A
13B
13C
14B
13A
13B
13C
MPB
MC
MC
MC
MC
MC
MC
MC
MC
I_LV
C_LV
III
II
I

FIG. 3E

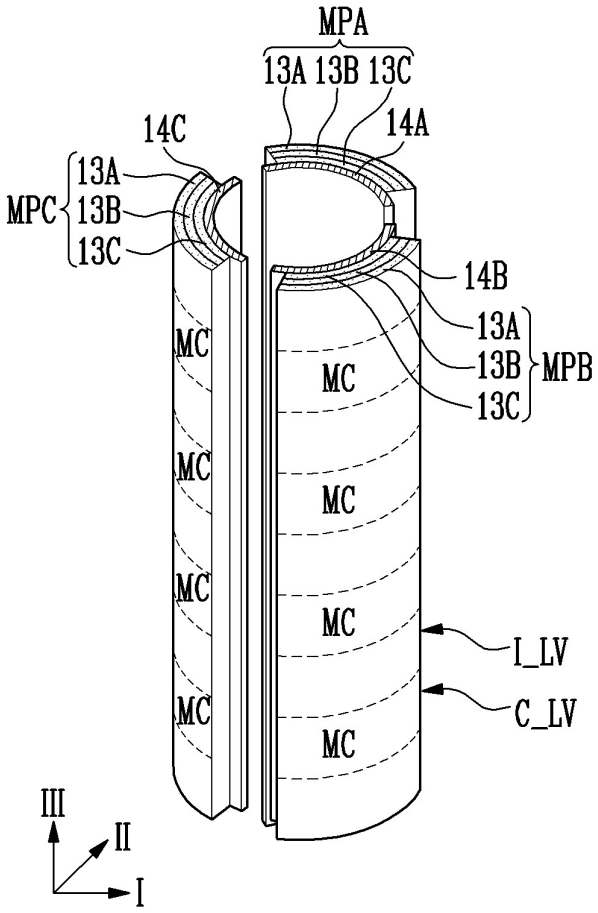

MPA
13A 13B 13C
14C
14A
MPC
13A
13B
13C
14B
13A
13B
13C
MPB
MC
MC
MC
MC
MC
MC
MC
MC
I_LV
C_LV
III
II
I

FIG. 4

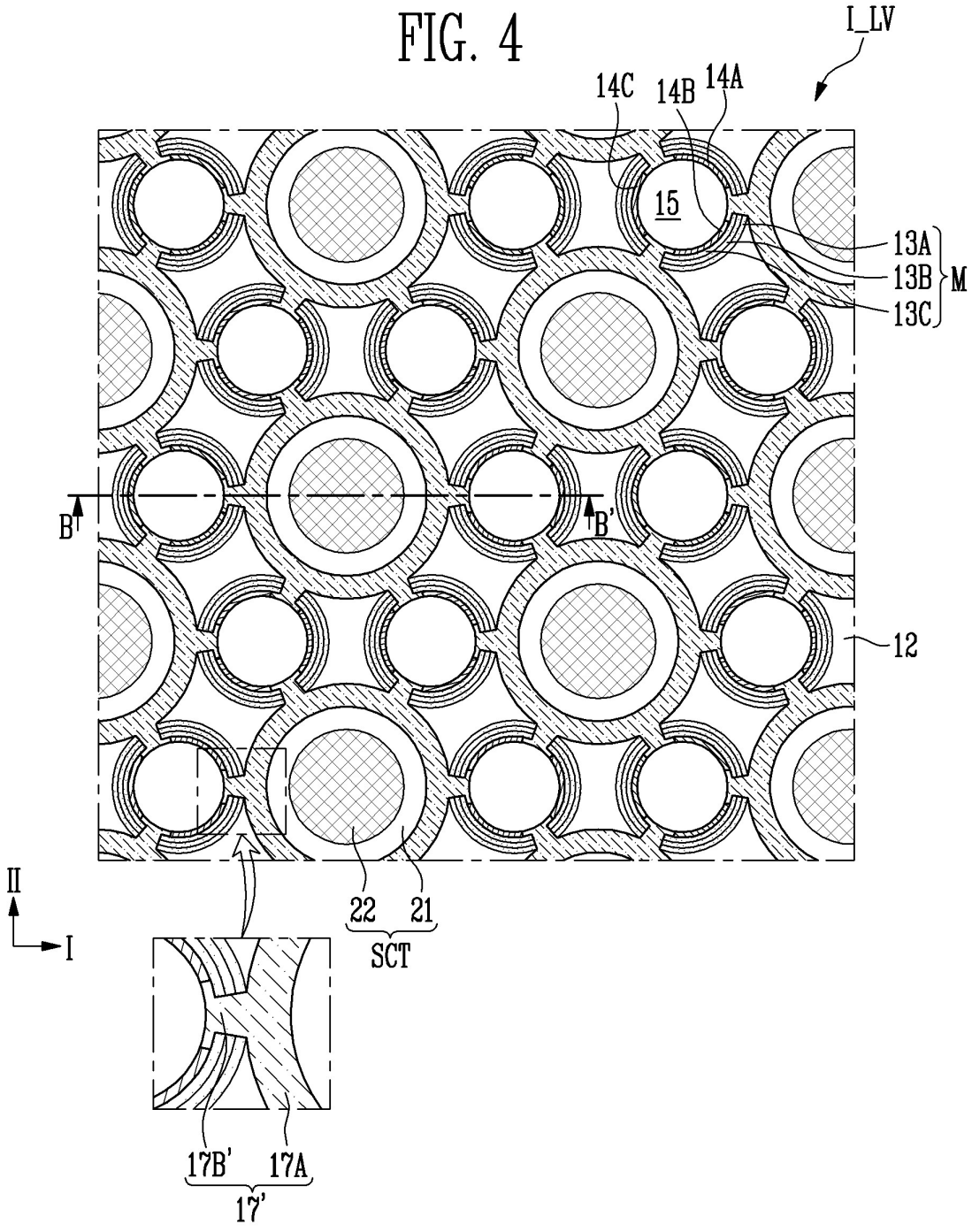


FIG. 5A

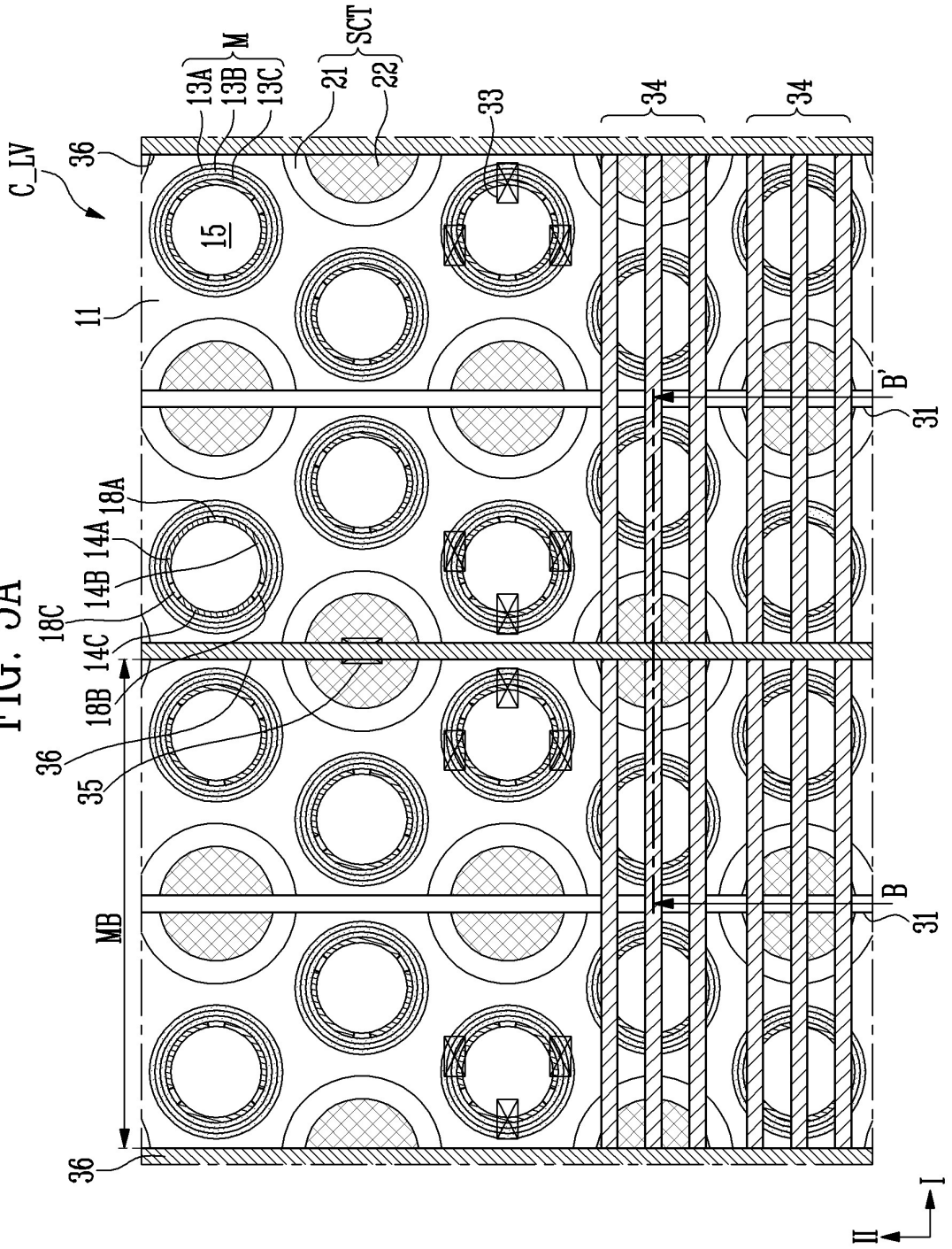

C_LV
36
13A
13B
13C
M
21
22
SCT
33
34
34
15
11
18A
14A
14B
18C
14C
18B
36
35
MB
36
B'
31
B
31
II
I

FIG. 5B

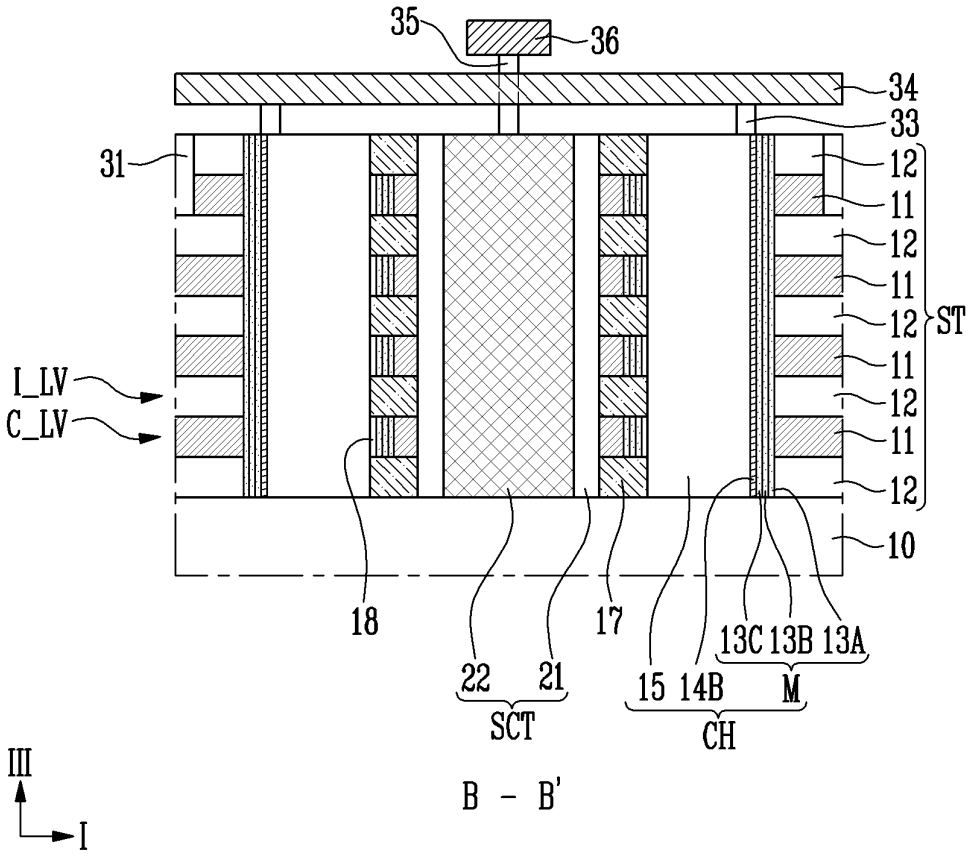

35
36
34
33
31
12
11
12
11
12
ST
11
12
11
12
I_LV
C_LV
10
18
17
13C 13B 13A
22
21
15
14B
M
SCT
CH
III
I
B - B'

FIG. 6A

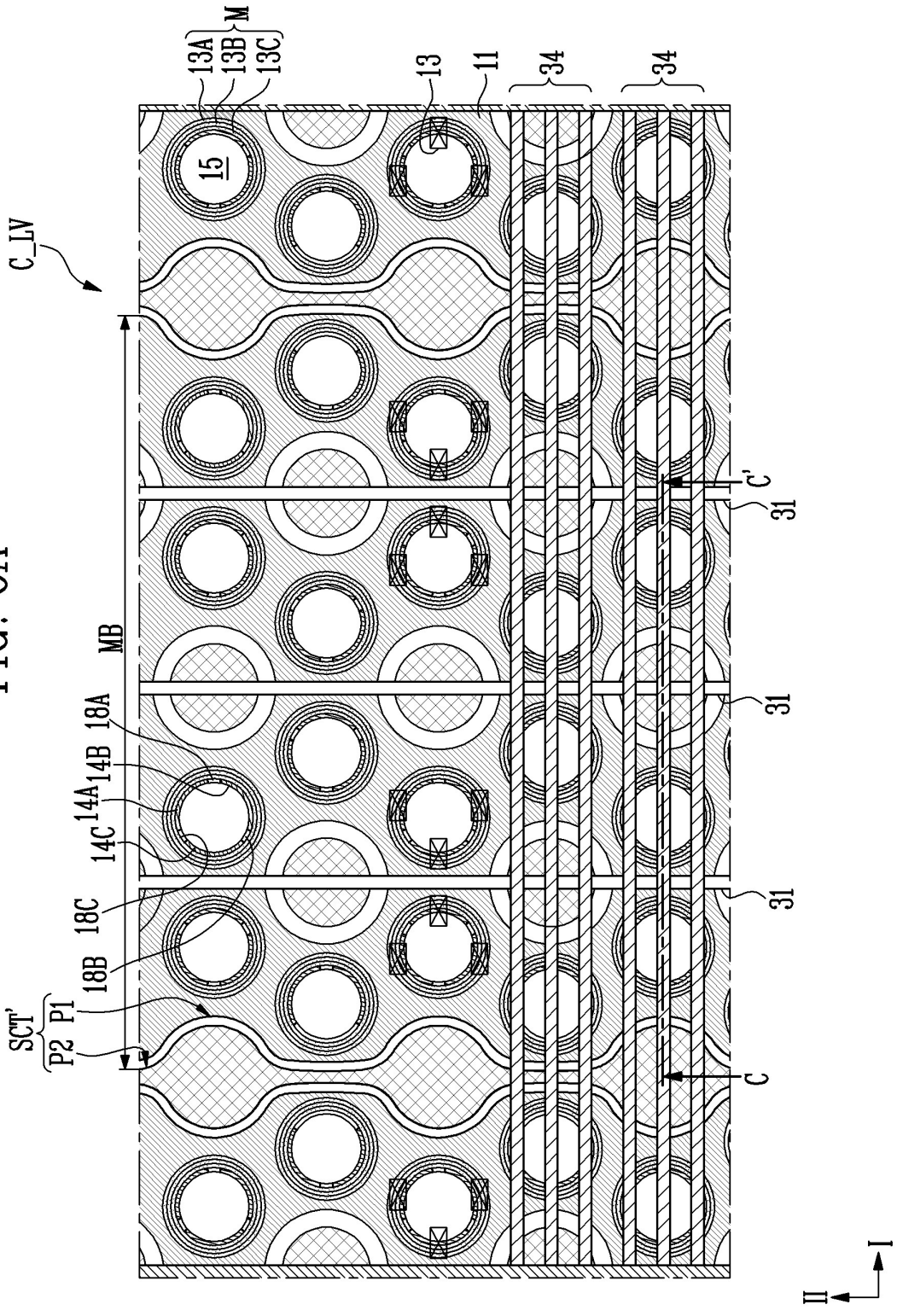

C_LV
SCT'
P2
P1
MB
M
13A
13B
13C
13
11
34
34
15
18A
14B
14A
14C
18C
18B
31
31
31
C
C'
II
I

FIG. 6B

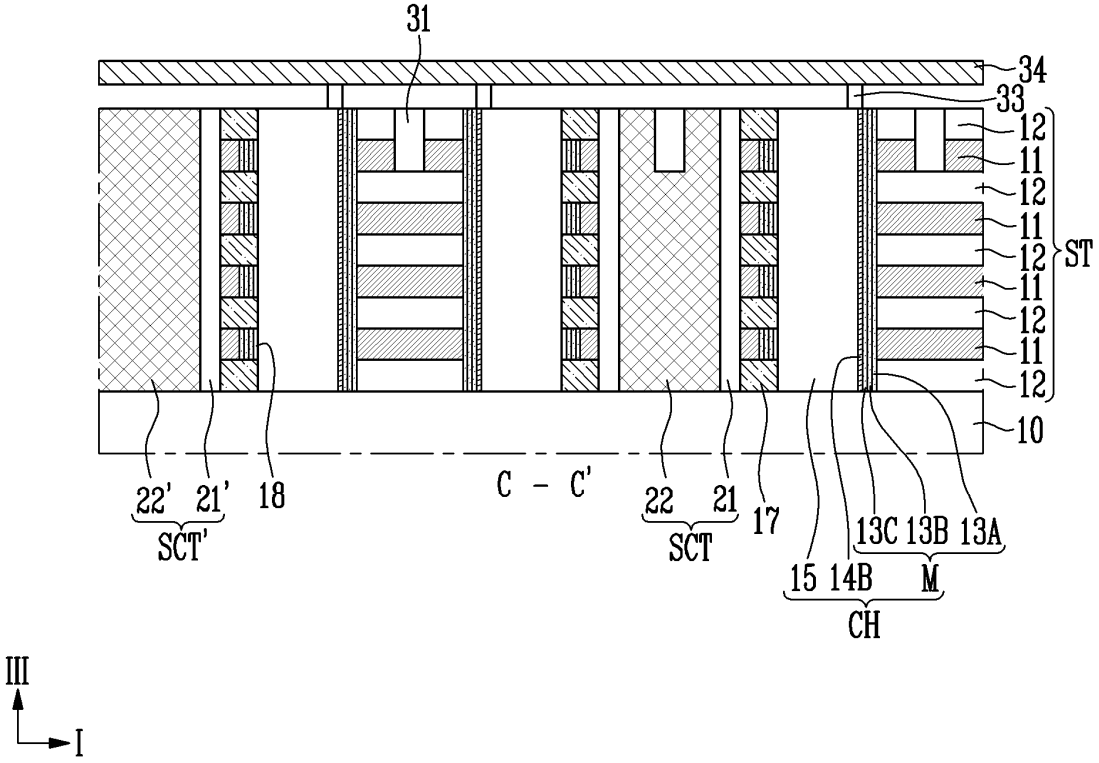

31
34
33
12
11
12
11
12
11
12
11
12
ST
10
22'
21'
18
C - C'
22
21
17
15
14B
13C
13B
13A
M
SCT'
SCT
CH
III
I

FIG. 7A

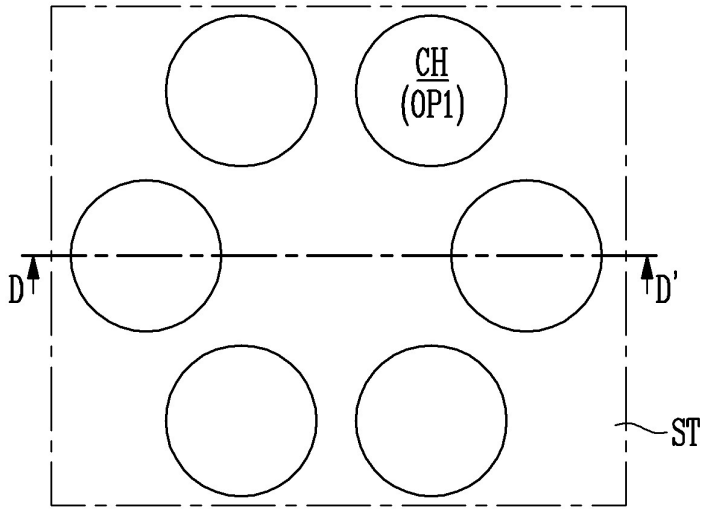

CH
(OP1)
D
D'
ST
II
I

FIG. 7B

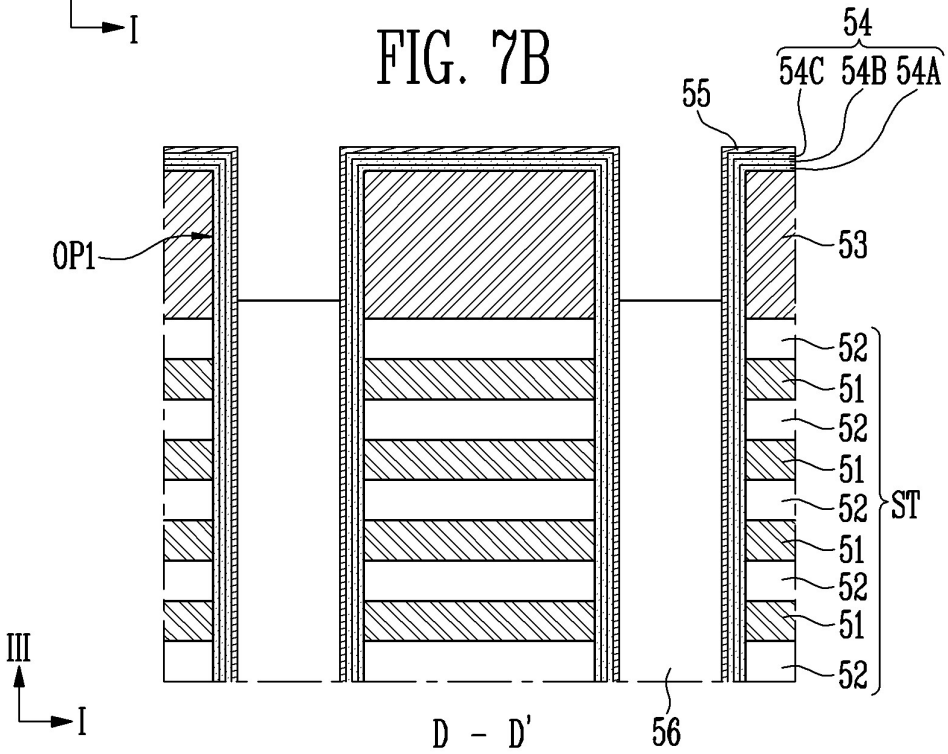

54
54C 54B 54A
55
OP1
53
52
51
52
51
52
51
52
51
52
ST
III
I
D - D'
56

FIG. 7C

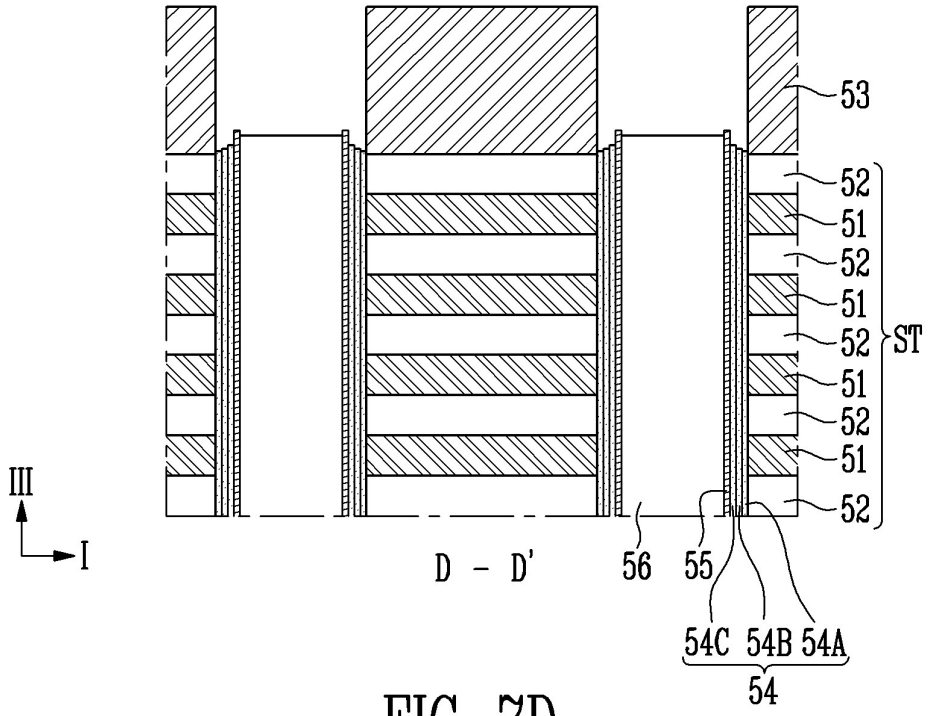

53
52
51
52
51
52
51
52
51
52
ST
III
I
D - D'
56
55
54C
54B
54A
54

FIG. 7D

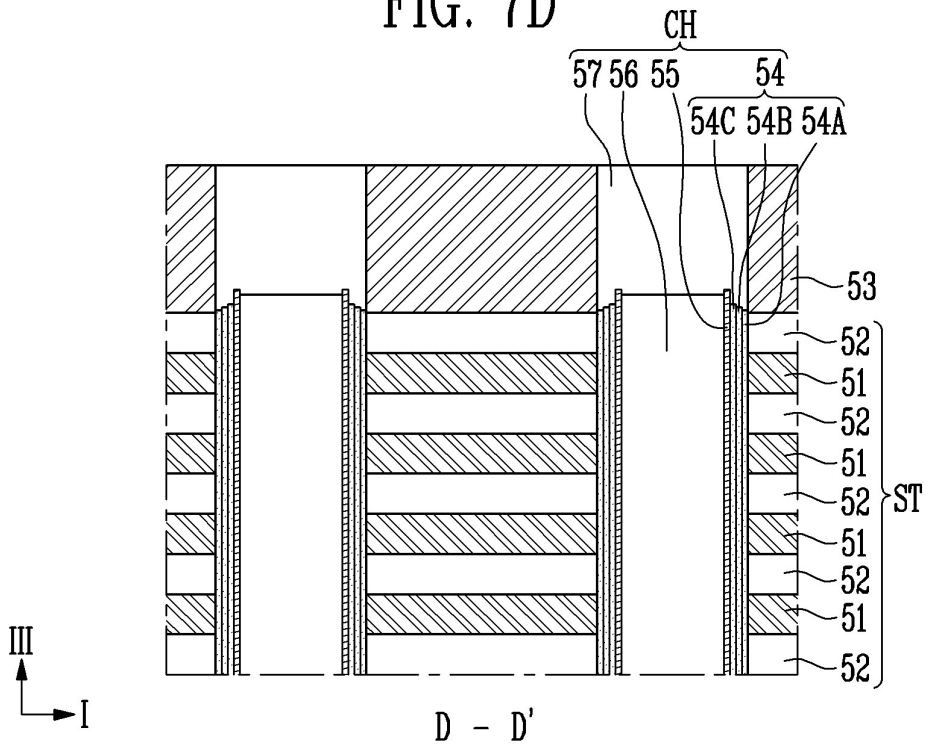

CH
57
56
55
54
54C
54B
54A
53
52
51
52
51
52
51
52
51
52
ST
III
I
D - D'

FIG. 8A

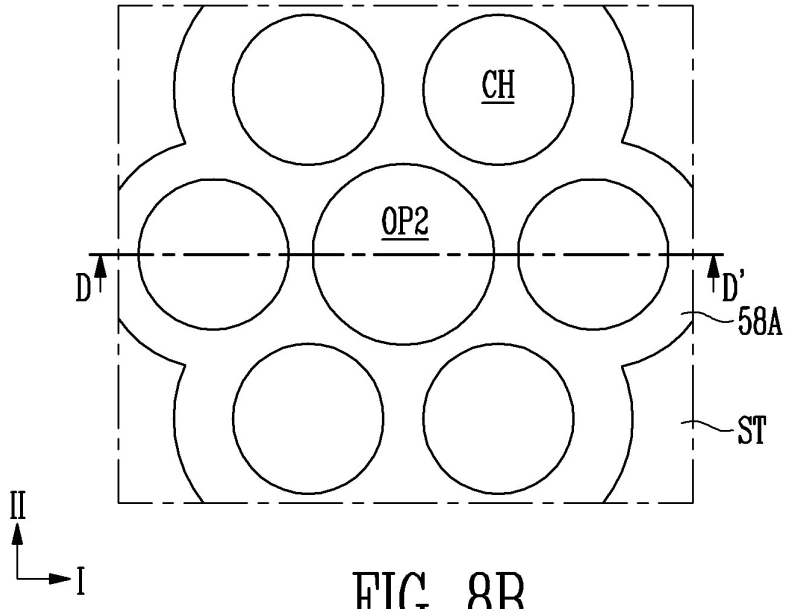

CH
OP2
D
D'
58A
ST
II
I

FIG. 8B

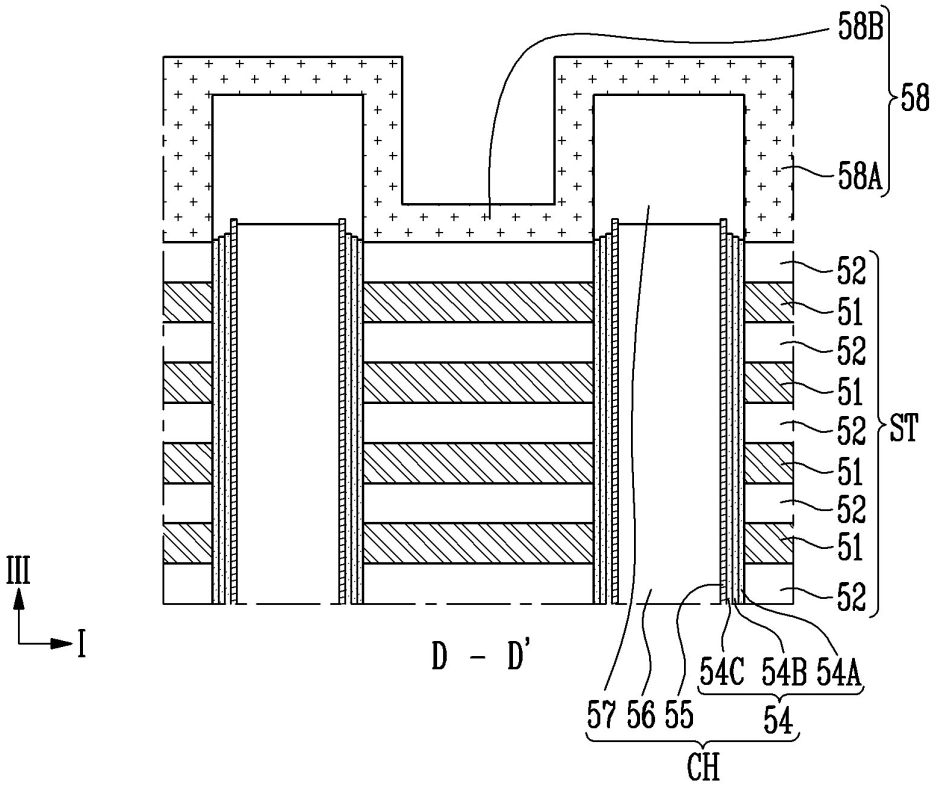

58B
58
58A
52
51
52
51
52
51
52
51
52
ST
III
I
D - D'
54C 54B 54A
54
57 56 55
CH

FIG. 8C

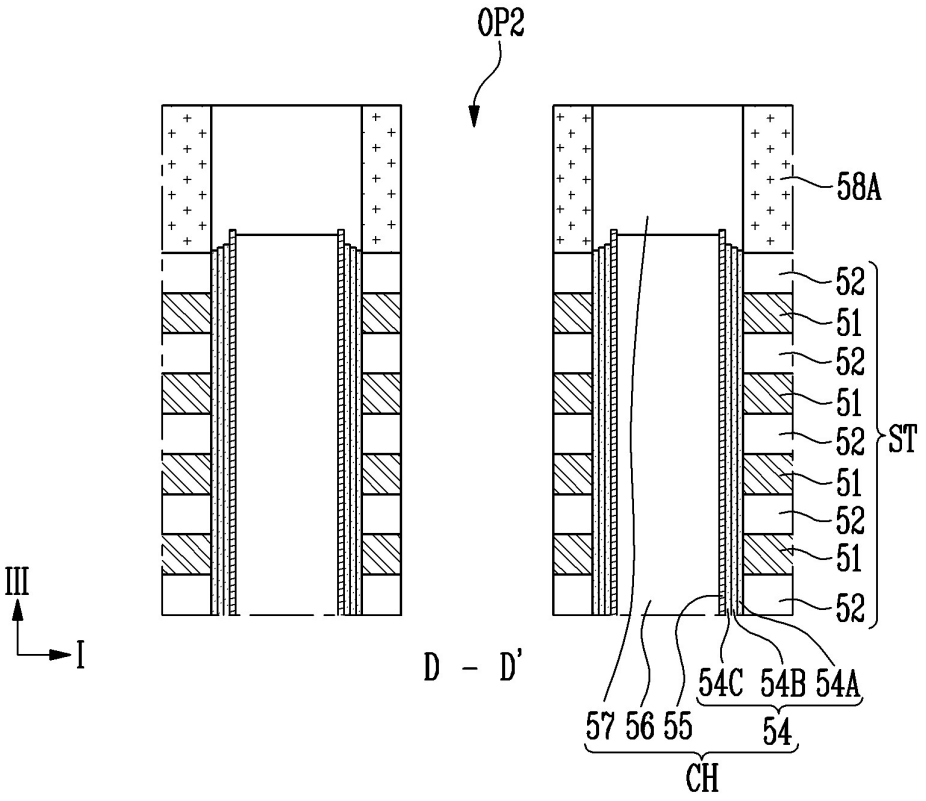

OP2
58A
52
51
52
51
52
51
52
51
52
ST
III
I
D - D'
54C
54B
54A
57
56
55
54
CH

FIG. 9A

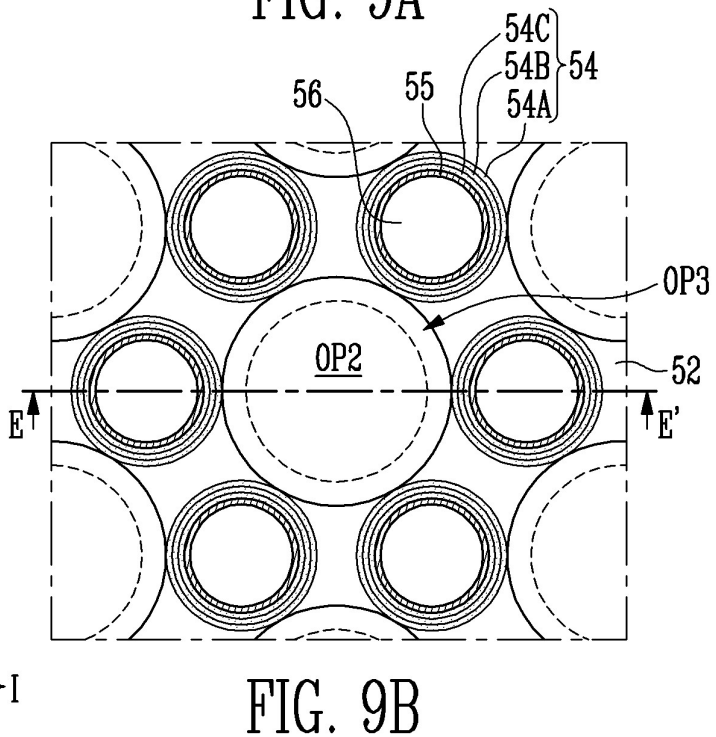

54C
54B
54A
54
56
55
OP3
OP2
52
E
E'
II
I

FIG. 9B

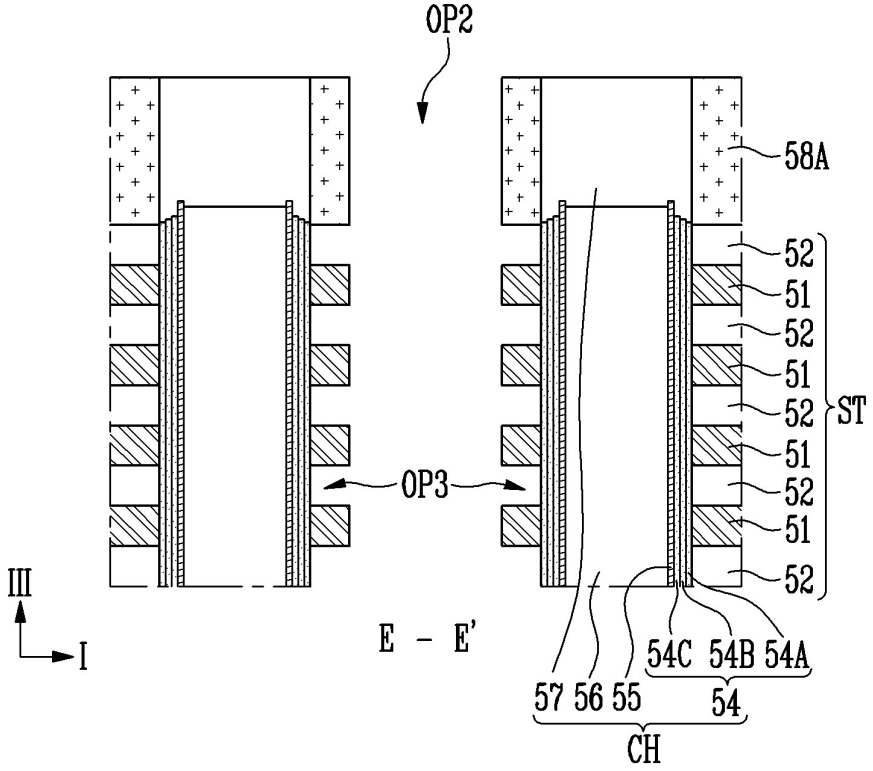

OP2
58A
52
51
52
51
52
51
52
51
52
ST
OP3
III
I
E - E'
54C 54B 54A
57 56 55
54
CH

FIG. 10A

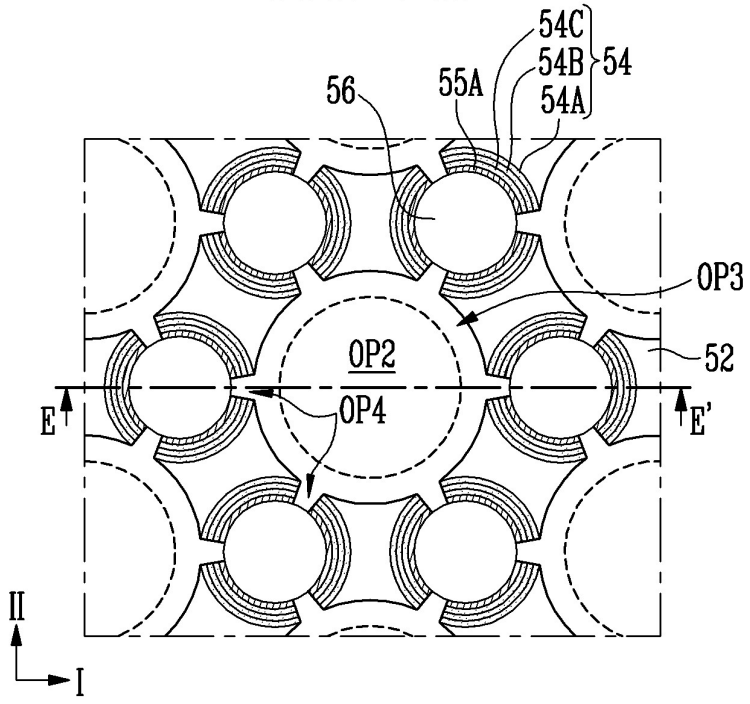


FIG. 10B

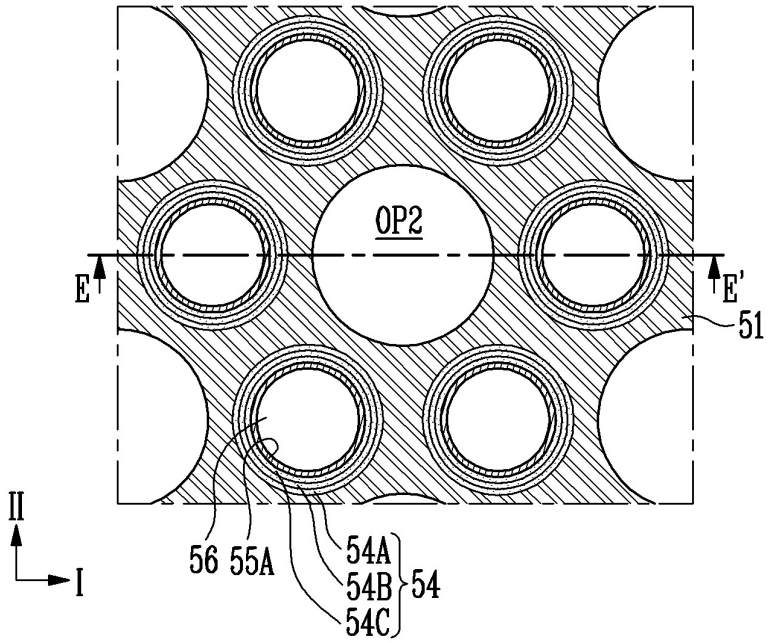


FIG. 10C

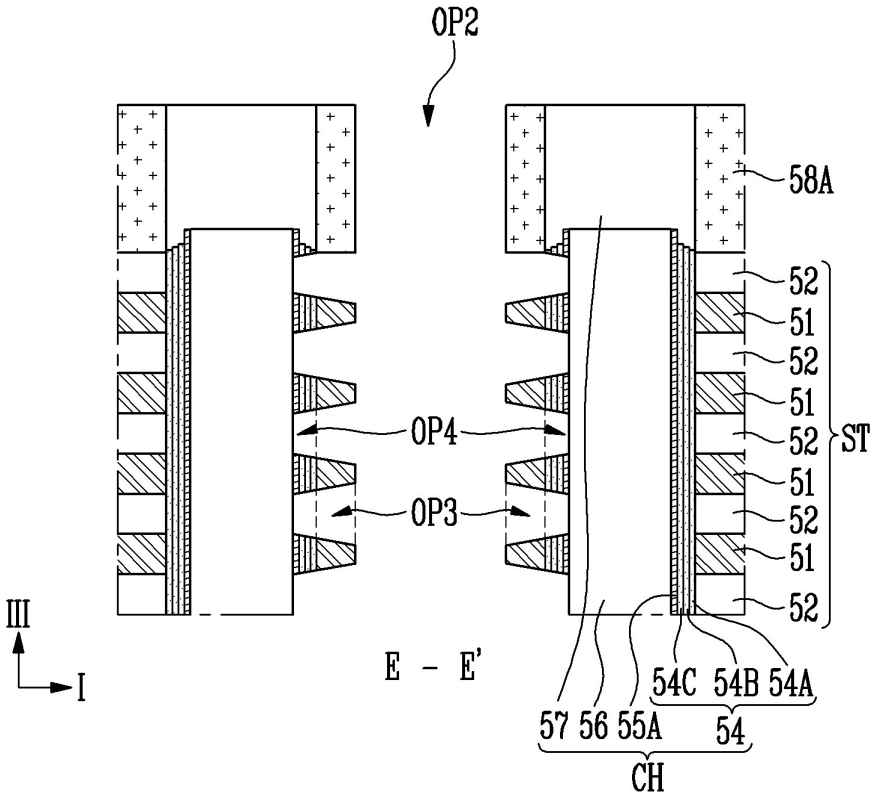

OP2
58A
52
51
52
51
52
51
52
51
52
ST
OP4
OP3
III
I
E - E'
54C
54B
54A
57
56
55A
54
CH

FIG. 11A

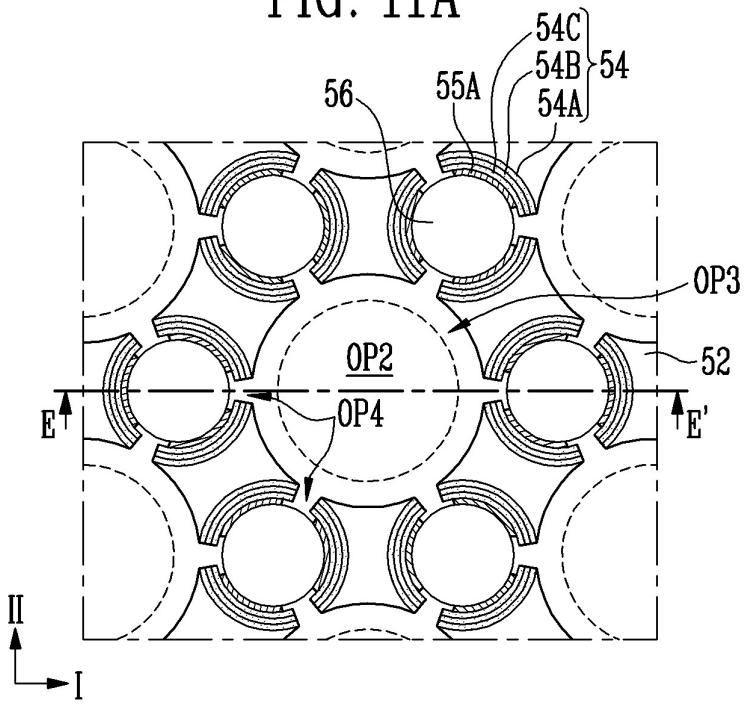


FIG. 11B

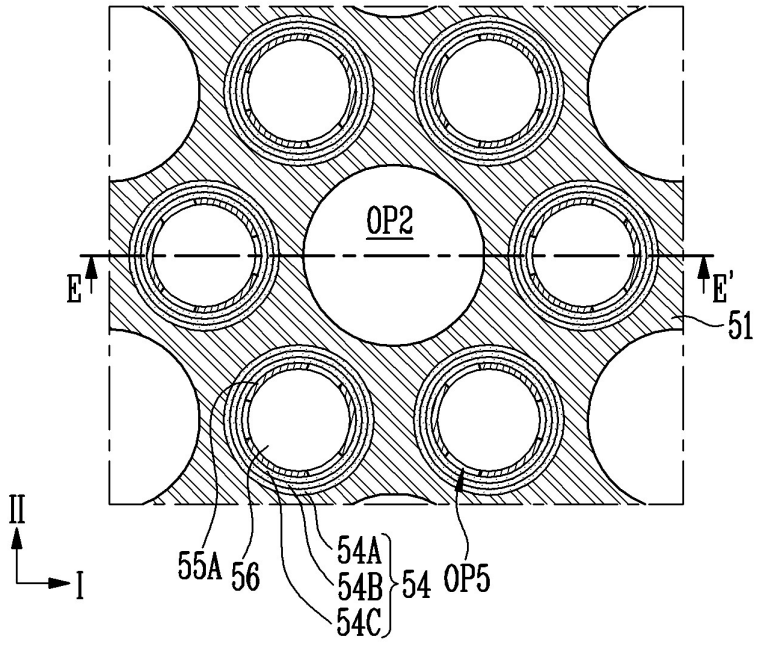


FIG. 11C

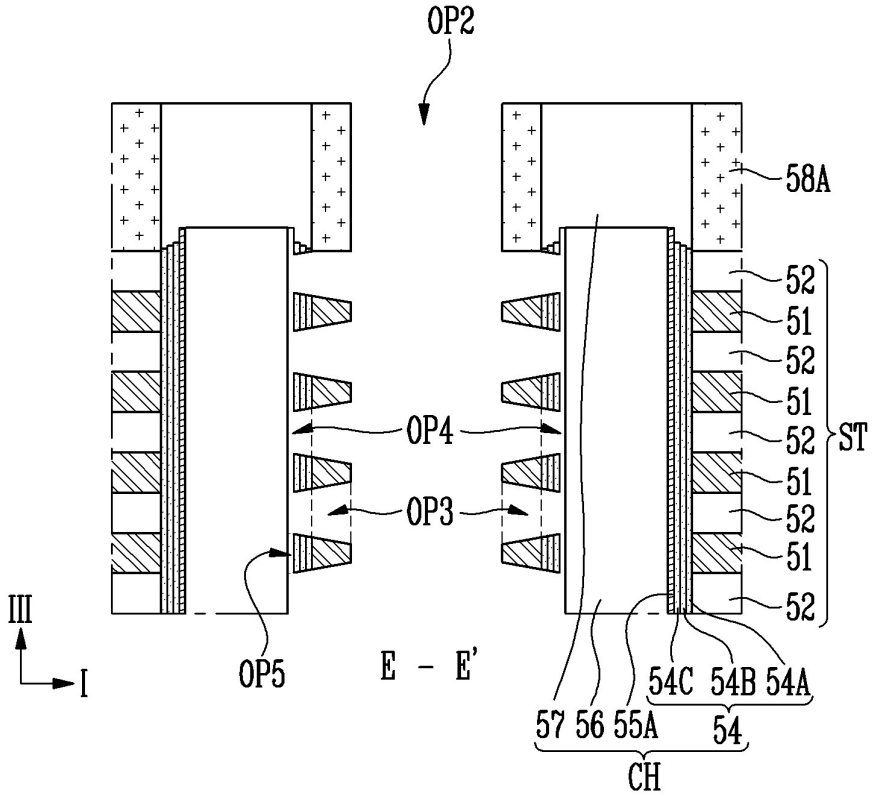

OP2
58A
52
51
52
51
52
51
52
51
52
ST
OP4
OP3
OP5
III
I
E - E'
54C 54B 54A
57 56 55A
54
CH

FIG. 12A

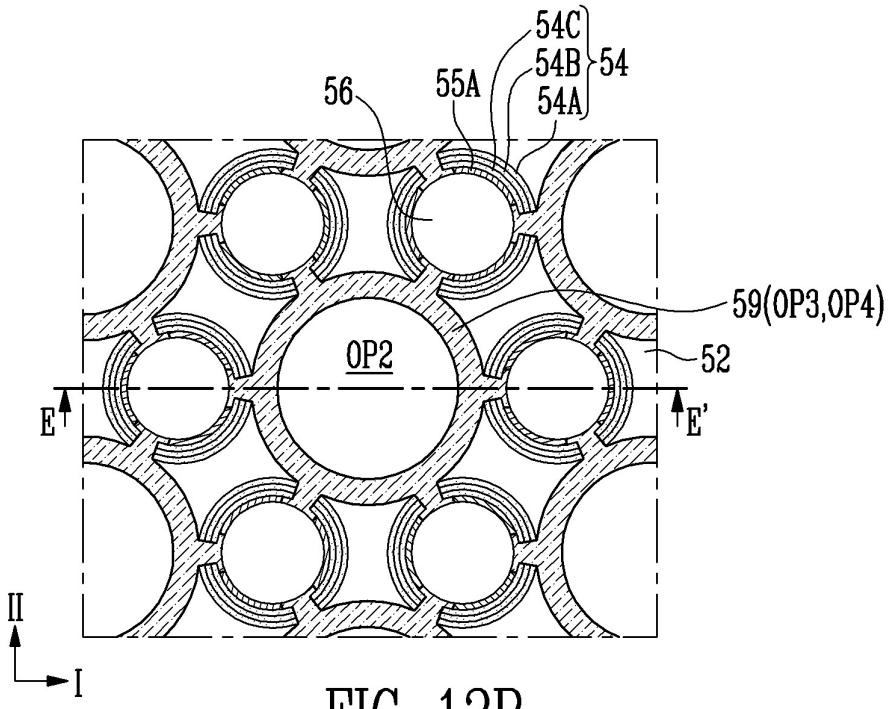


FIG. 12B

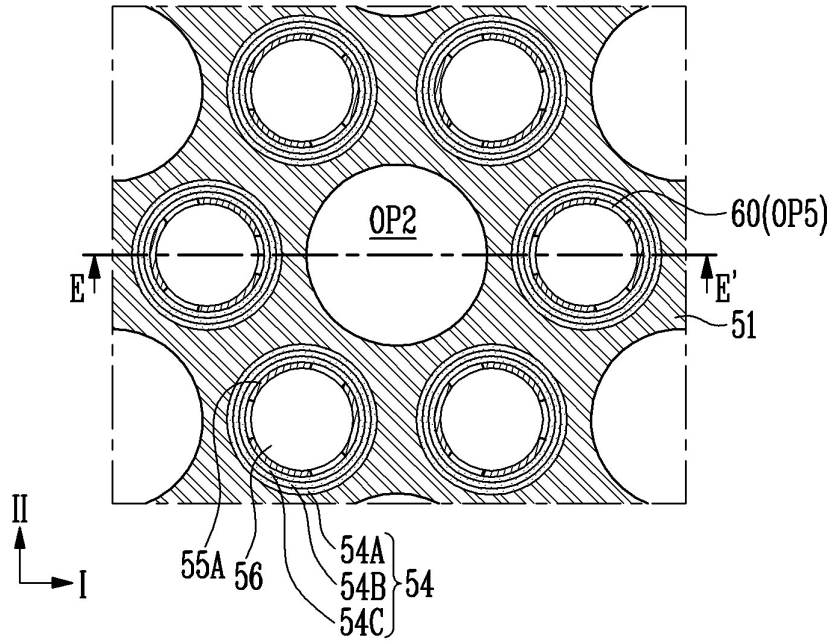


FIG. 12C

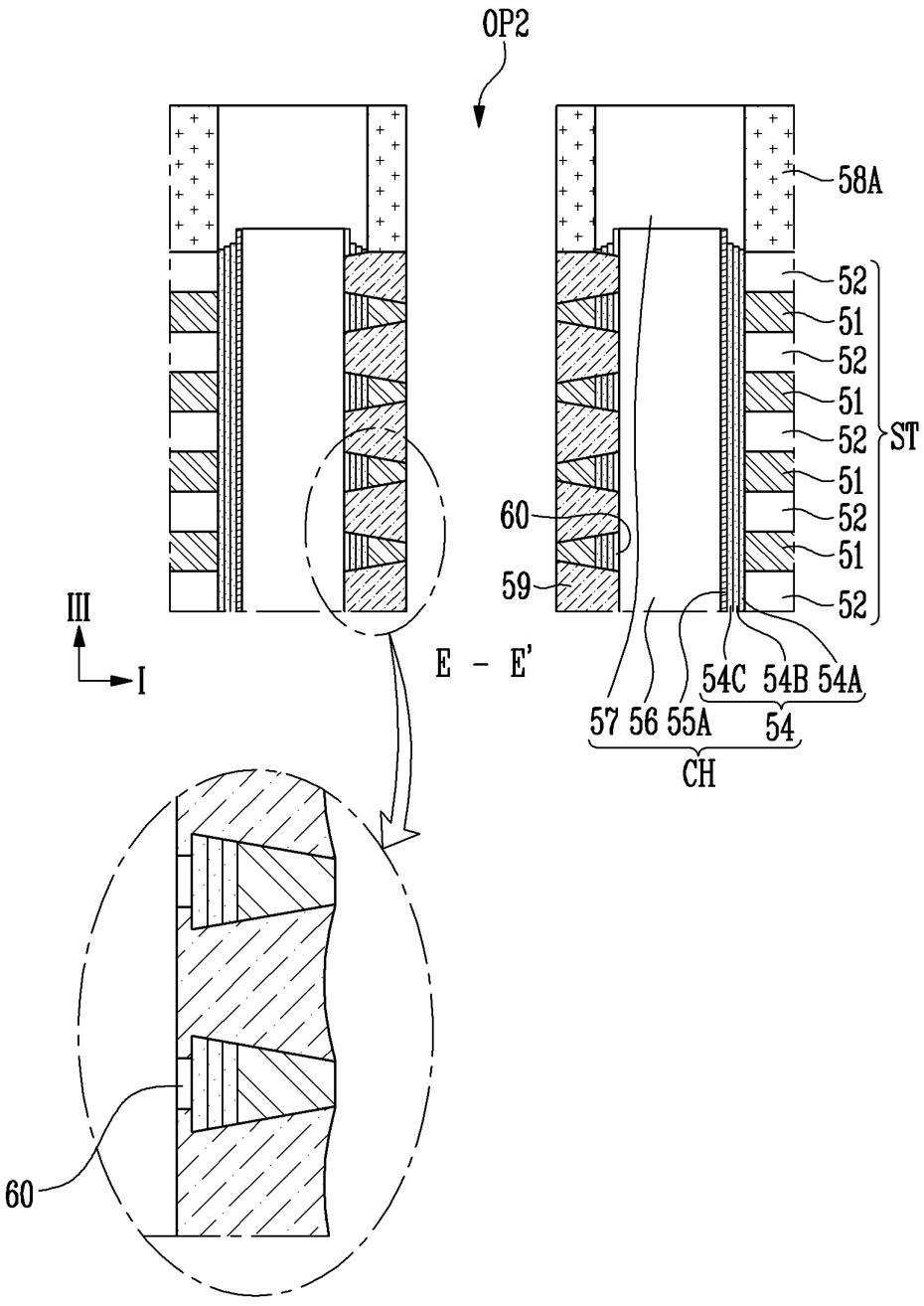

OP2
58A
52
51
52
51
52
51
52
51
52
ST
60
59
III
I
E - E'
54C 54B 54A
57 56 55A
54
CH
60

FIG. 13A

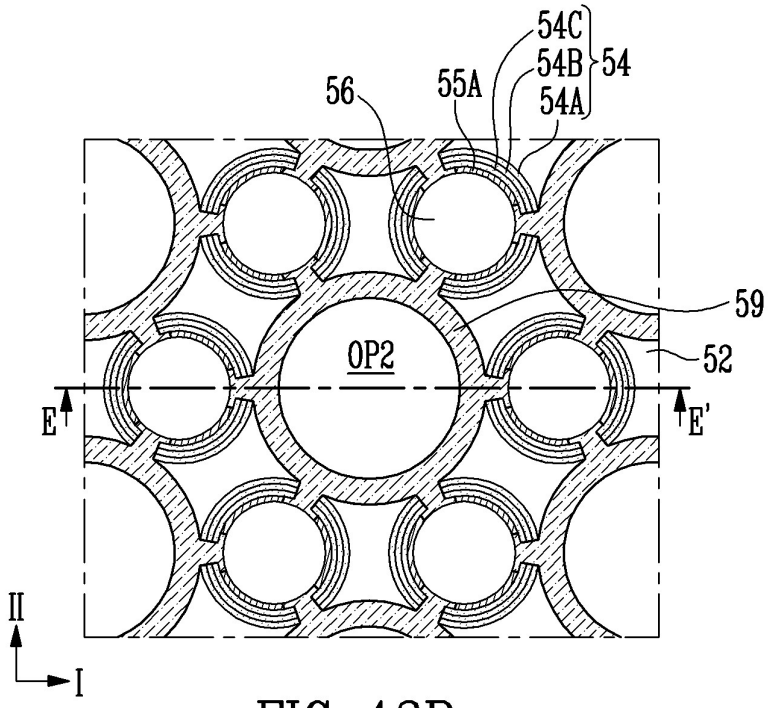


FIG. 13B

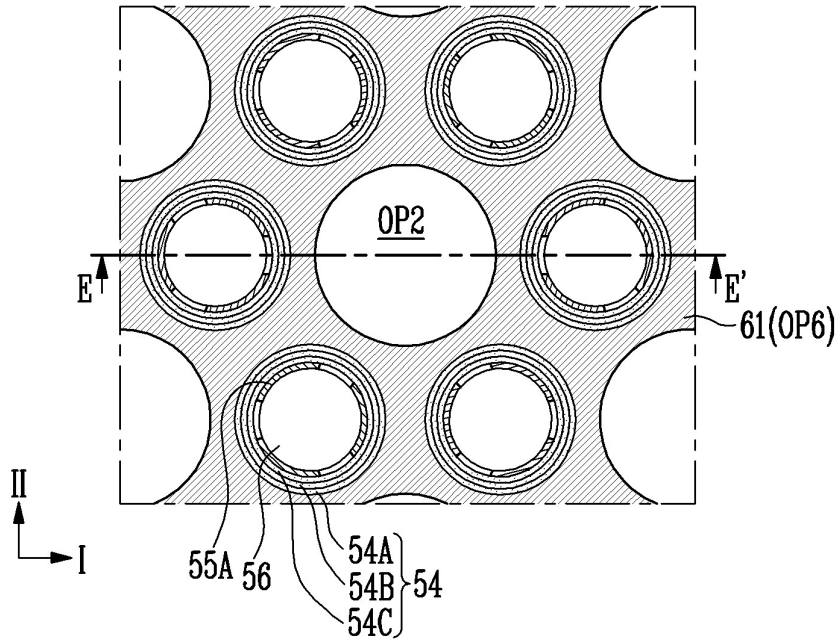


FIG. 13C

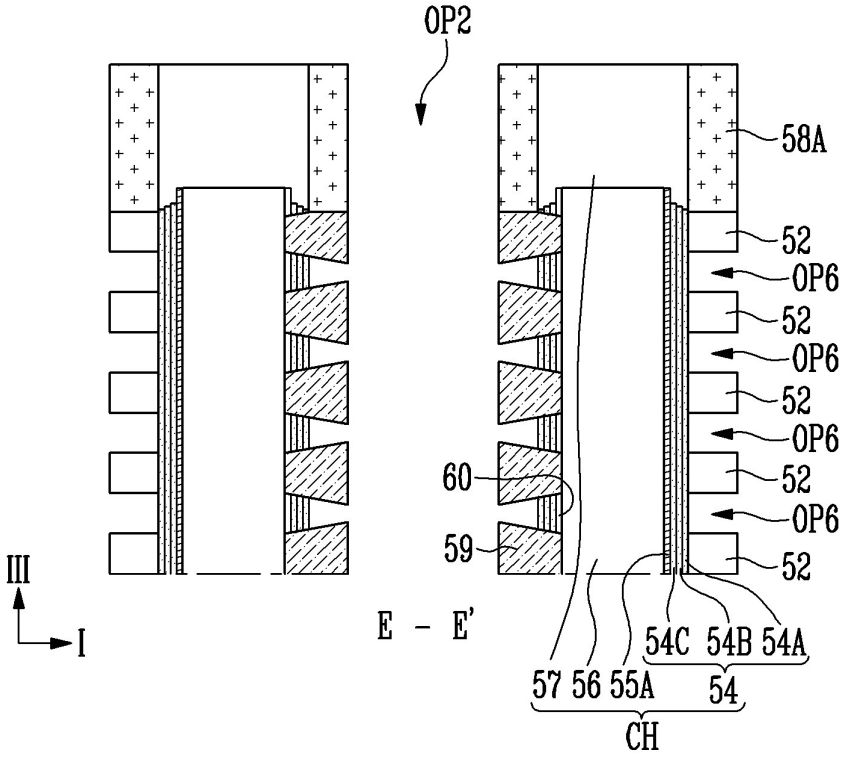


FIG. 13D

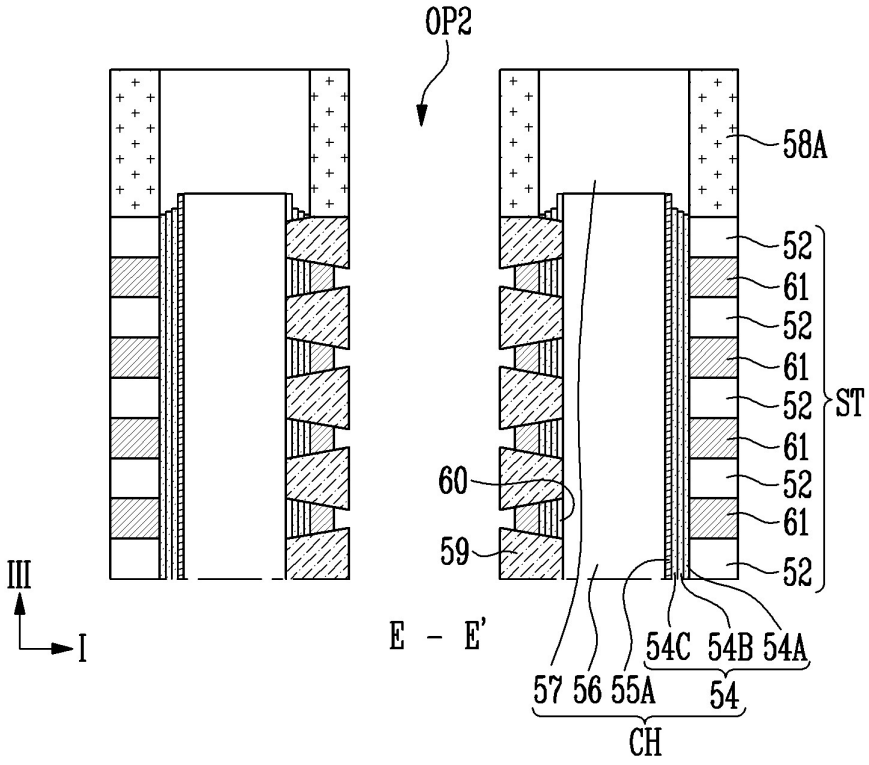


FIG. 14A

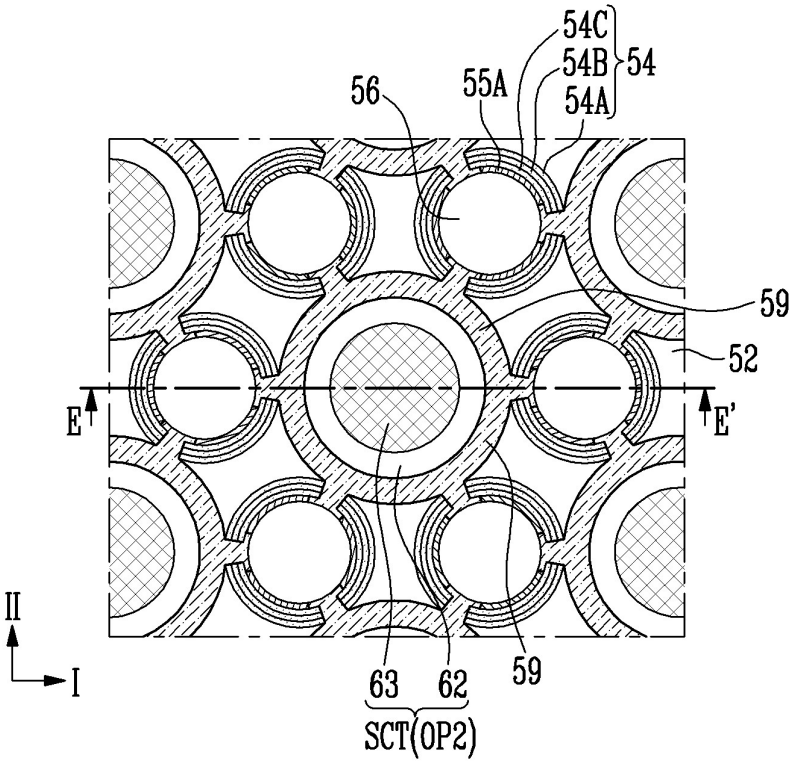


FIG. 14B

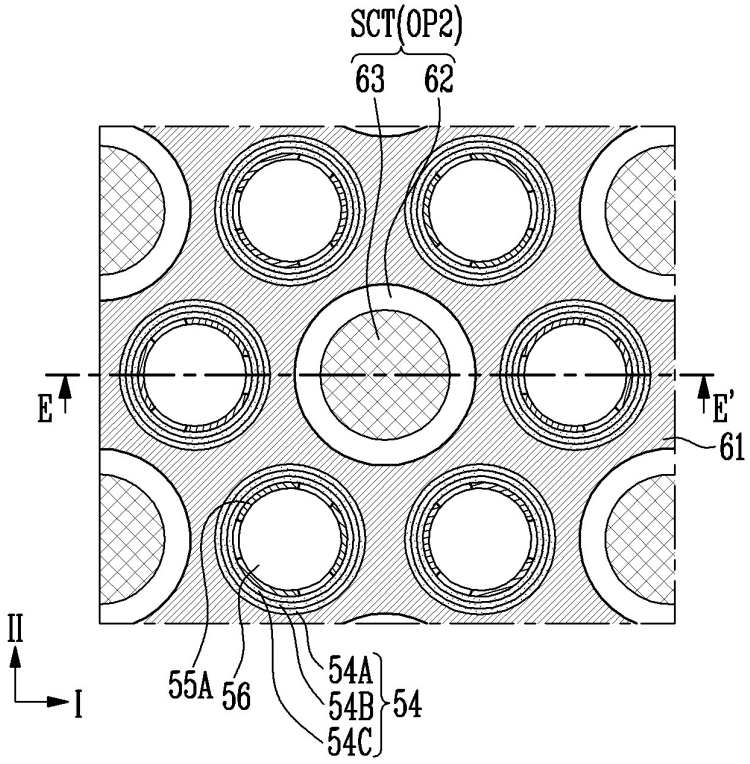


FIG. 14C

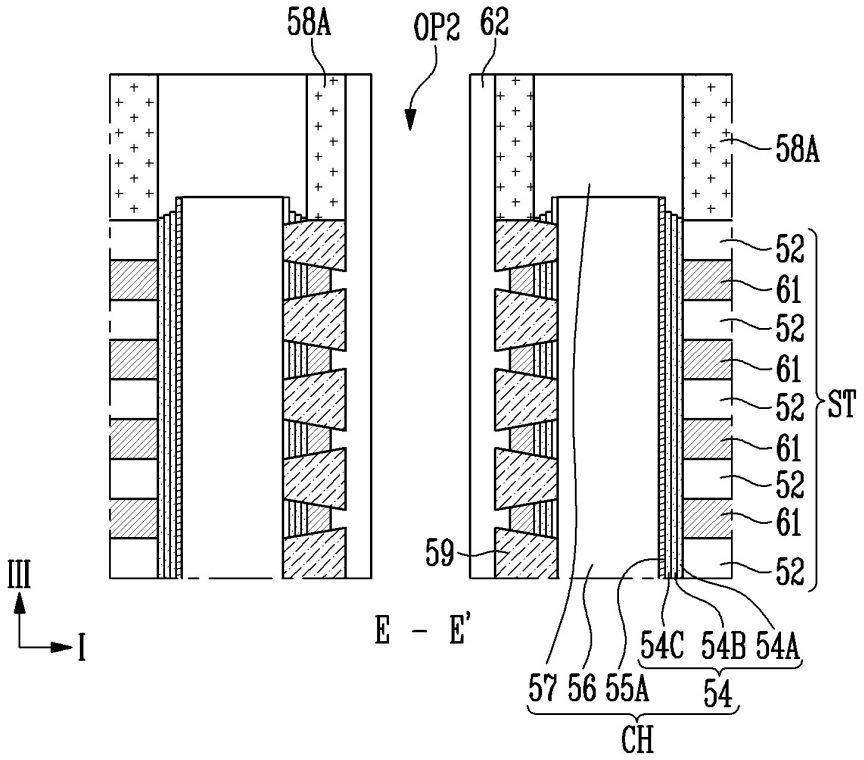


FIG. 14D

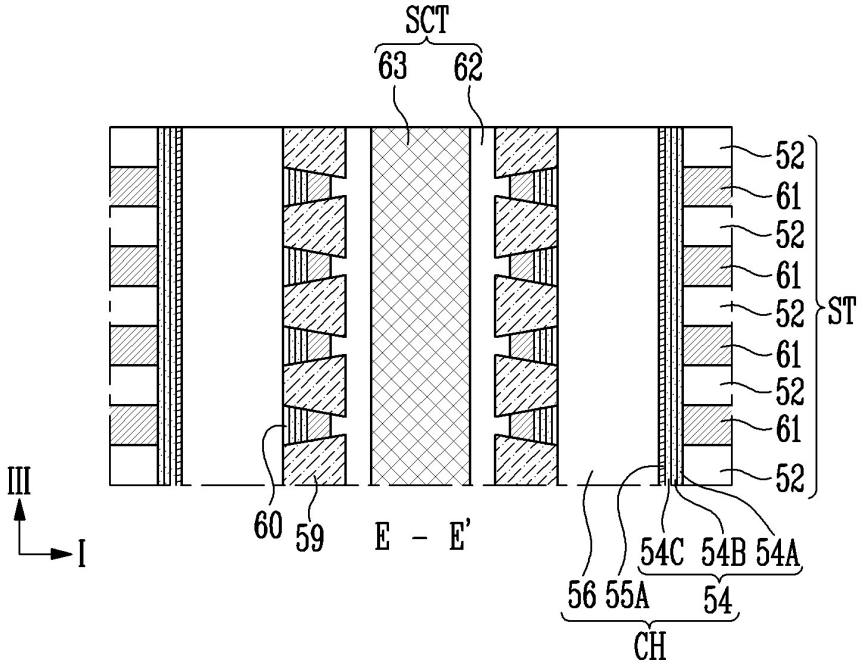


FIG. 15A

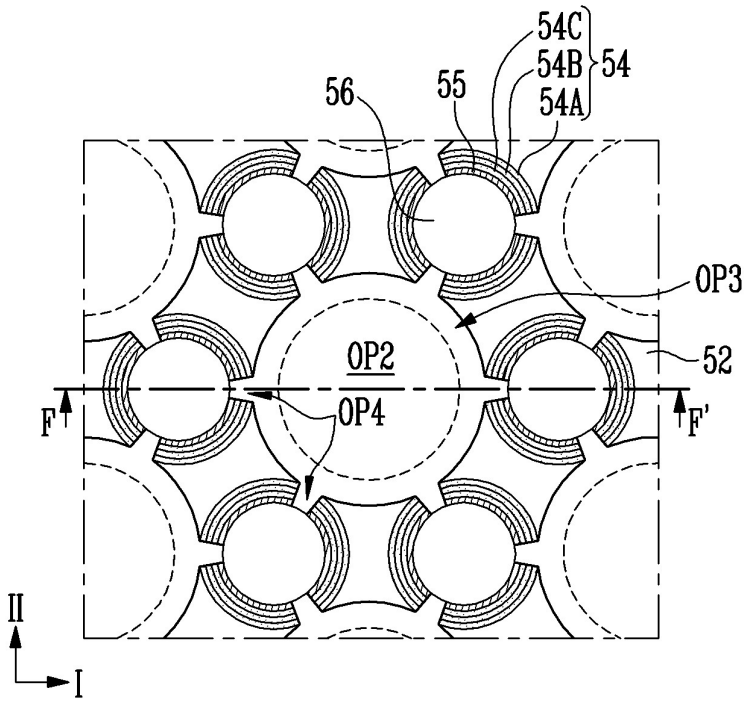


FIG. 15B

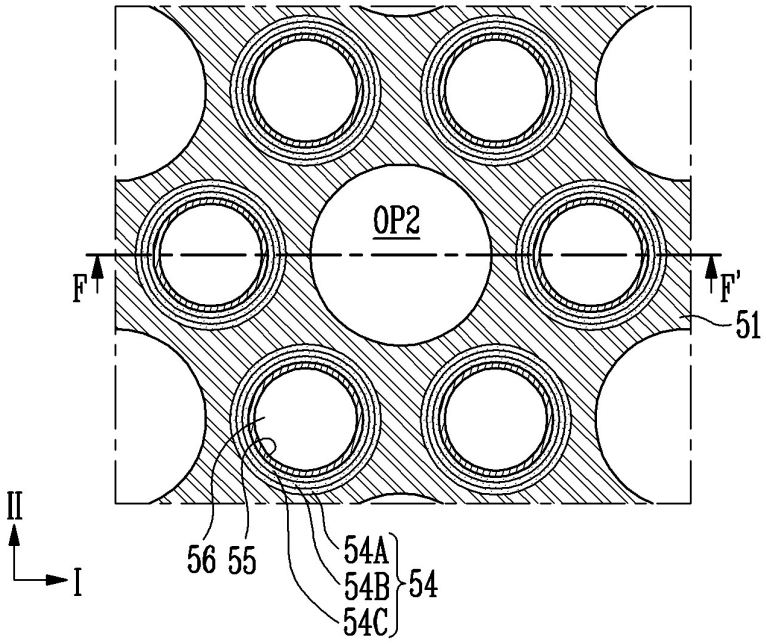


FIG. 15C

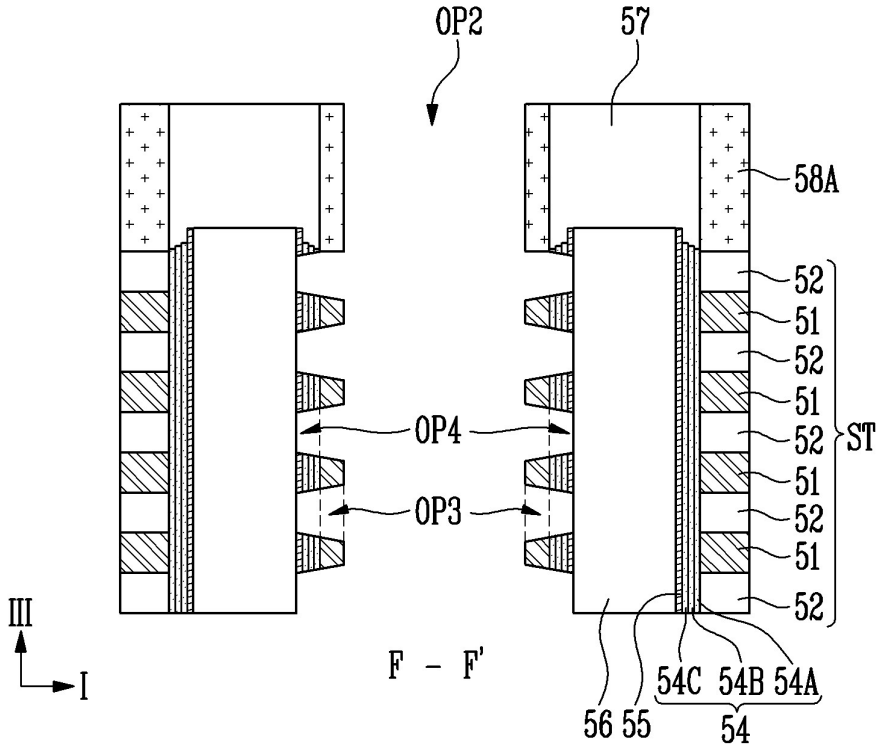

OP2
57
58A
52
51
52
51
52
51
52
51
52
ST
OP4
OP3
III
I
F - F'
56
55
54C
54B
54A
54

FIG. 16A

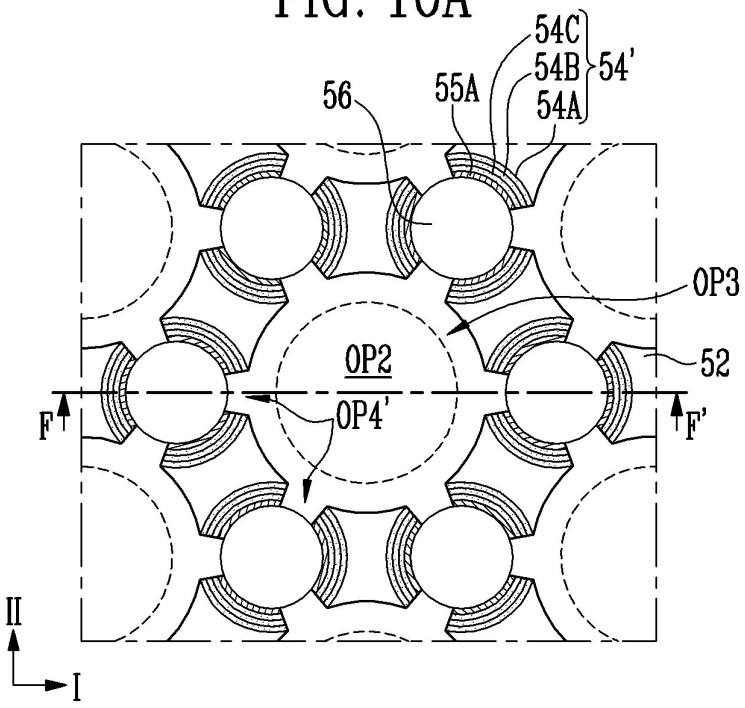


FIG. 16B

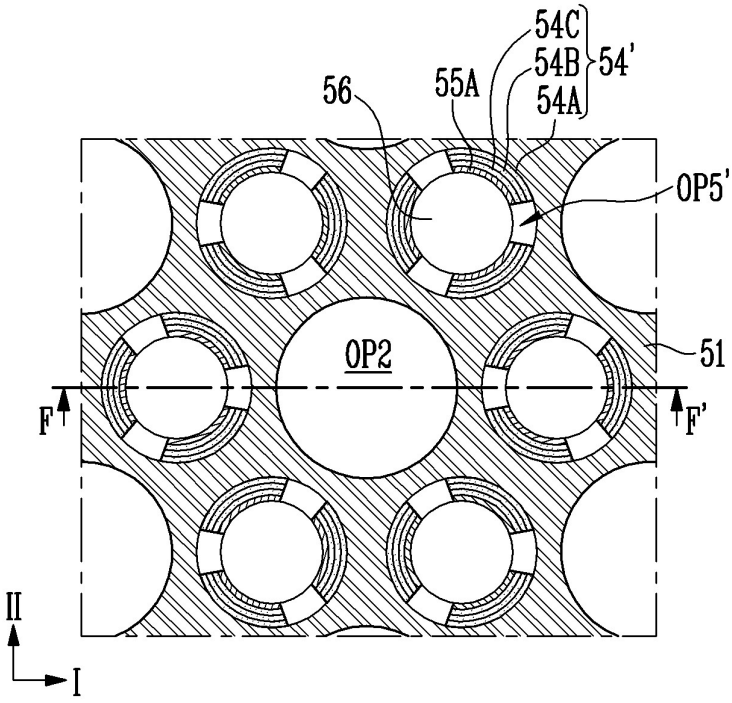


FIG. 16C

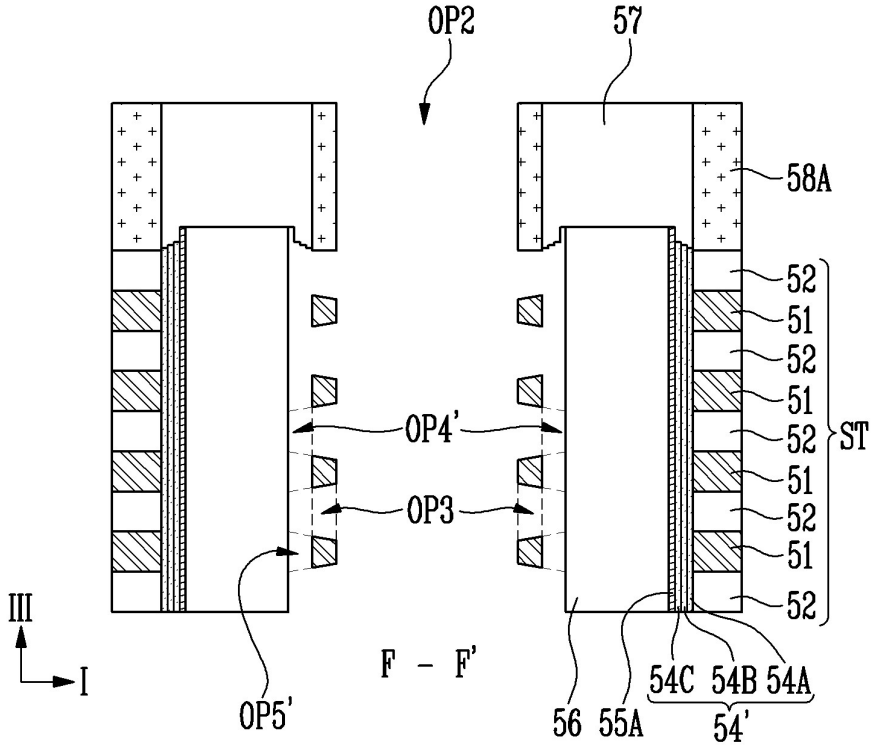

OP2
57
58A
52
51
52
51
52
51
52
51
52
ST
OP4'
OP3
III
I
F - F'
OP5'
56
55A
54C
54B
54A
54'

FIG. 17A

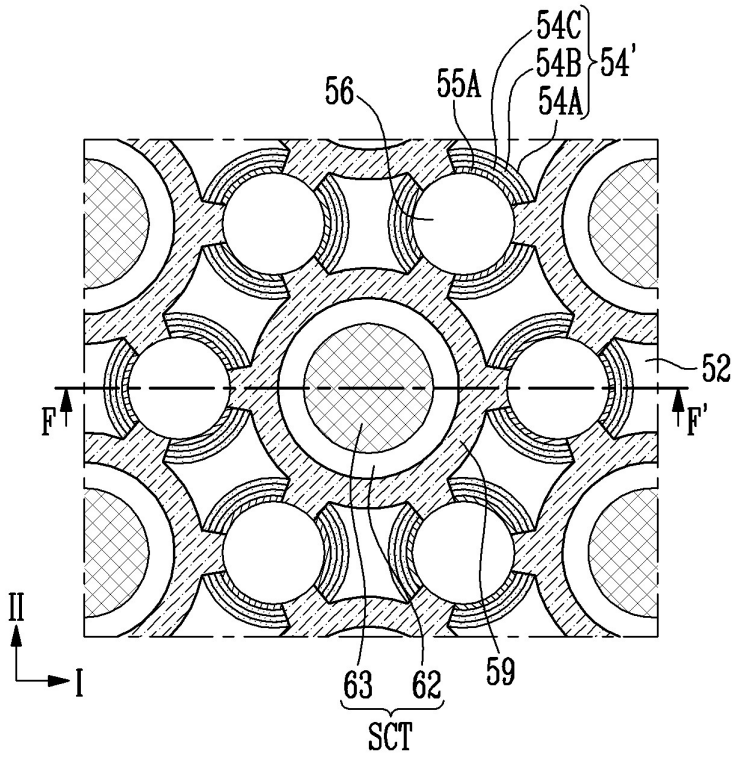


FIG. 17B

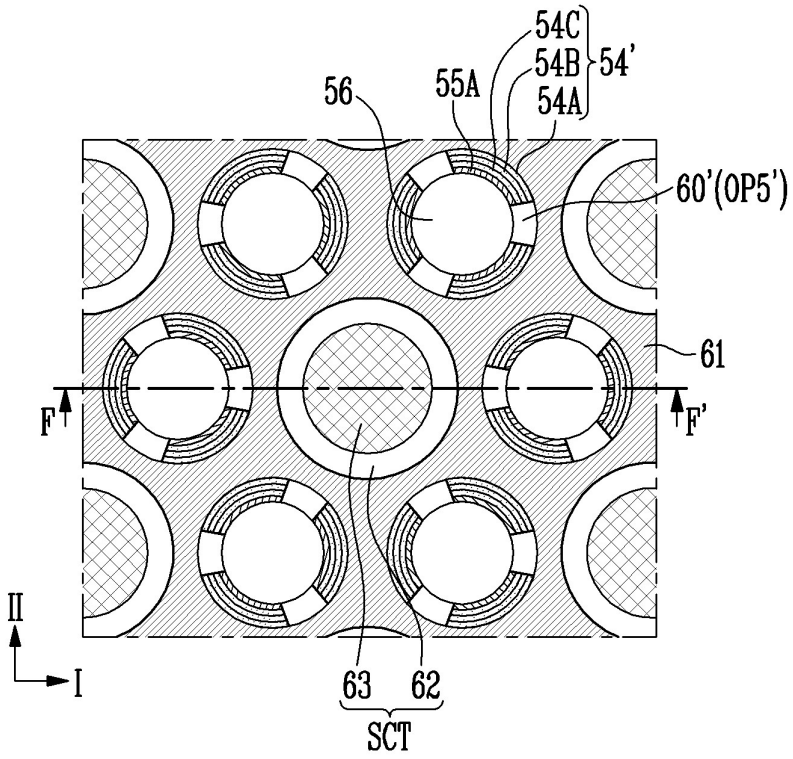


FIG. 17C

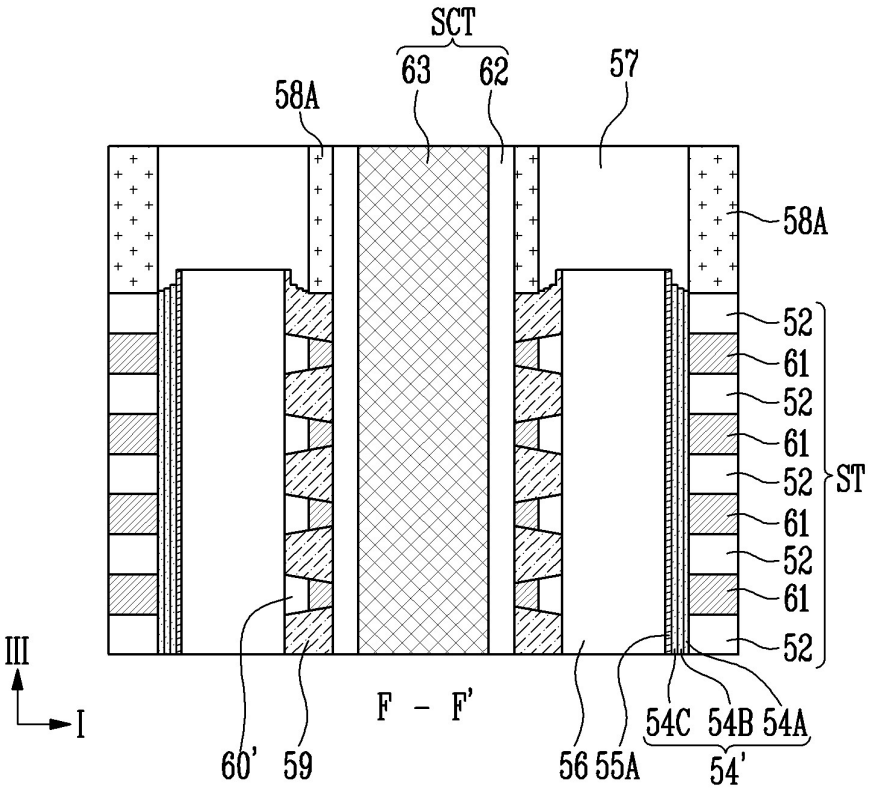

SCT
63
62
57
58A
58A
52
61
52
61
52
61
52
61
52
ST
III
I
F - F'
60'
59
56
55A
54C
54B
54A
54'

FIG. 18A

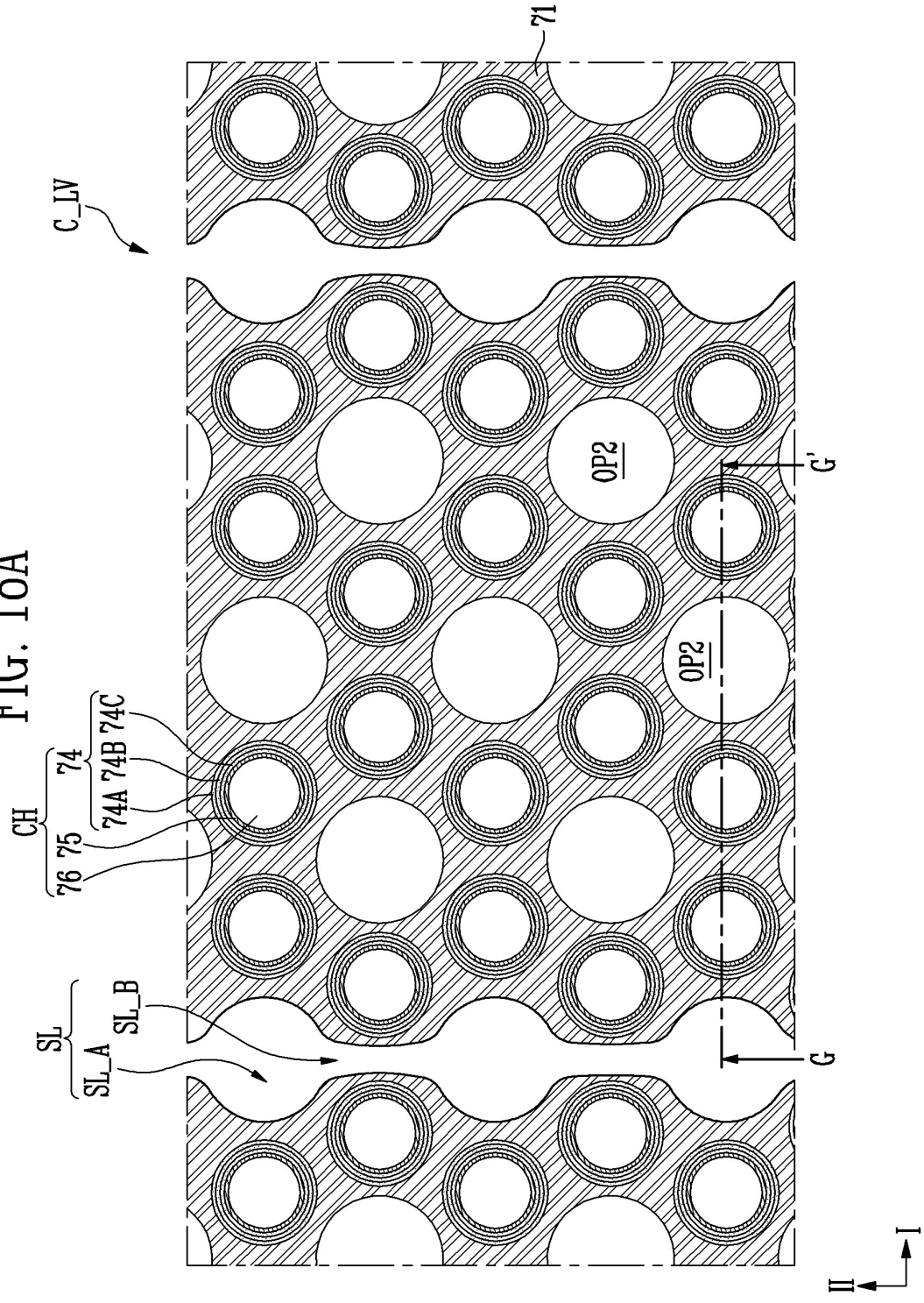


FIG. 18B

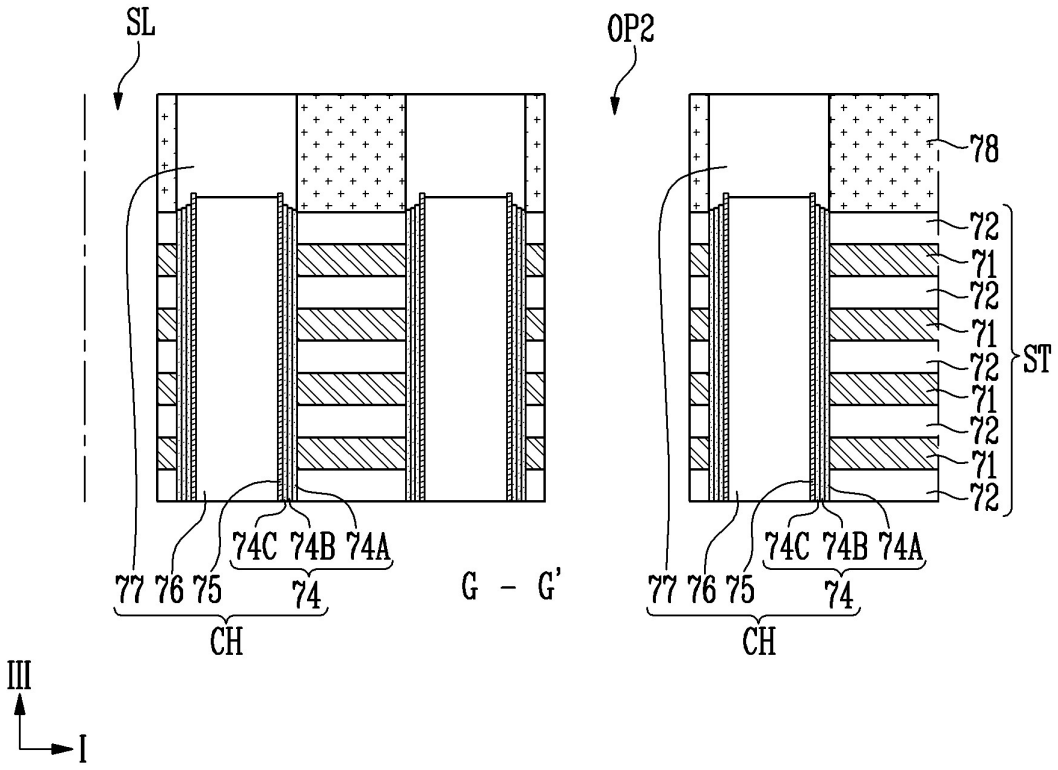

SL
OP2
78
72
71
72
71
72
71
72
71
72
ST
74C 74B 74A
77 76 75
74
G - G'
CH
III
I

FIG. 19A

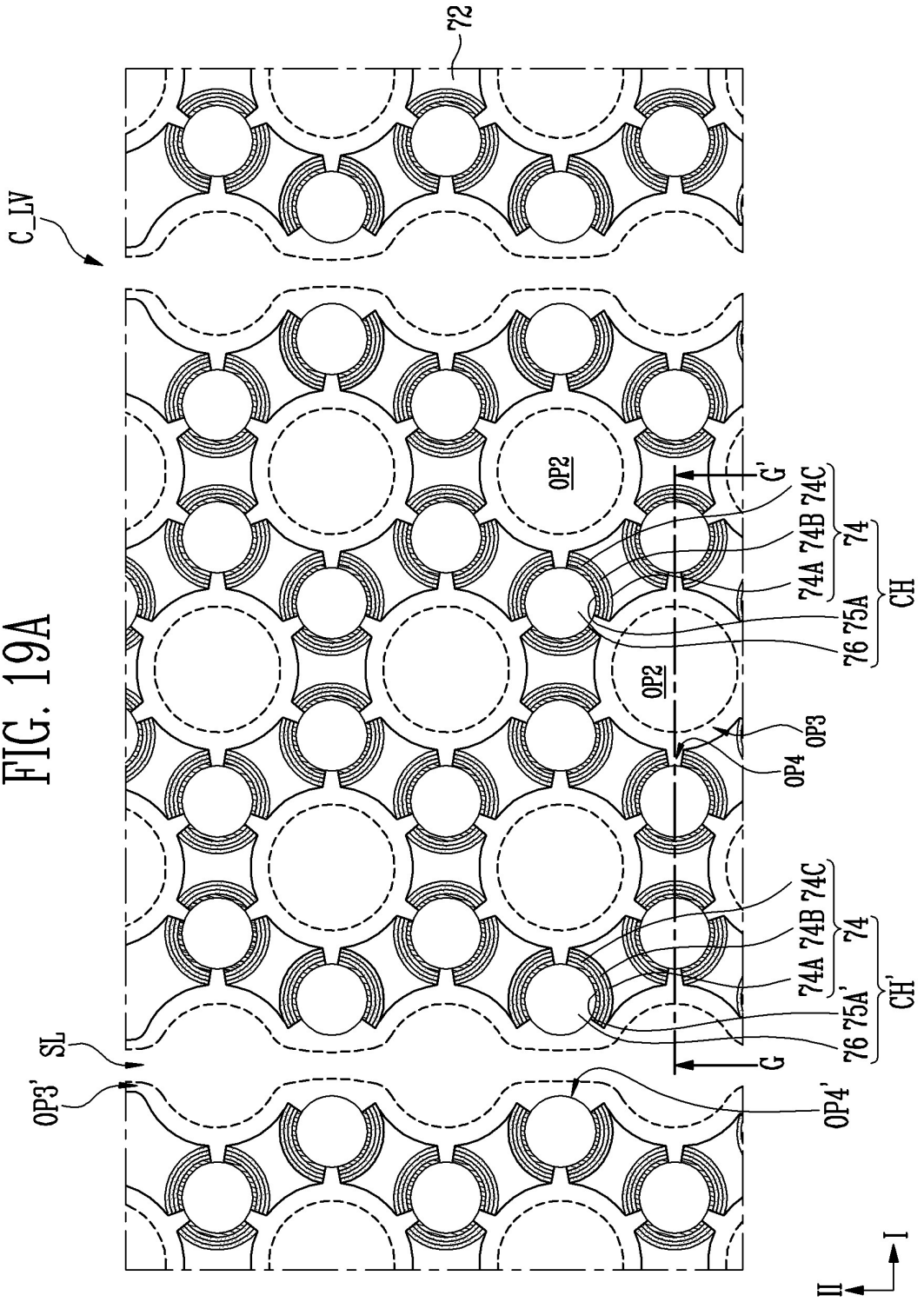

72
C_LV
OP2
G'
74A 74B 74C
74
CH
76 75A
OP2
OP3
OP4
OP3'
SL
74A 74B 74C
74
CH'
76 75A'
G
OP4'
II
I

FIG. 19B

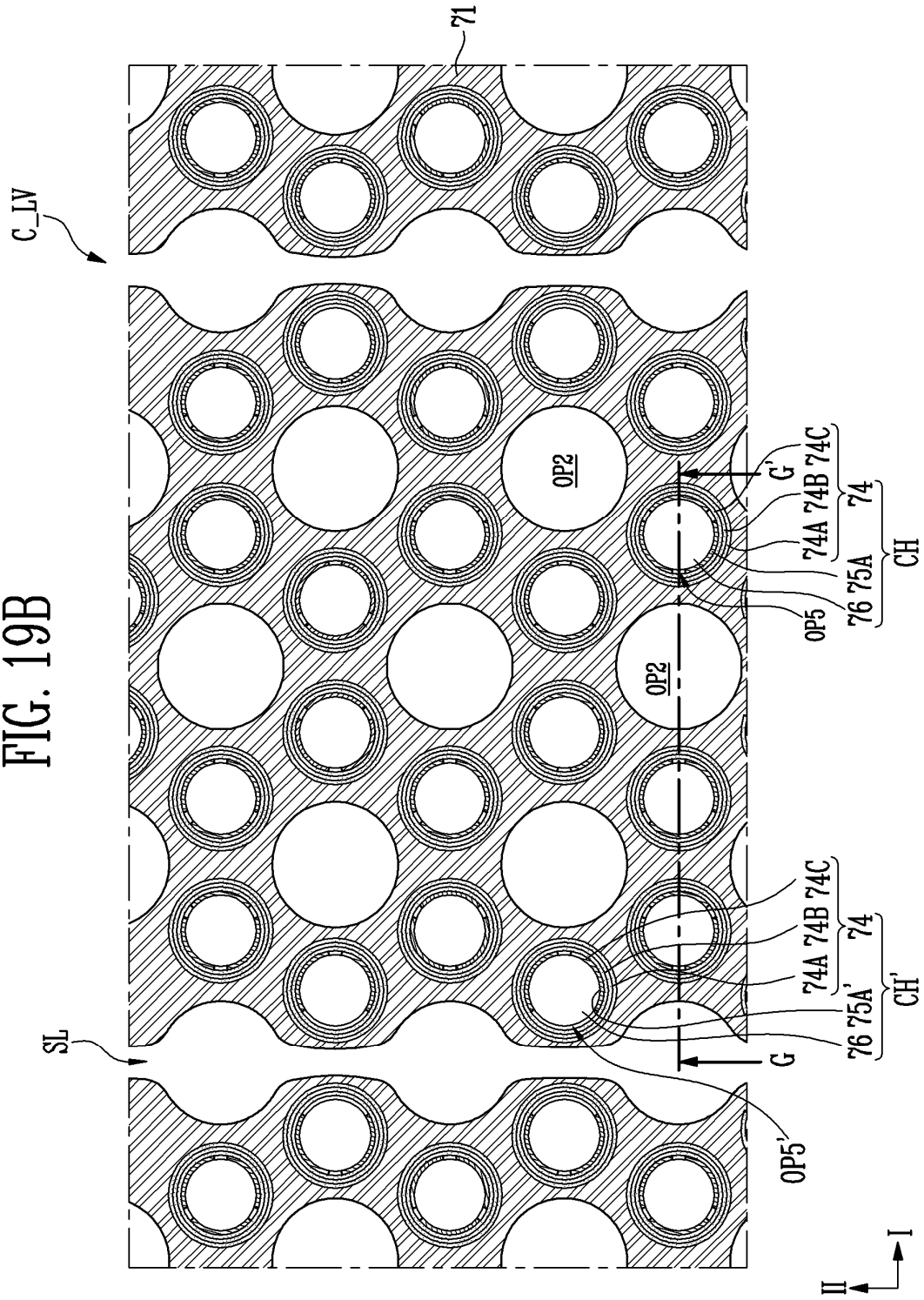

71
C_LV
OP2
OP2
G'
74C
74B
74A
74
CH
75A
76
OP5
SL
G
74C
74B
74A'
74
CH'
75A'
76
OP5'
II
I

FIG. 19C

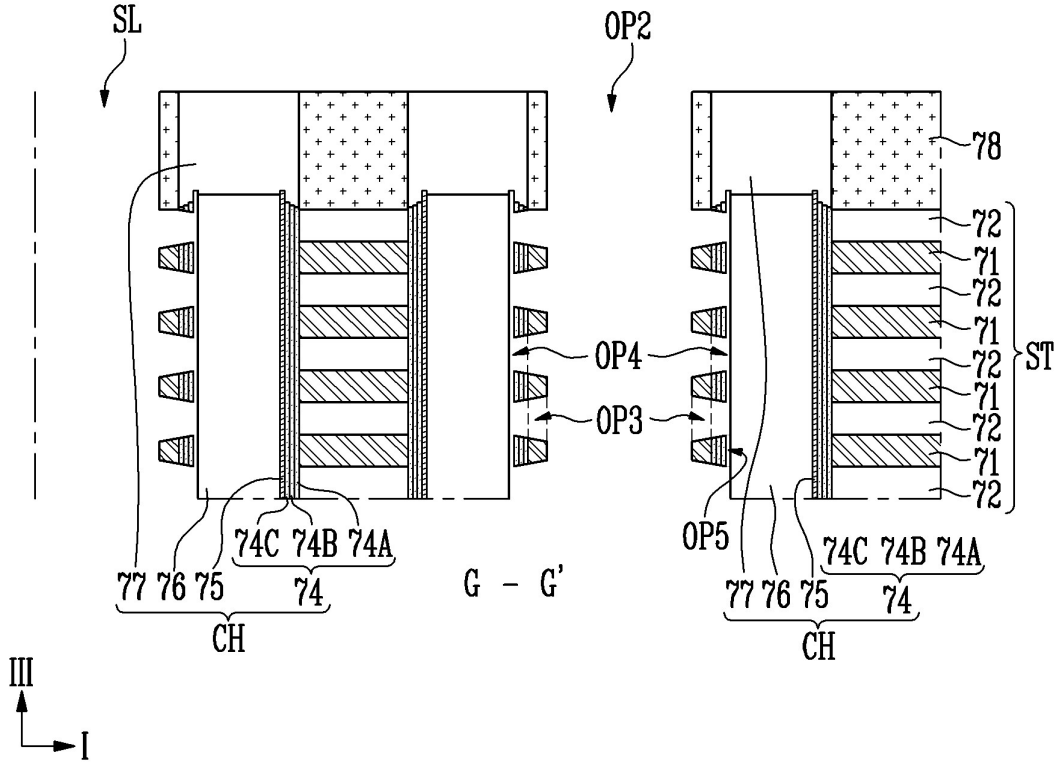

SL
OP2
78
72
71
72
71
72
71
72
71
72
ST
OP4
OP3
OP5
74C 74B 74A
74
77 76 75
CH
G - G'
III
I

FIG. 20A

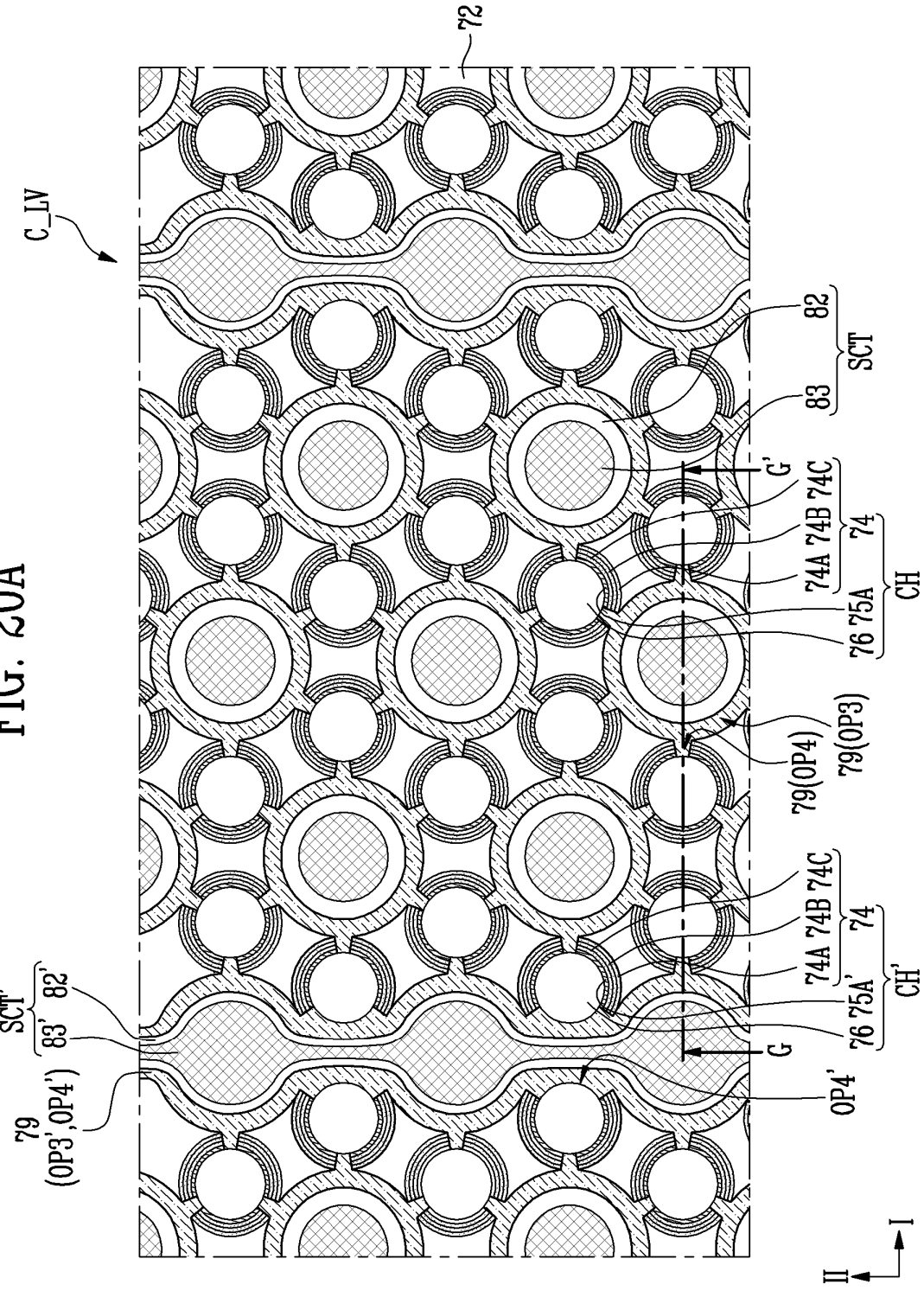

72
C_LV
82
83
SCT
G'
74A 74B 74C
74
76 75A
CH
79(OP4)
79(OP3)
74A 74B 74C
74
76 75A'
CH'
G
OP4'
SCT'
83' 82'
79
(OP3',OP4')
II
I

FIG. 20B

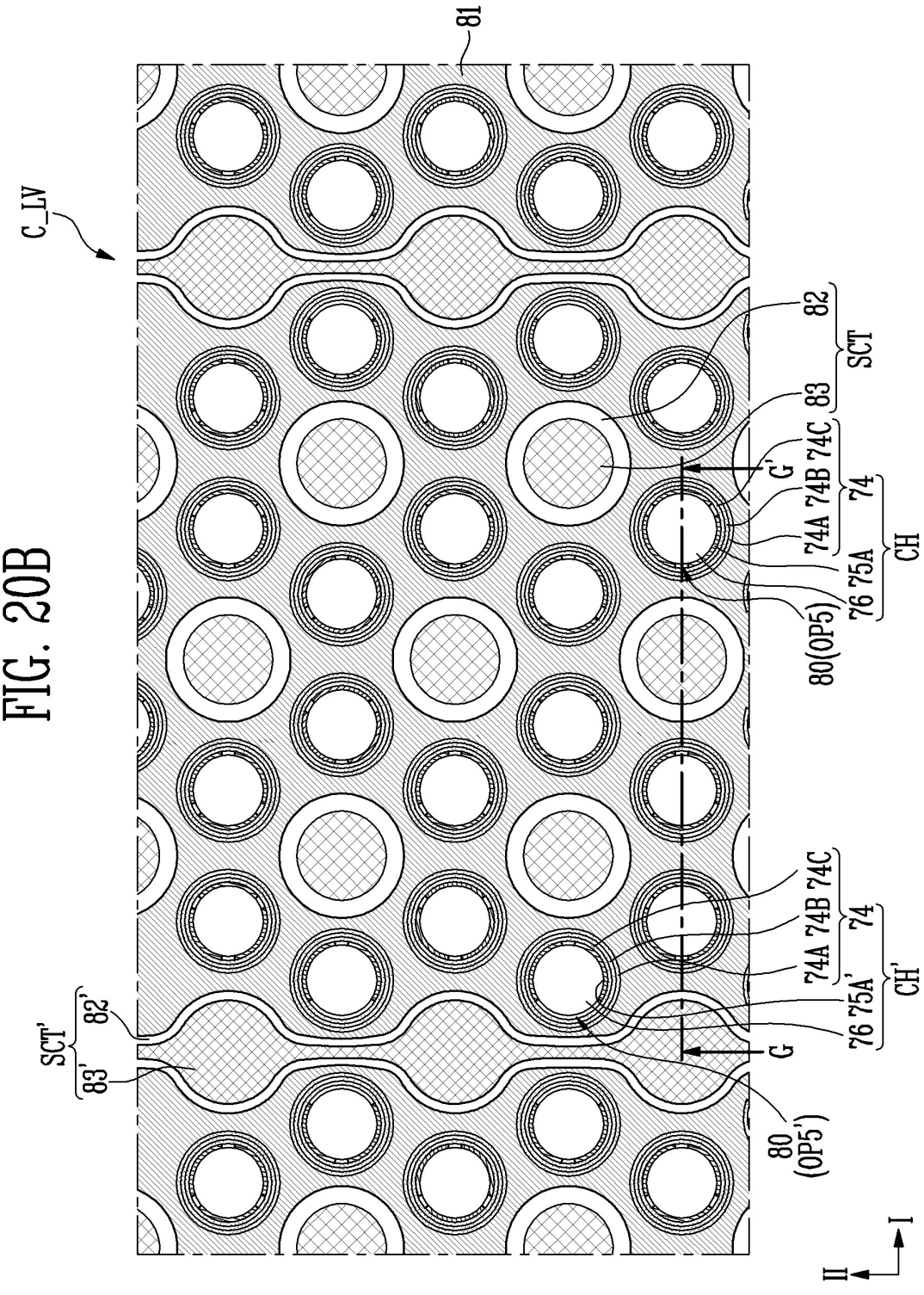

81
C_LV
82
SCT
83
G'
74C
74B
74A
74
80(OP5)
75A
76
CH
82'
SCT'
83'
G
74C
74B
74A
74
75A'
76
CH'
80
(OP5')
II
I

FIG. 20C

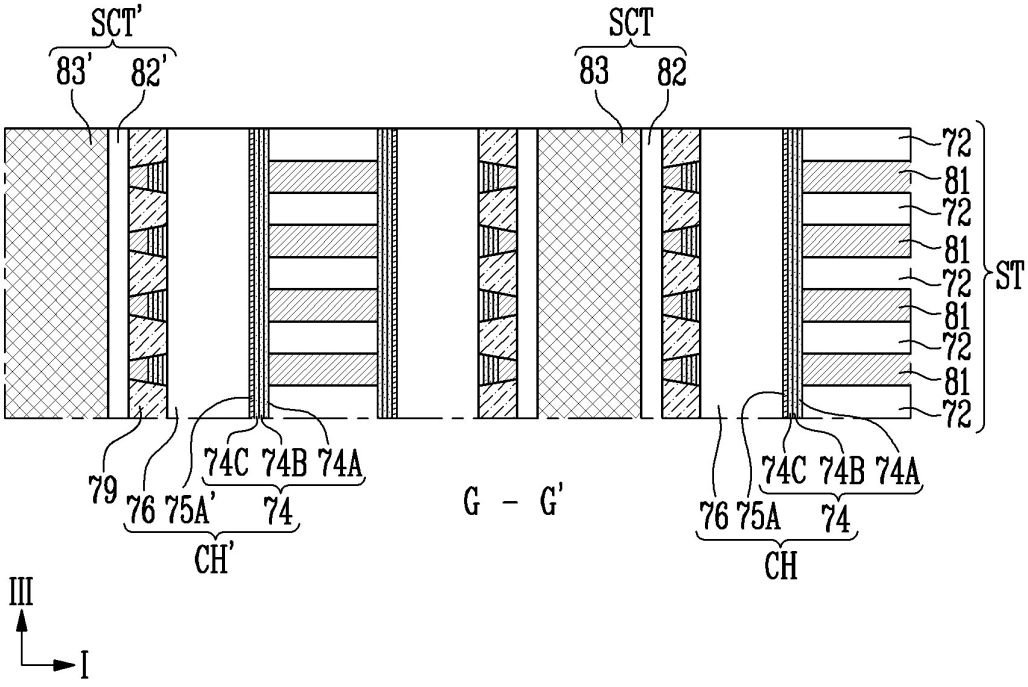

SCT'
83'
82'
SCT
83
82
72
81
72
81
72
81
72
81
72
ST
79
76
75A'
74C
74B
74A
74
CH'
G - G'
76
75A
74C
74B
74A
74
CH
III
I

FIG. 21A

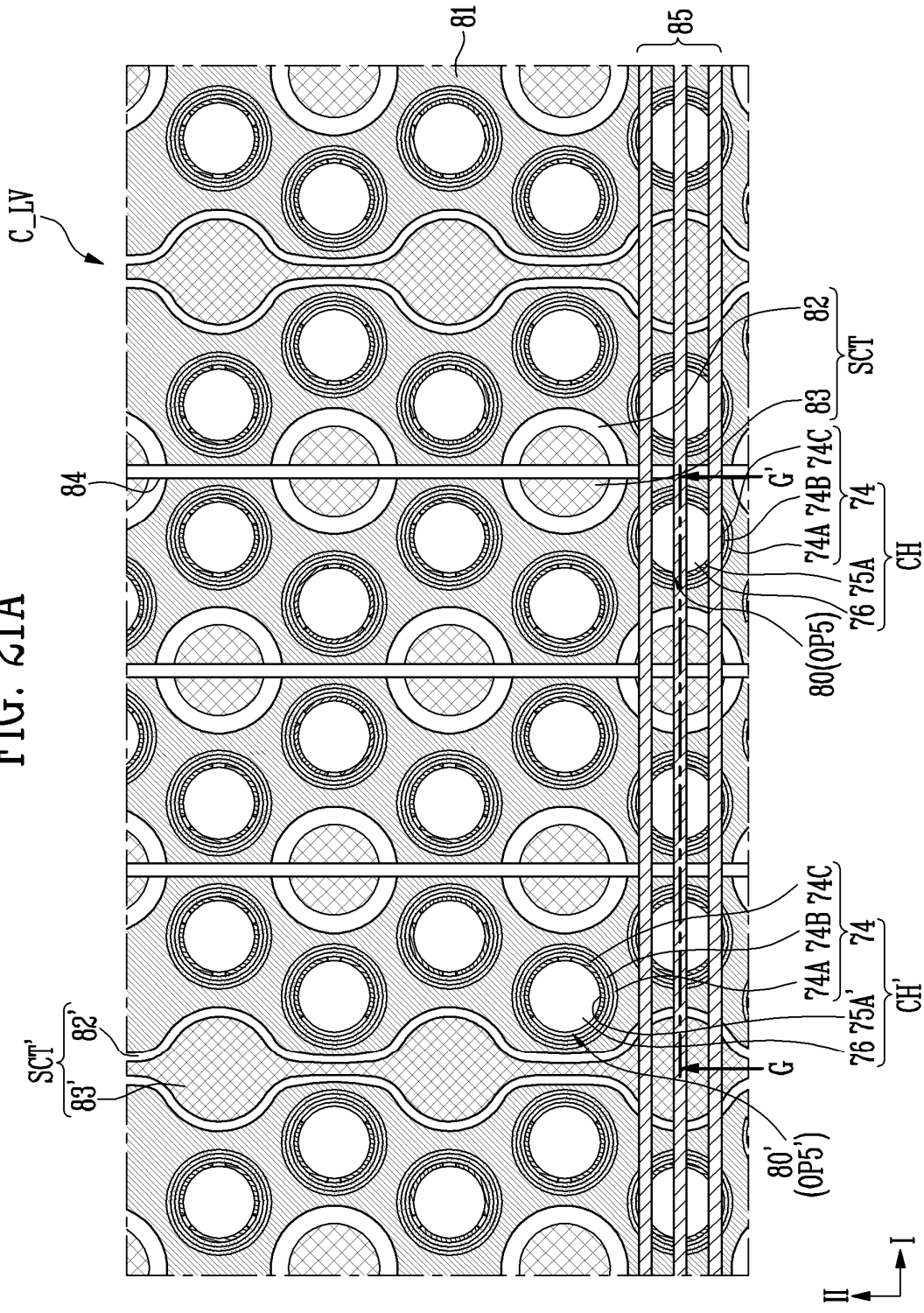

C_LV
81
85
84
82
SCT
83
74C
G'
74B
74
74A
CH
75A
76
80(OP5)
SCT'
82'
83'
74C
74B
74
74A
CH'
75A'
76
G
80'
(OP5')
II
I

FIG. 21B

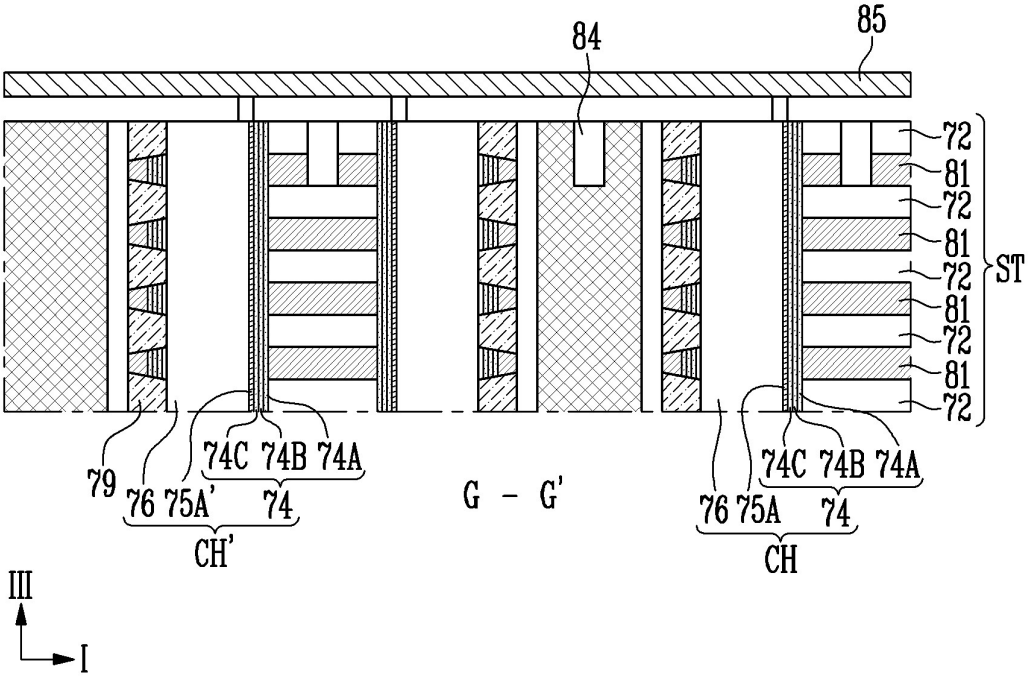


FIG. 22

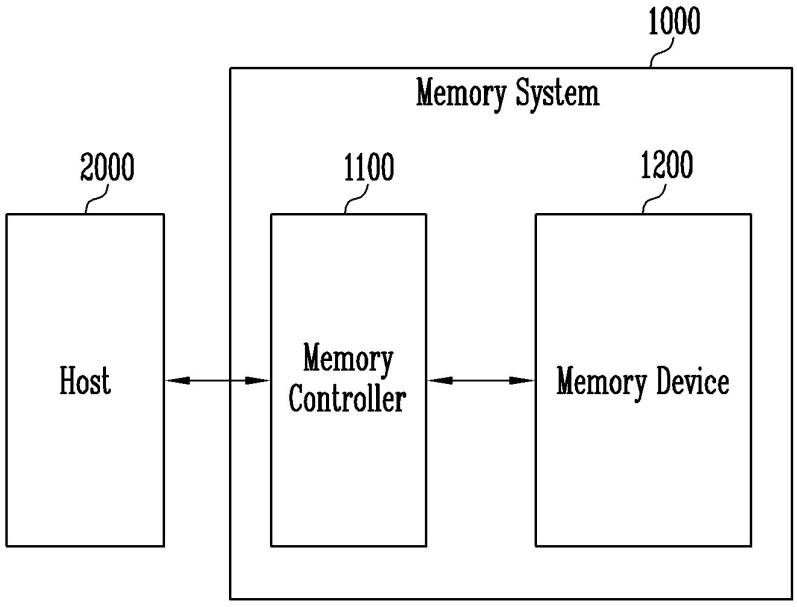


FIG. 23

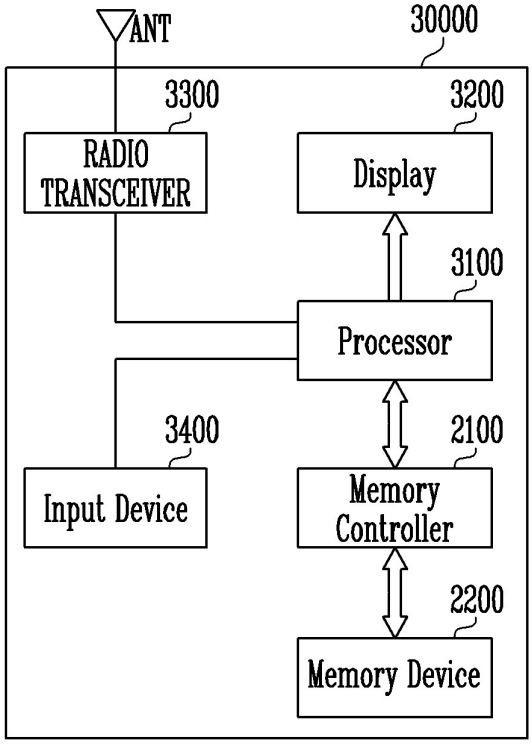

ANT
30000
3300
3200
RADIO TRANSCEIVER
Display
3100
Processor
3400
2100
Input Device
Memory Controller
2200
Memory Device

FIG. 24

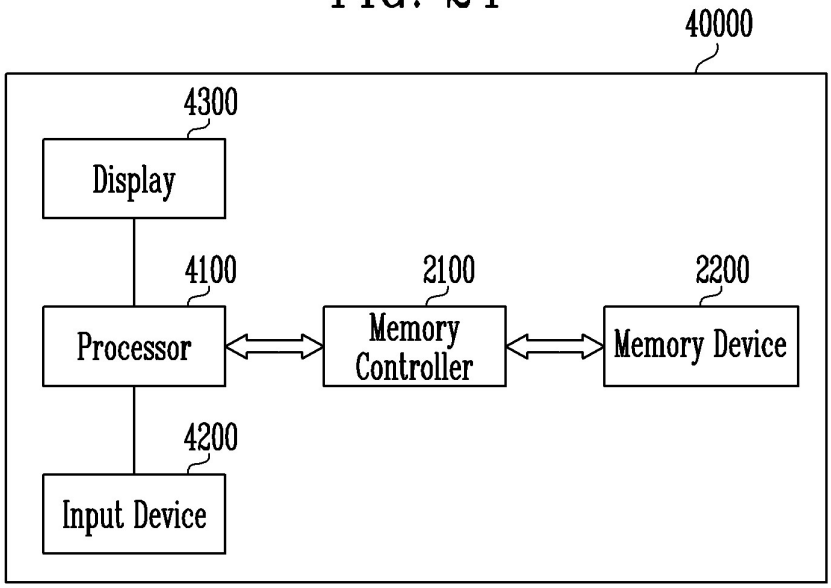

40000
4300
Display
4100
2100
2200
Processor
Memory Controller
Memory Device
4200
Input Device

FIG. 25

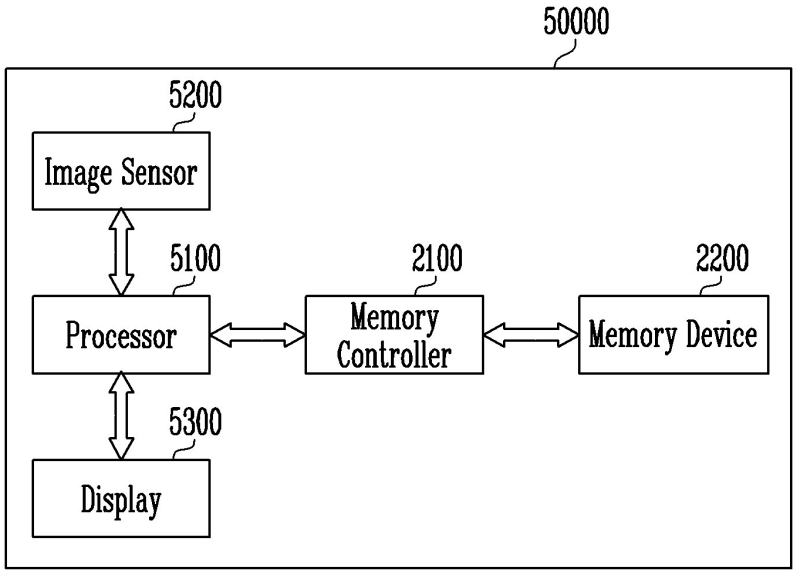
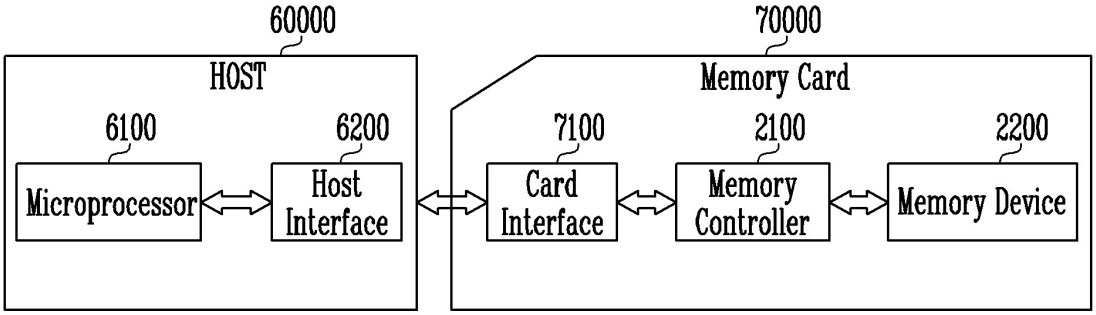

50000
5200
Image Sensor
5100
2100
2200
Processor
Memory Controller
Memory Device
5300
Display

FIG. 26


60000
HOST
6100
6200
Microprocessor
Host Interface
70000
Memory Card
7100
2100
2200
Card Interface
Memory Controller
Memory Device