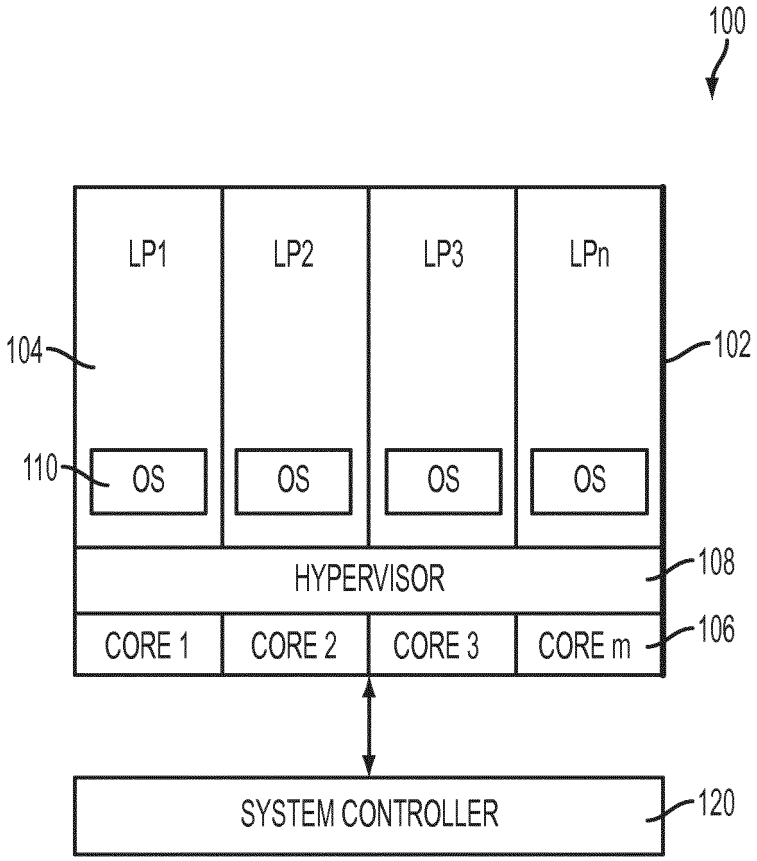
100
LP1
LP2
LP3
LPn
104
102
110
OS
OS
OS
OS
HYPERVISOR
108
CORE 1
CORE 2
CORE 3
CORE m
106
SYSTEM CONTROLLER
120

FIG. 1

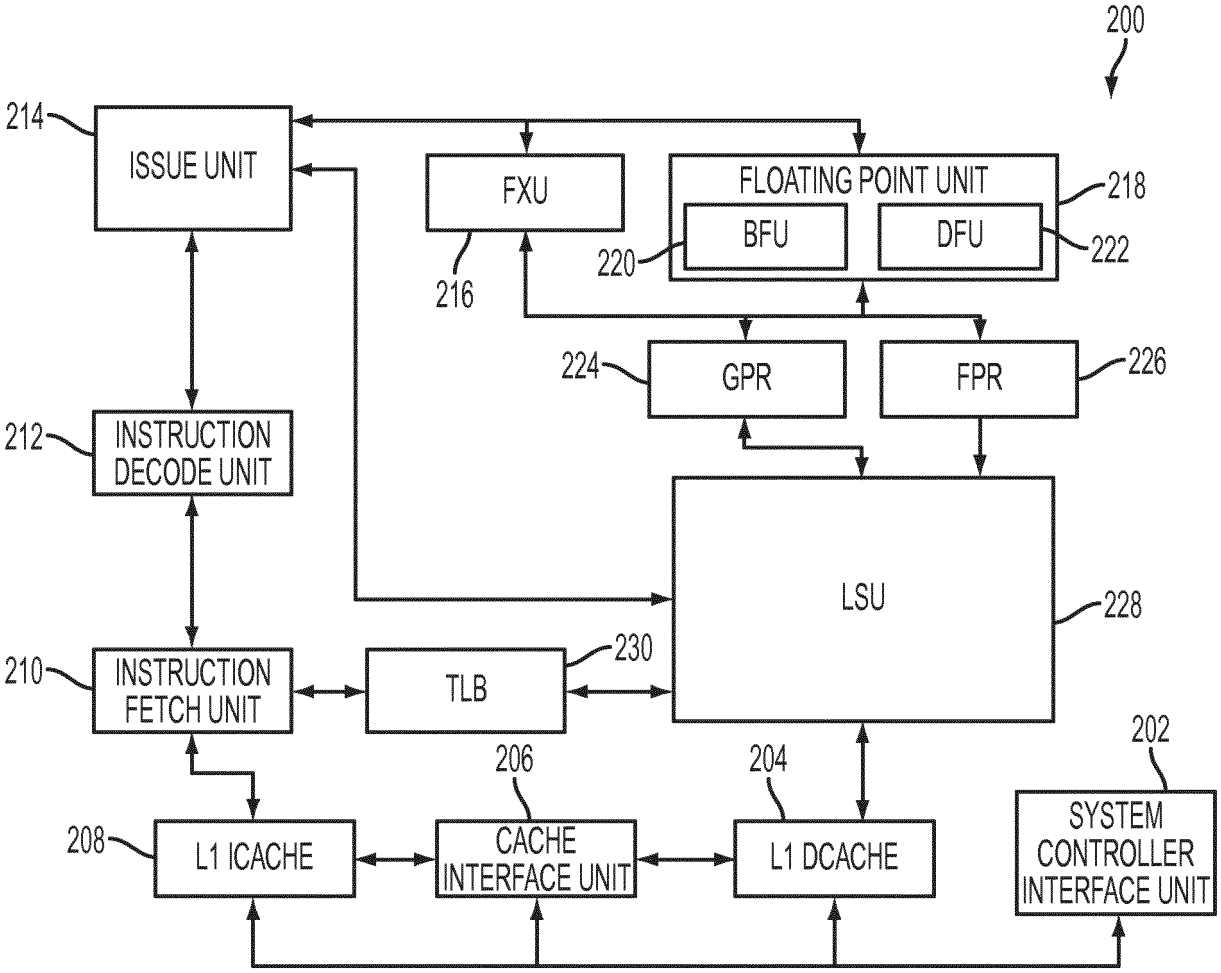
200
214
ISSUE UNIT
FXU
FLOATING POINT UNIT
218
BFU
DFU
220
222
216
224
GPR
FPR
226
212
INSTRUCTION DECODE UNIT
LSU
228
210
INSTRUCTION FETCH UNIT
TLB
230
202
206
204
208
L1 ICACHE
CACHE INTERFACE UNIT
L1 DCACHE
SYSTEM CONTROLLER INTERFACE UNIT

FIG. 2

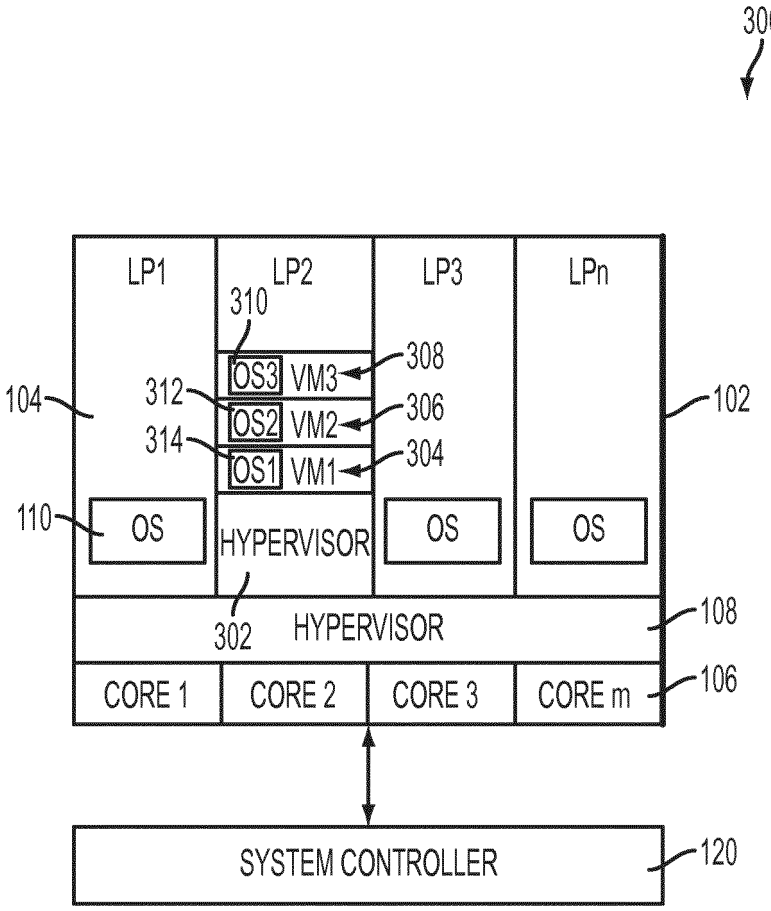
300
LP1
LP2
LP3
LPn
310
308
OS3
VM3
312
306
OS2
VM2
104
102
314
304
OS1
VM1
110
OS
HYPERVISOR
OS
OS
302
HYPERVISOR
108
CORE 1
CORE 2
CORE 3
CORE m
106
SYSTEM CONTROLLER
120

FIG. 3

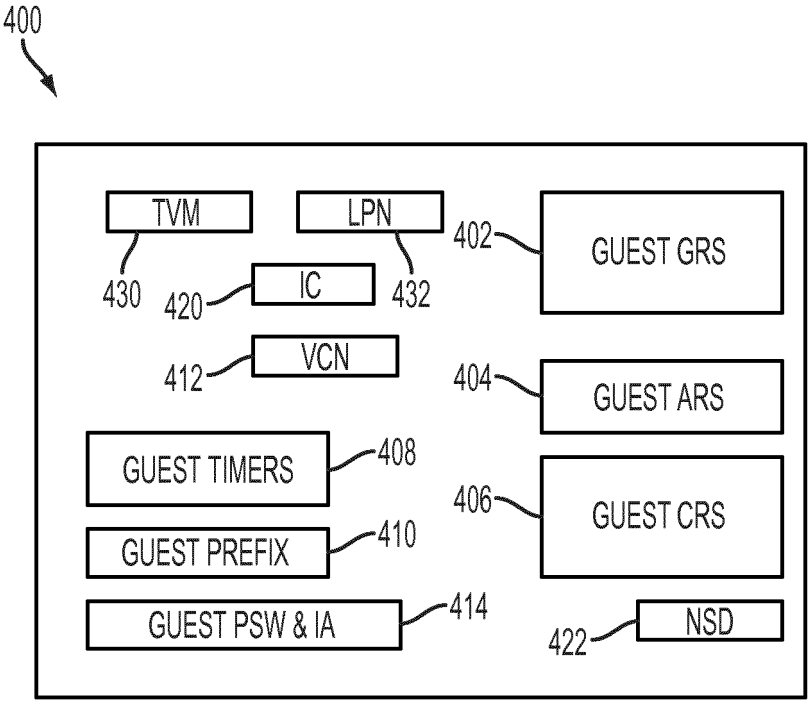
400
TVM
LPN
430
IC
420
432
402
GUEST GRS
412
VCN
404
GUEST ARS
GUEST TIMERS
408
406
GUEST CRS
GUEST PREFIX
410
GUEST PSW & IA
414
422
NSD

FIG. 4

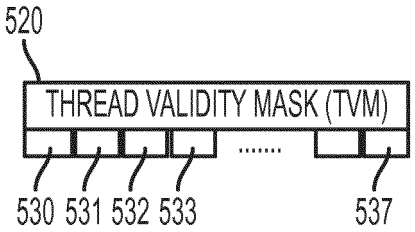

FIG. 5

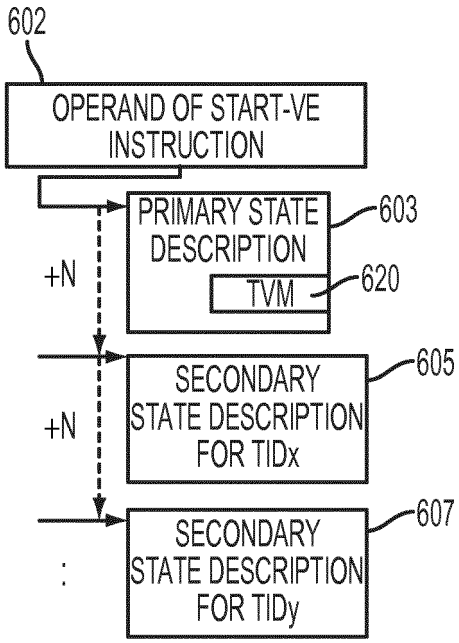
602
OPERAND OF START-VE INSTRUCTION
PRIMARY STATE DESCRIPTION
603
TVM
620
+N
SECONDARY STATE DESCRIPTION FOR TIDx
605
+N
SECONDARY STATE DESCRIPTION FOR TIDy
607
:

FIG. 6

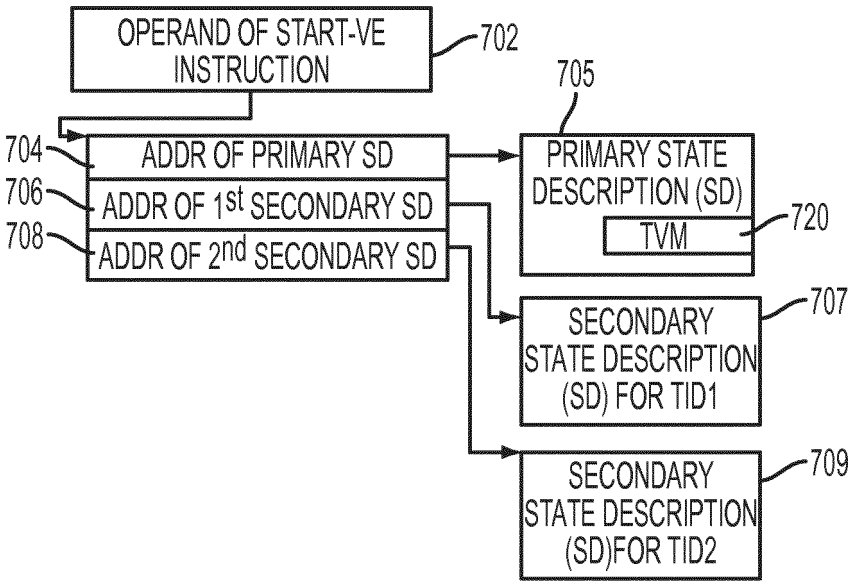
OPERAND OF START-VE INSTRUCTION
702
705
704
ADDR OF PRIMARY SD
706
ADDR OF 1st SECONDARY SD
708
ADDR OF 2nd SECONDARY SD
PRIMARY STATE DESCRIPTION (SD)
TVM
720
SECONDARY STATE DESCRIPTION (SD) FOR TID1
707
SECONDARY STATE DESCRIPTION (SD)FOR TID2
709

FIG. 7

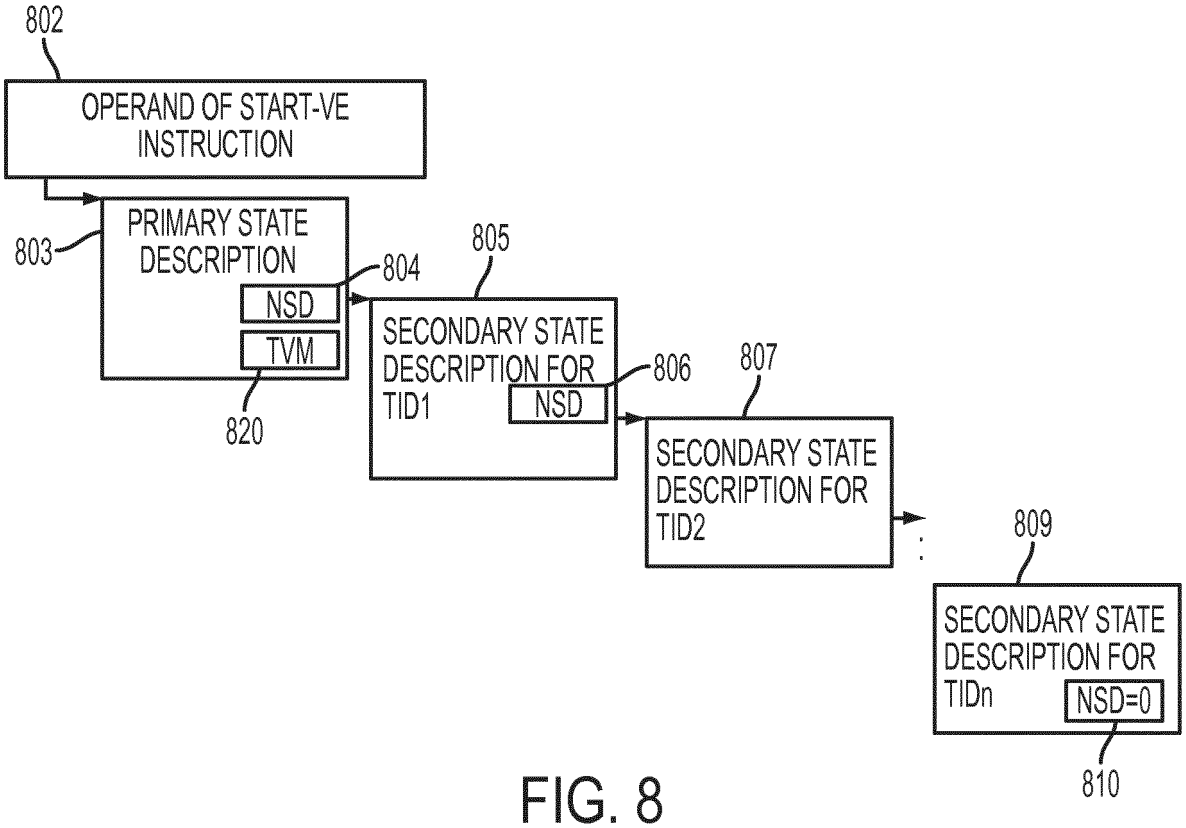
802
OPERAND OF START-VE INSTRUCTION
803
PRIMARY STATE DESCRIPTION
NSD
TVM
804
820
805
SECONDARY STATE DESCRIPTION FOR TID1
NSD
806
807
SECONDARY STATE DESCRIPTION FOR TID2
809
SECONDARY STATE DESCRIPTION FOR TIDn
NSD=0
810

FIG. 8

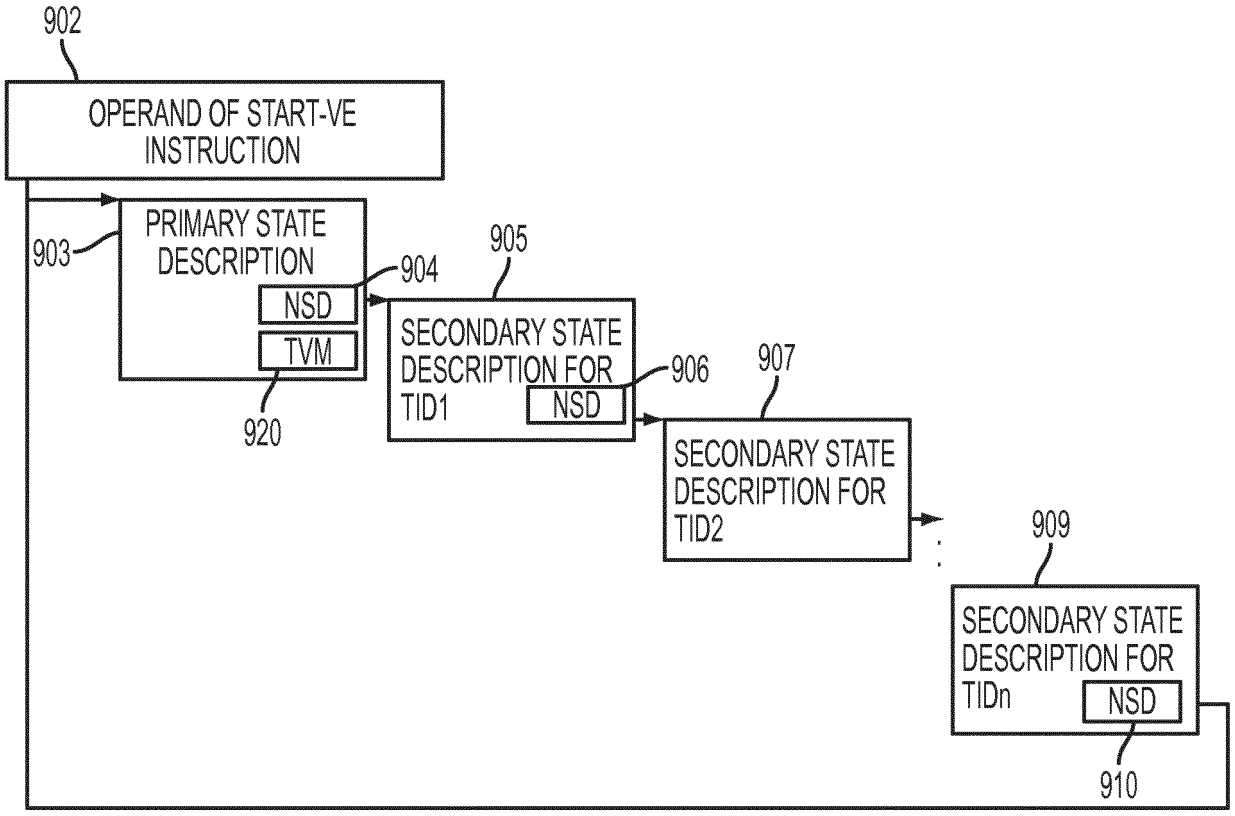
902
OPERAND OF START-VE INSTRUCTION
903
PRIMARY STATE DESCRIPTION
NSD
TVM
904
920
905
SECONDARY STATE DESCRIPTION FOR TID1
NSD
906
907
SECONDARY STATE DESCRIPTION FOR TID2
909
SECONDARY STATE DESCRIPTION FOR TIDn
NSD
910

FIG. 9

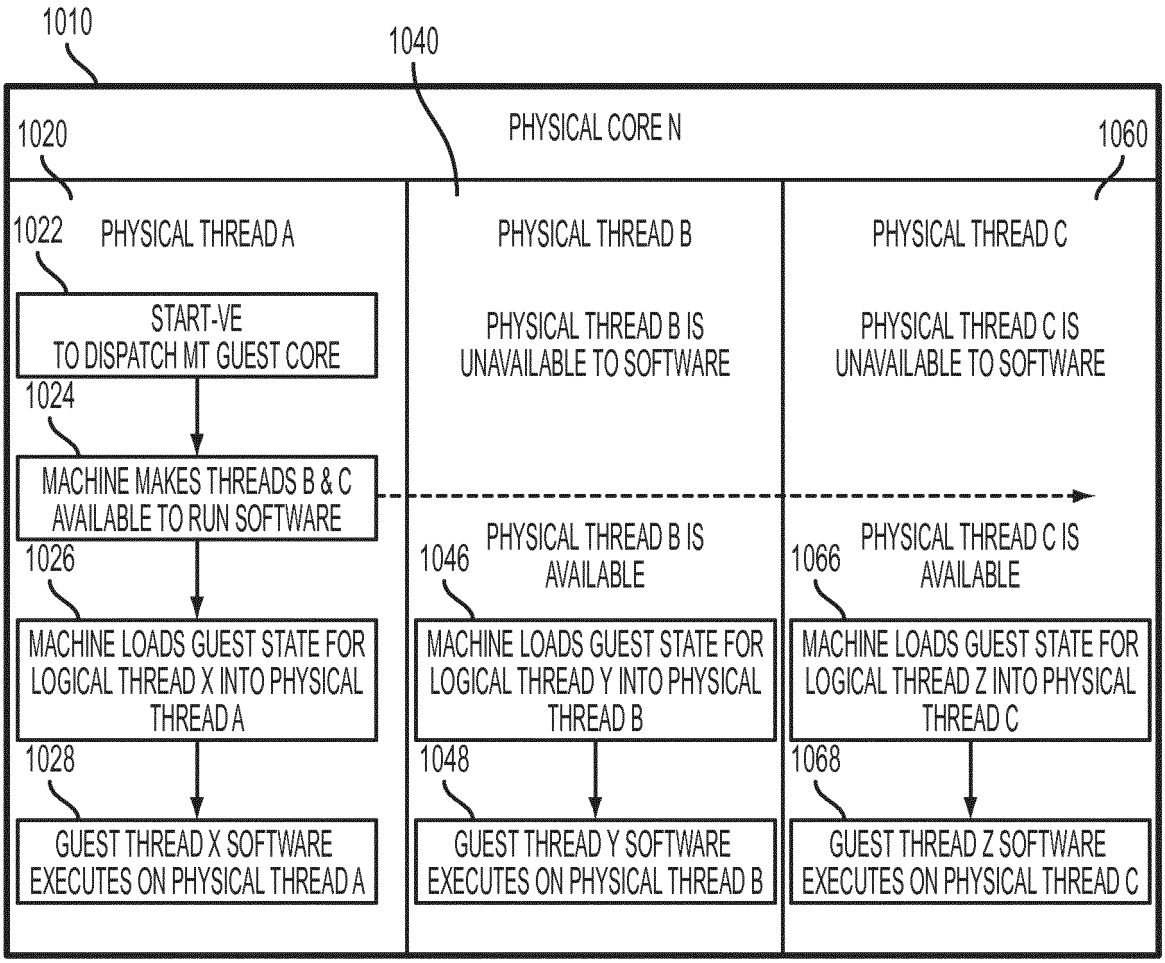
1010
1040
1020
PHYSICAL CORE N
1060
1022
PHYSICAL THREAD A
PHYSICAL THREAD B
PHYSICAL THREAD C
START-VE
TO DISPATCH MT GUEST CORE
PHYSICAL THREAD B IS
UNAVAILABLE TO SOFTWARE
PHYSICAL THREAD C IS
UNAVAILABLE TO SOFTWARE
1024
MACHINE MAKES THREADS B & C
AVAILABLE TO RUN SOFTWARE
1026
1046
PHYSICAL THREAD B IS
AVAILABLE
1066
PHYSICAL THREAD C IS
AVAILABLE
MACHINE LOADS GUEST STATE FOR
LOGICAL THREAD X INTO PHYSICAL
THREAD A
MACHINE LOADS GUEST STATE FOR
LOGICAL THREAD Y INTO PHYSICAL
THREAD B
MACHINE LOADS GUEST STATE FOR
LOGICAL THREAD Z INTO PHYSICAL
THREAD C
1028
1048
1068
GUEST THREAD X SOFTWARE
EXECUTES ON PHYSICAL THREAD A
GUEST THREAD Y SOFTWARE
EXECUTES ON PHYSICAL THREAD B
GUEST THREAD Z SOFTWARE
EXECUTES ON PHYSICAL THREAD C

FIG. 10

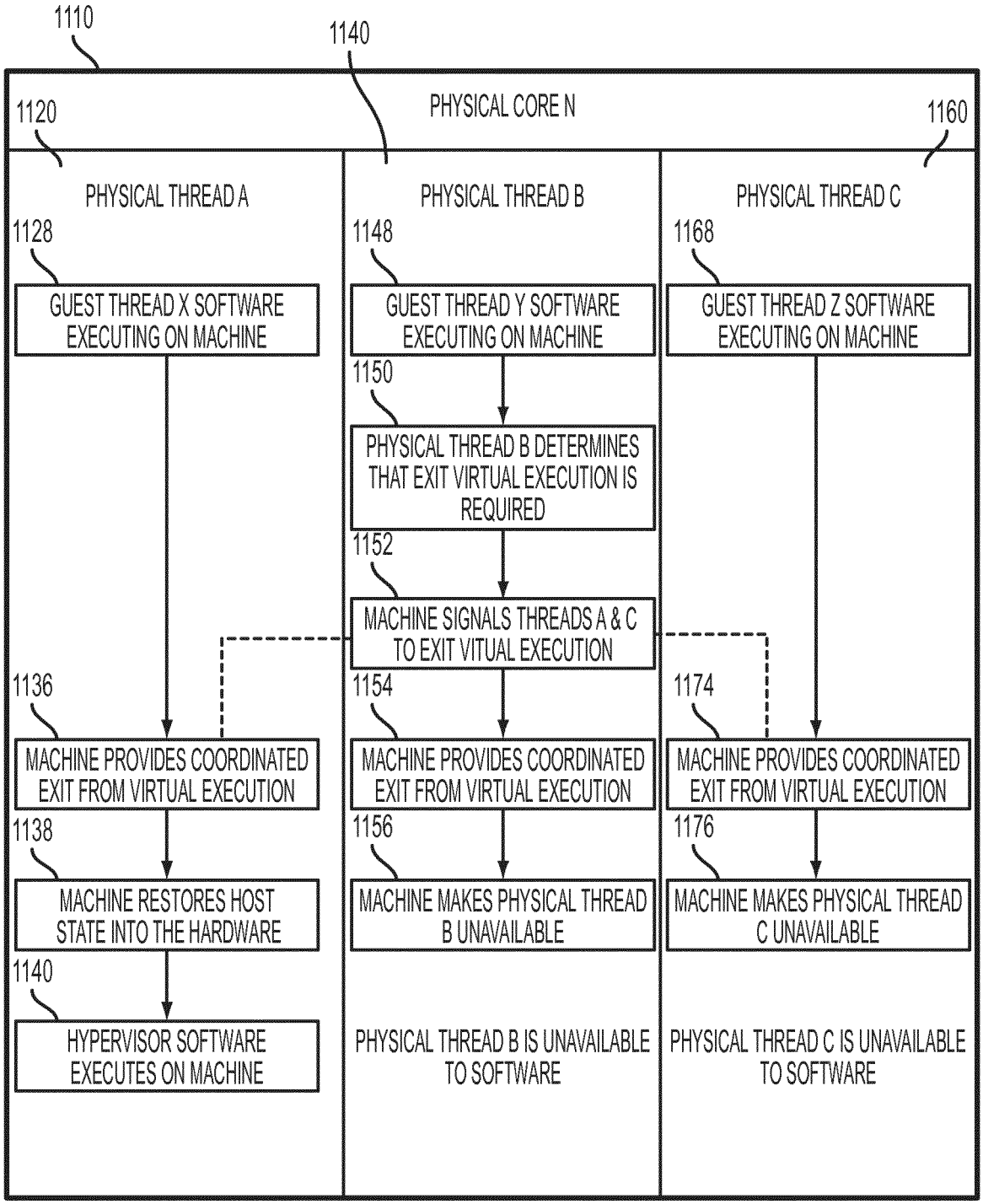
1110
1140
1120
PHYSICAL CORE N
1160
PHYSICAL THREAD A
PHYSICAL THREAD B
PHYSICAL THREAD C
1128
1148
1168
GUEST THREAD X SOFTWARE EXECUTING ON MACHINE
GUEST THREAD Y SOFTWARE EXECUTING ON MACHINE
GUEST THREAD Z SOFTWARE EXECUTING ON MACHINE
1150
PHYSICAL THREAD B DETERMINES THAT EXIT VIRTUAL EXECUTION IS REQUIRED
1152
MACHINE SIGNALS THREADS A & C TO EXIT VITUAL EXECUTION
1136
1154
1174
MACHINE PROVIDES COORDINATED EXIT FROM VIRTUAL EXECUTION
MACHINE PROVIDES COORDINATED EXIT FROM VIRTUAL EXECUTION
MACHINE PROVIDES COORDINATED EXIT FROM VIRTUAL EXECUTION
1138
1156
1176
MACHINE RESTORES HOST STATE INTO THE HARDWARE
MACHINE MAKES PHYSICAL THREAD B UNAVAILABLE
MACHINE MAKES PHYSICAL THREAD C UNAVAILABLE
1140
HYPERVISOR SOFTWARE EXECUTES ON MACHINE
PHYSICAL THREAD B IS UNAVAILABLE TO SOFTWARE
PHYSICAL THREAD C IS UNAVAILABLE TO SOFTWARE

FIG. 11

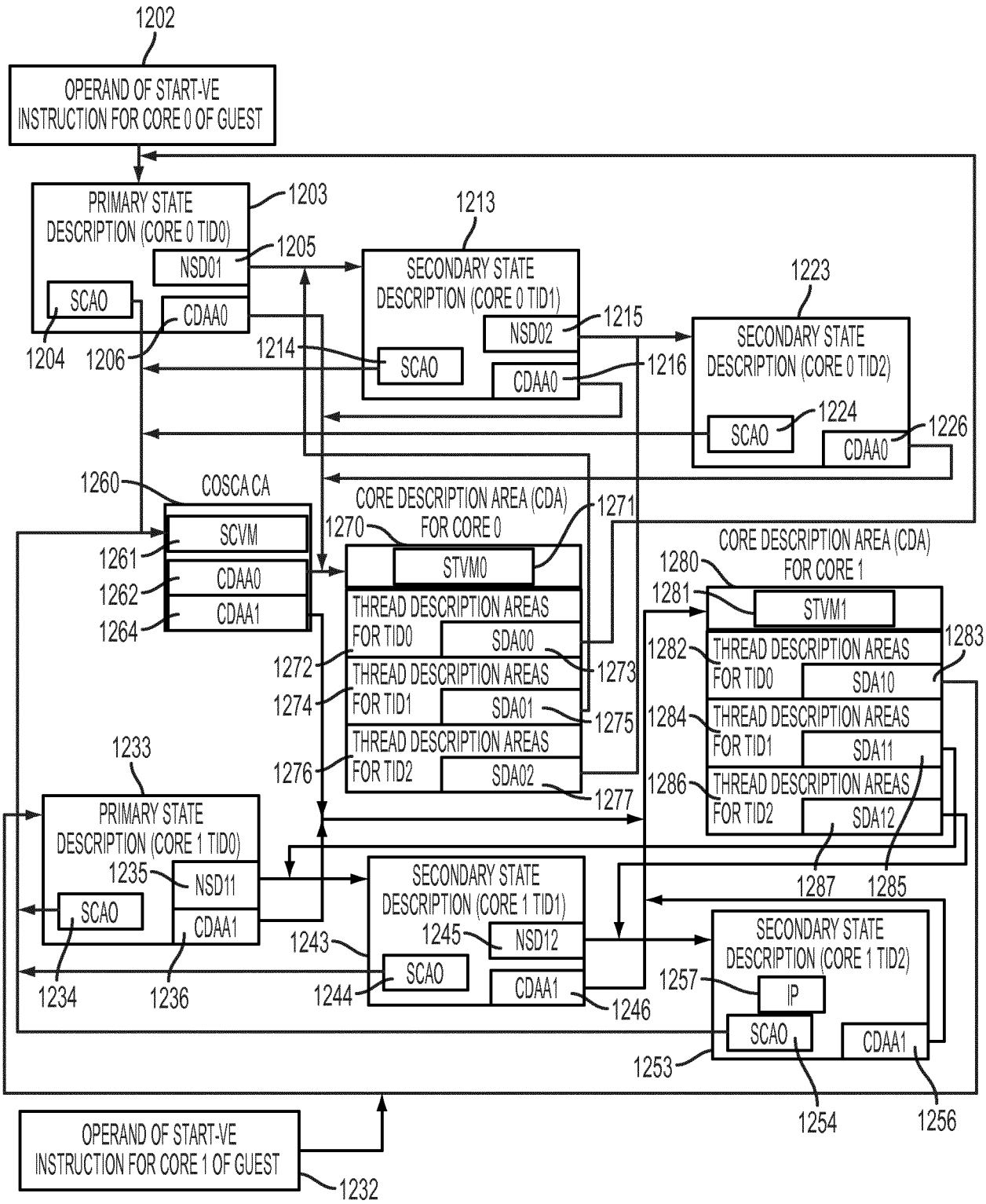
1202
OPERAND OF START-VE INSTRUCTION FOR CORE 0 OF GUEST
PRIMARY STATE DESCRIPTION (CORE 0 TID0)
1203
NSD01
1205
SCAO
CDAA0
1204
1206
1213
SECONDARY STATE DESCRIPTION (CORE 0 TID1)
NSD02
1215
1214
SCAO
CDAA0
1216
1223
SECONDARY STATE DESCRIPTION (CORE 0 TID2)
SCAO
1224
CDAA0
1226
1260
COSCA CA
SCVM
1261
CDAA0
1262
CDAA1
1264
CORE DESCRIPTION AREA (CDA) FOR CORE 0
1270
1271
STVM0
THREAD DESCRIPTION AREAS FOR TID0
SDA00
1272
1273
THREAD DESCRIPTION AREAS FOR TID1
SDA01
1274
1275
THREAD DESCRIPTION AREAS FOR TID2
SDA02
1276
1277
CORE DESCRIPTION AREA (CDA) FOR CORE 1
1280
1281
STVM1
1282
THREAD DESCRIPTION AREAS FOR TID0
SDA10
1283
1284
THREAD DESCRIPTION AREAS FOR TID1
SDA11
1286
THREAD DESCRIPTION AREAS FOR TID2
SDA12
1287
1285
1233
PRIMARY STATE DESCRIPTION (CORE 1 TID0)
1235
NSD11
SCAO
CDAA1
1234
1236
SECONDARY STATE DESCRIPTION (CORE 1 TID1)
1243
1245
NSD12
SCAO
CDAA1
1244
1246
SECONDARY STATE DESCRIPTION (CORE 1 TID2)
1257
IP
SCAO
CDAA1
1253
1254
1256
OPERAND OF START-VE INSTRUCTION FOR CORE 1 OF GUEST
1232

FIG. 12

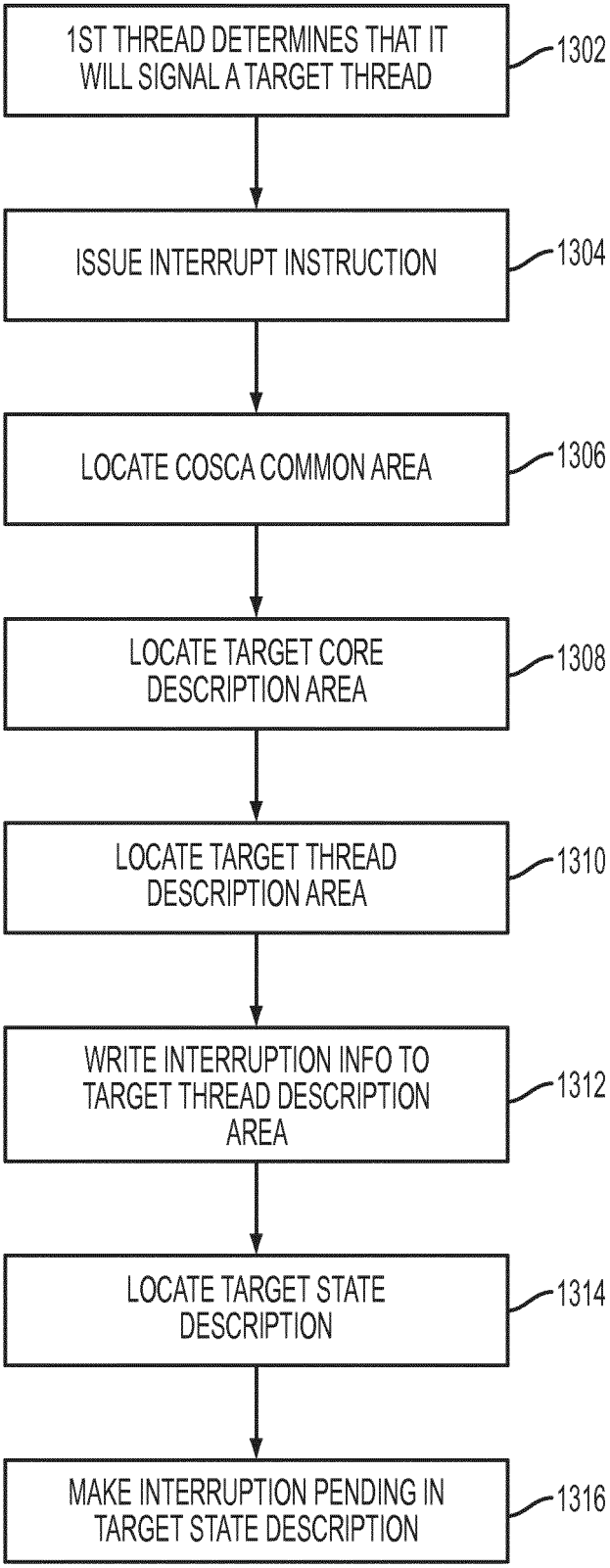
1ST THREAD DETERMINES THAT IT WILL SIGNAL A TARGET THREAD
1302
ISSUE INTERRUPT INSTRUCTION
1304
LOCATE COSCA COMMON AREA
1306
LOCATE TARGET CORE DESCRIPTION AREA
1308
LOCATE TARGET THREAD DESCRIPTION AREA
1310
WRITE INTERRUPTION INFO TO TARGET THREAD DESCRIPTION AREA
1312
LOCATE TARGET STATE DESCRIPTION
1314
MAKE INTERRUPTION PENDING IN TARGET STATE DESCRIPTION
1316

FIG. 13

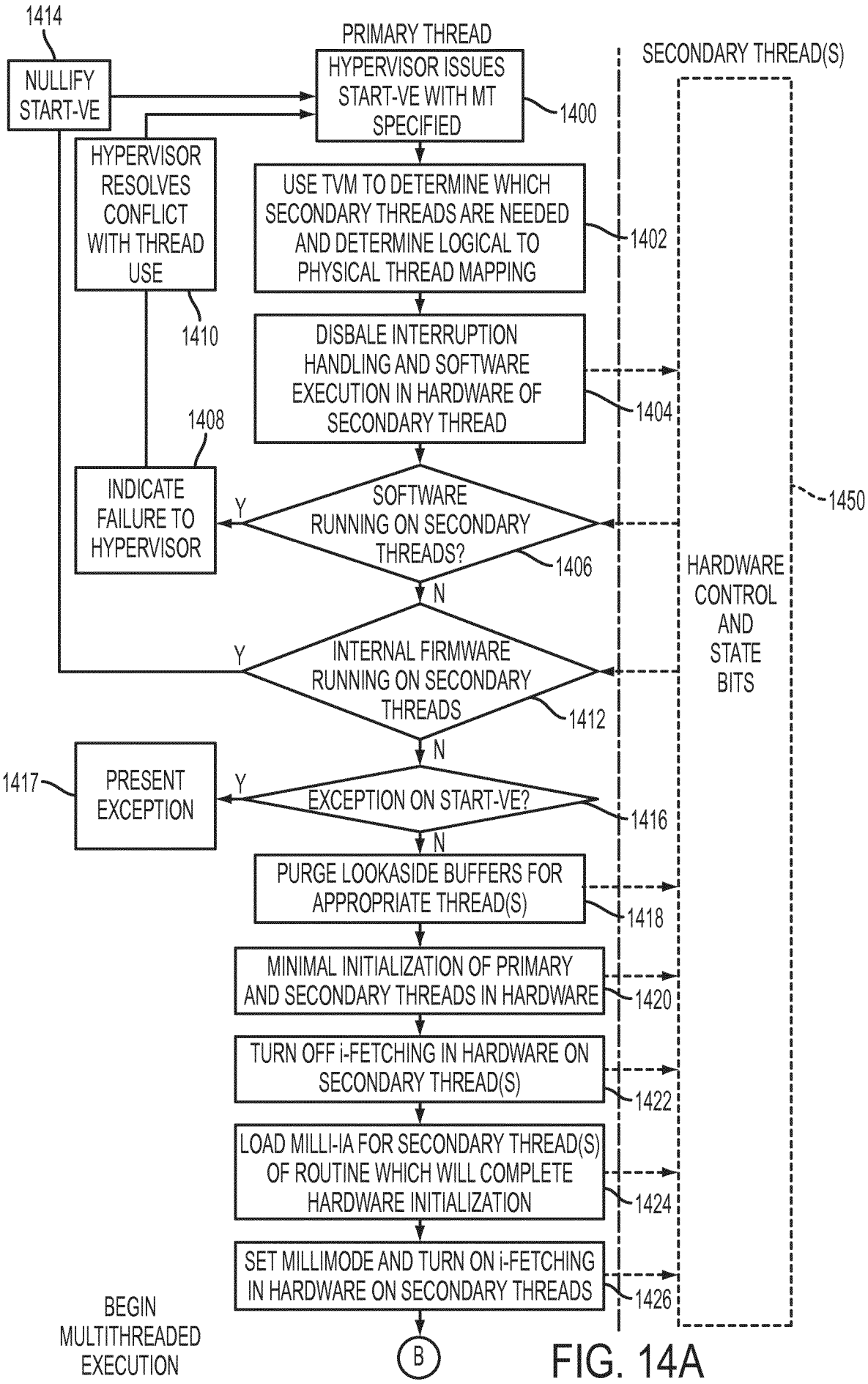
1414
NULLIFY START-VE
PRIMARY THREAD
SECONDARY THREAD(S)
HYPERVISOR ISSUES START-VE WITH MT SPECIFIED
1400
HYPERVISOR RESOLVES CONFLICT WITH THREAD USE
1410
USE TVM TO DETERMINE WHICH SECONDARY THREADS ARE NEEDED AND DETERMINE LOGICAL TO PHYSICAL THREAD MAPPING
1402
DISBALE INTERRUPTION HANDLING AND SOFTWARE EXECUTION IN HARDWARE OF SECONDARY THREAD
1404
1408
INDICATE FAILURE TO HYPERVISOR
Y
SOFTWARE RUNNING ON SECONDARY THREADS?
1406
N
1450
HARDWARE CONTROL AND STATE BITS
Y
INTERNAL FIRMWARE RUNNING ON SECONDARY THREADS
1412
N
1417
PRESENT EXCEPTION
Y
EXCEPTION ON START-VE?
1416
N
PURGE LOOKASIDE BUFFERS FOR APPROPRIATE THREAD(S)
1418
MINIMAL INITIALIZATION OF PRIMARY AND SECONDARY THREADS IN HARDWARE
1420
TURN OFF i-FETCHING IN HARDWARE ON SECONDARY THREAD(S)
1422
LOAD MILLI-IA FOR SECONDARY THREAD(S) OF ROUTINE WHICH WILL COMPLETE HARDWARE INITIALIZATION
1424
SET MILLIMODE AND TURN ON i-FETCHING IN HARDWARE ON SECONDARY THREADS
1426
BEGIN MULTITHREADED EXECUTION
B

FIG. 14A

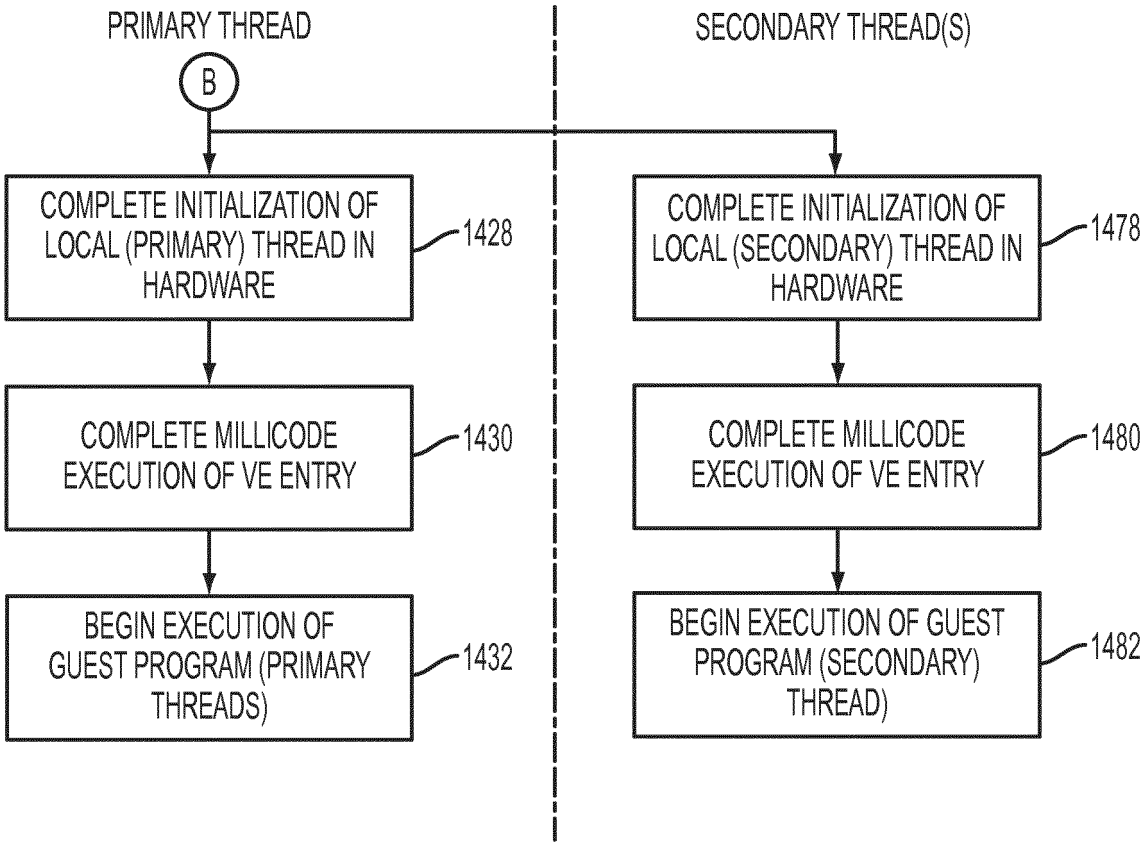
PRIMARY THREAD
SECONDARY THREAD(S)
B
COMPLETE INITIALIZATION OF LOCAL (PRIMARY) THREAD IN HARDWARE
1428
COMPLETE MILLICODE EXECUTION OF VE ENTRY
1430
BEGIN EXECUTION OF GUEST PROGRAM (PRIMARY THREADS)
1432
COMPLETE INITIALIZATION OF LOCAL (SECONDARY) THREAD IN HARDWARE
1478
COMPLETE MILLICODE EXECUTION OF VE ENTRY
1480
BEGIN EXECUTION OF GUEST PROGRAM (SECONDARY) THREAD)
1482

FIG. 14B

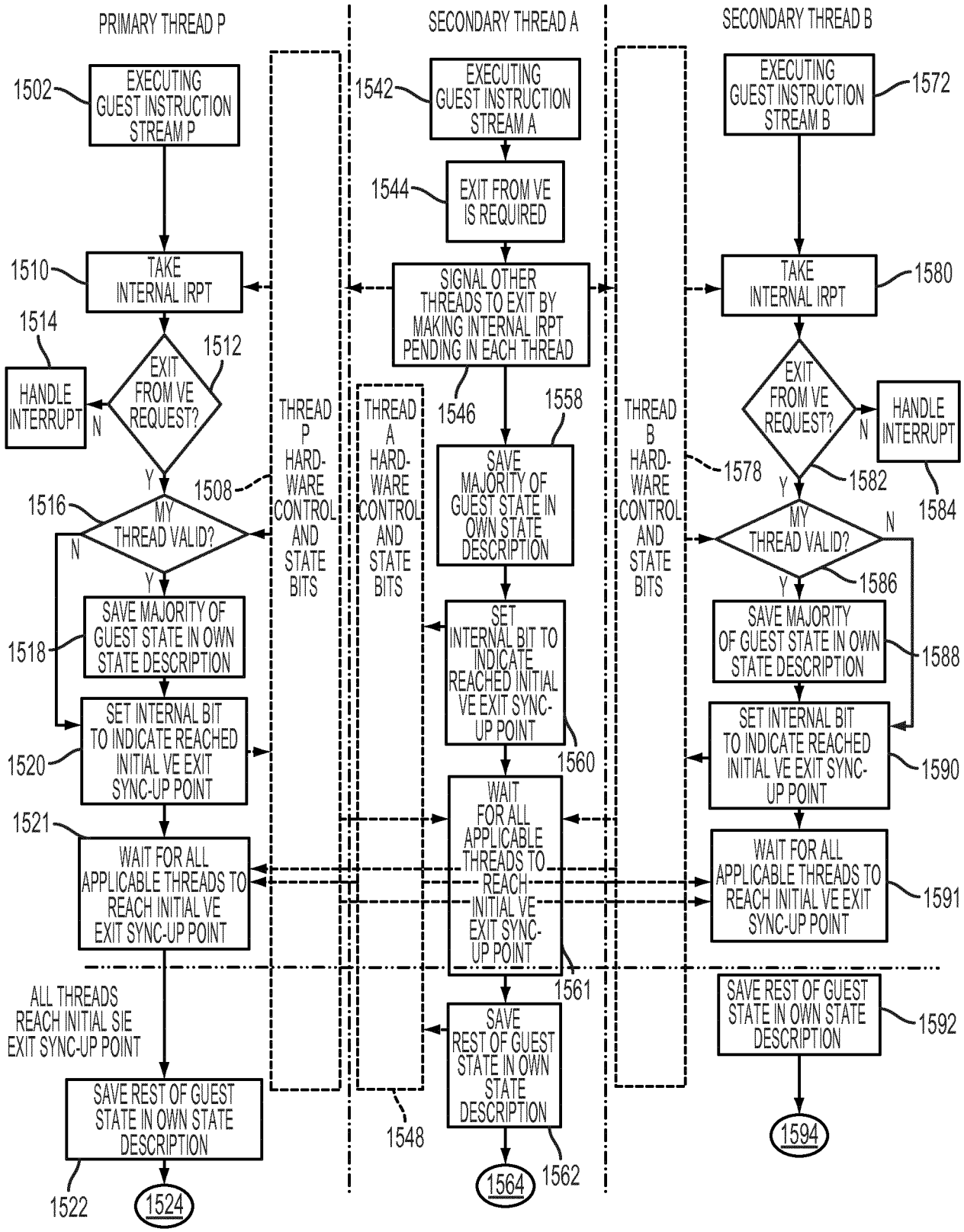
PRIMARY THREAD P
SECONDARY THREAD A
SECONDARY THREAD B
1502
EXECUTING GUEST INSTRUCTION STREAM P
1542
EXECUTING GUEST INSTRUCTION STREAM A
1572
EXECUTING GUEST INSTRUCTION STREAM B
1544
EXIT FROM VE IS REQUIRED
1510
TAKE INTERNAL IRPT
SIGNAL OTHER THREADS TO EXIT BY MAKING INTERNAL IRPT PENDING IN EACH THREAD
1546
1580
TAKE INTERNAL IRPT
1514
1512
HANDLE INTERRUPT
EXIT FROM VE REQUEST?
N
Y
1558
SAVE MAJORITY OF GUEST STATE IN OWN STATE DESCRIPTION
1578
1582
1584
HANDLE INTERRUPT
1508
THREAD P HARD-WARE CONTROL AND STATE BITS
THREAD A HARD-WARE CONTROL AND STATE BITS
THREAD B HARD-WARE CONTROL AND STATE BITS
1516
MY THREAD VALID?
1586
1518
SAVE MAJORITY OF GUEST STATE IN OWN STATE DESCRIPTION
SET INTERNAL BIT TO INDICATE REACHED INITIAL VE EXIT SYNC-UP POINT
1560
1588
1520
SET INTERNAL BIT TO INDICATE REACHED INITIAL VE EXIT SYNC-UP POINT
1590
1521
WAIT FOR ALL APPLICABLE THREADS TO REACH INITIAL VE EXIT SYNC-UP POINT
1591
1561
ALL THREADS REACH INITIAL SIE EXIT SYNC-UP POINT
SAVE REST OF GUEST STATE IN OWN STATE DESCRIPTION
1592
1548
1522
1524
1562
1564
1594

FIG. 15A

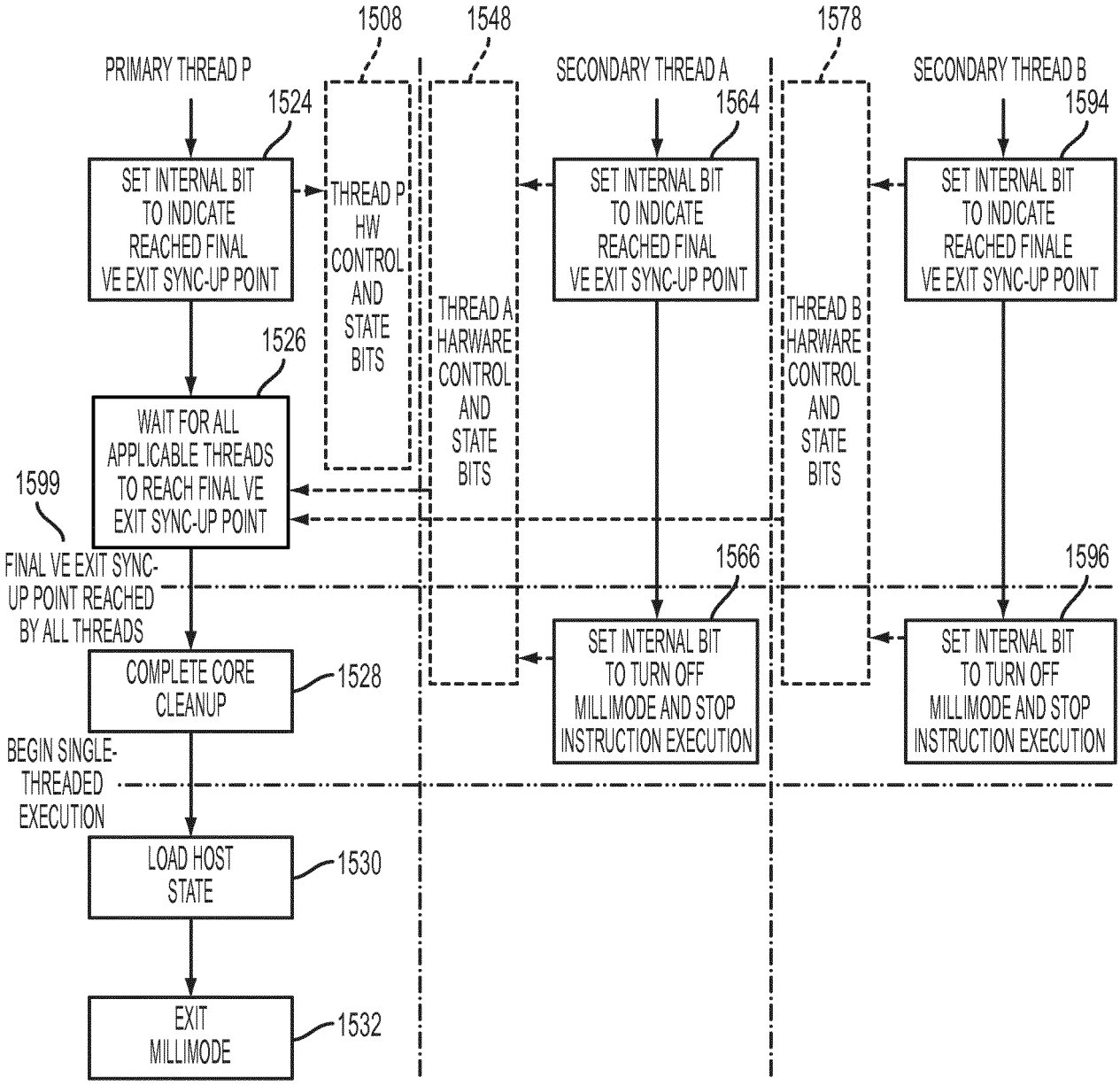
1508
1548
1578
PRIMARY THREAD P
SECONDARY THREAD A
SECONDARY THREAD B
1524
1564
1594
SET INTERNAL BIT TO INDICATE REACHED FINAL VE EXIT SYNC-UP POINT
THREAD P HW CONTROL AND STATE BITS
THREAD A HARWARE CONTROL AND STATE BITS
SET INTERNAL BIT TO INDICATE REACHED FINAL VE EXIT SYNC-UP POINT
THREAD B HARWARE CONTROL AND STATE BITS
SET INTERNAL BIT TO INDICATE REACHED FINALE VE EXIT SYNC-UP POINT
1526
WAIT FOR ALL APPLICABLE THREADS TO REACH FINAL VE EXIT SYNC-UP POINT
1599
FINAL VE EXIT SYNC-UP POINT REACHED BY ALL THREADS
1566
1596
SET INTERNAL BIT TO TURN OFF MILLIMODE AND STOP INSTRUCTION EXECUTION
SET INTERNAL BIT TO TURN OFF MILLIMODE AND STOP INSTRUCTION EXECUTION
COMPLETE CORE CLEANUP
1528
BEGIN SINGLE-THREADED EXECUTION
LOAD HOST STATE
1530
EXIT MILLIMODE
1532

FIG. 15B

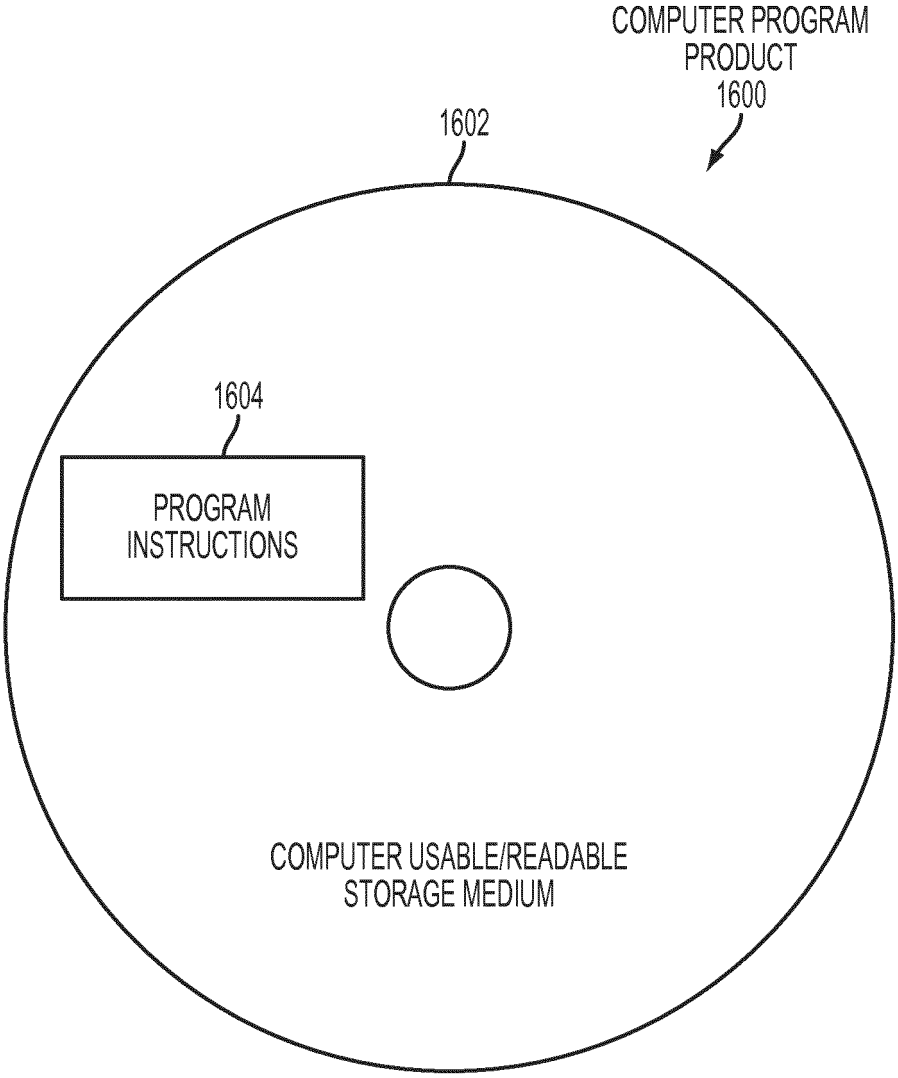
COMPUTER PROGRAM
PRODUCT
1600
1602
1604
PROGRAM
INSTRUCTIONS
COMPUTER USABLE/READABLE
STORAGE MEDIUM

FIG. 16